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seventh edition

ELECTRONIC DEVICES

CONVENTIONAL CURRENT VERSION

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SEVENTH EDITION

ELECTRONIC DEVICES

Thomas L. Floyd

PEARSON
Education
Delhi • Chandigarh • Chennai

Chapter opening photos by EyeWire, Inc.

Authorized adaptation from the United States edition, entitled *Electronic Devices, 7th Edition,* ISBN: 9780131140806 by Floyd, Thomas L., published by Pearson Education, Inc., © 2005

Indian Subcontinent Adaptation

ISBN 978-81-7758-643-5

First Impression
Second Impression, 2009

This edition is manufactured in India and is authorized for sale only in India, Bangladesh, Bhutan, Pakistan, Nepal, Sri Lanka and the Maldives.

Published by Dorling Kindersley (India) Pvt. Ltd., licensees of Pearson Education in South Asia.

Head Office: 482 F.I.E., Patparganj, Delhi 110 092, India.
Registered Office: 14 Local Shopping Centre, Panchsheel Park, New Delhi 110 017, India.

Printed in India at Swan Press.

Preface

This seventh edition of *Electronic Devices* has been carefully revised and some important new topics have been added. Several recommendations from reviewers and current users have been incorporated to make this edition better. A comprehensive coverage of electronic devices and circuits is provided. Chapters 1 through 11 are essentially devoted to fundamental discrete devices and circuits. Chapters 12 through 17 primarily cover linear integrated circuits. Chapter 18 is a new chapter that is completely devoted to programmable analog arrays. Data sheets are introduced in certain areas to provide a practical connection with actual devices. Extensive exercises and problems are designed to help students verify circuit theory and develop troubleshooting and measurement skills.

New in This Edition

New Chapter on Programmable Analog Arrays Chapter 18 introduces field-programmable analog arrays (FPAAs) and how to program them. Also, switched-capacitor circuits are described because they are basic to FPAA technology.

Objective-type Questions This feature is at the end of most chapters. It checks students' understanding of how changes in certain parameters affect the behavior of a circuit. Given a specified change in one parameter, students determine the resulting effect (increase, decrease, no change) in another parameter or parameters.

More Coverage of Optical Topics High-intensity LEDs are introduced and a new section on fiber optics has been added.

New Devices New sections on differential amplifiers and the IGBT (insulated gate bipolar transistor) are now included.

General Improvements Obsolete devices have been replaced, text descriptions have been reworded for greater clarity, and graphics have been enhanced in certain areas for better appearance or improved effectiveness.

Features

- One-page chapter openers containing a chapter outline and introduction.
- The beginning of each section includes a brief introduction for the section.
- Abundant worked-out examples, each with a related problem similar to that illustrated in the example. Answers to related problems are at the end of the chapter.
- Section Reviews with answers at the end of the chapter
- A typical chapter ends with a chapter summary and questions and answers to objective-type questions and problems.
- A problem set at the end of each chapter is divided by chapter sections, and generally organized into basic and advanced problems.

Chapter Features

Chapter Opener Each chapter begins with a chapter outline and a chapter introduction as shown in Figure P–1.

Section Opener Each section in a chapter begins with a brief introduction. An example is shown in Figure P–2.


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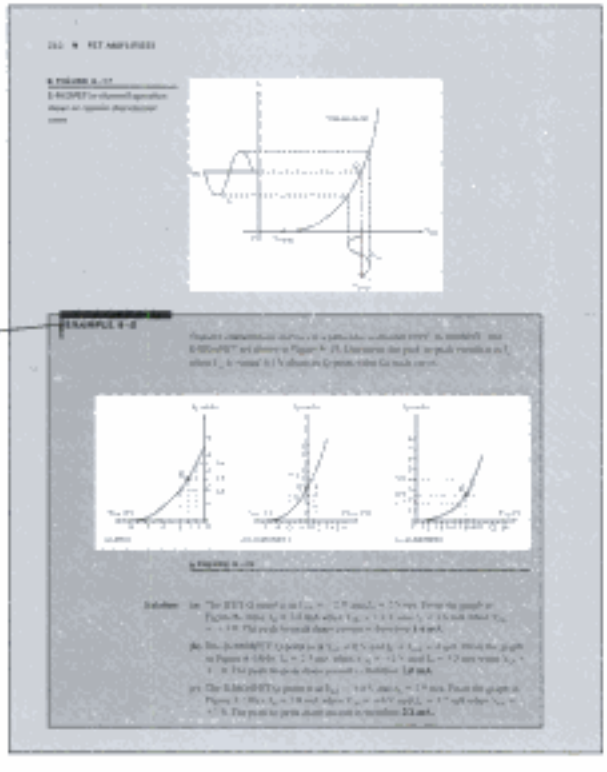
Section Review Each section in a chapter ends with a review consisting of questions that highlight the main concepts presented in the section. This feature is also illustrated in Figure P–2. The answers to the Section Reviews are at the end of the chapter.

Worked Examples and Related Problems Numerous worked examples throughout each chapter illustrate and clarify basic concepts or specific procedures. Each example ends with a Related Problem that reinforces or expands on the example by requiring the student to work through a problem similar to the example. Answers to Related Problems are at the end of the chapter.



Examples are set **off from text.**

◄ FIGURE P–3

A typical example with a related problem.

Chapter End Matter The following pedagogical features are found at the end of most chapters:

- Summary
- Obejective type Questions
- Basic Problems
- Advanced Problems
- Data Sheet Problems (selected chapters)
- Answers to Section Reviews
- Answers to Objective type Questions

Suggestions for Using This Textbook

As mentioned, this book covers discrete devices in Chapters 1 through 11, integrated circuits in Chapters 12 through 17, and programmable analog arrays in Chapter 18.

Option 1 (two terms) Chapters 1 through 11 can be covered in the first term. Depending on individual preferences and program emphasis, selective coverage may be necessary. For example, you may choose to omit Chapter 11 if the topic of thyristors is covered in a later industrial electronics course. Chapters 12 through 18 can be covered in the second term. Again, selective coverage may be necessary.

Option 2 (one term) By omitting certain topics and by maintaining a rigorous schedule, this book can be used in one-term courses. For example, a course covering only discrete devices and circuits would cover Chapters 1 through 11 with, perhaps, some selectivity.

Similarly, a course requiring only linear integrated circuit coverage would cover Chapters 12 through 18. Another approach is a very selective coverage of discrete devices and circuits topics followed by a limited coverage of integrated circuits (only op-amps, for example).

To the Student

There is a saying that applies to the study of this textbook as well as many other endeavors in life. It goes like this—*Do one thing at a time, do it very well, and then move on.*

When studying a particular chapter, study one section until you understand it and only then move on to the next one. Read each section and study the related illustrations carefully, think about the material, work through each example step by step, work its Related Problem and check the answer, and then answer each question in the section review, checking your answers at the end of the chapter. Don't expect each concept to be crystal clear after a single reading; you may have to read the material two or even three times. Once you think that you understand the material, review the chapter summary at the end of the chapter. Take the objective type questions and the self-test. Finally, work the assigned problems at the end of the chapter. Working through these problems is perhaps the most important way to check and reinforce your comprehension of the chapter. By working problems, you acquire an additional level of insight and understanding, and develop logical thinking that reading or classroom lectures alone do not provide.

Generally, you cannot fully understand a concept or procedure by simply watching or listening to someone else. Only hard work and critical thinking will produce the results you expect and deserve.

Thomas Alva Edison 1847–1931
Born in Milan, Ohio, Thomas Edison was the most prolific inventor of all time. He is credited with 1093 patents and is the only person to ever have at least one patent every year for 65 consecutive years. Mr. Edison's inventions and enterprises encompass many different areas. One of his most famous inventions, the light bulb, was introduced in 1879. Mr. Edison is credited with discovering the diode effect while working with vacuum tubes for the light bulb. Most of his work was done in his laboratory in West Orange, NJ. He also maintained a laboratory at his winter home in Fort Myers, Florida, which was devoted principally to the development of a synthetic rubber using the goldenrod plant. (Photo credit: Library of Congress)

Milestones in Electronics

Before you begin your study of electronic devices, let's briefly look at some of the important developments that led to the electronics technology we have today. The names of many of the early pioneers in electricity and electromagnetics still live on in terms of familiar units and quantities. Names such as Ohm, Ampere, Volta, Farad, Henry, Coulomb, Oersted, and Hertz are some of the better known examples with which you are already familiar. More widely known names such as Franklin and Edison are also significant in the history of electricity and electronics because of their tremendous contributions. Biographies of a few important figures in the history of electronics are shown.

Early experiments with electronics involved electric currents in vacuum tubes. Heinrich Geissler (1814–1879) removed most of the air from a glass tube and found that the tube glowed when there was current through it. Later, Sir William Crookes (1832–1919) found the current in vacuum tubes seemed to consist of particles. Thomas Edison (1847–1931) experimented with carbon filament bulbs with plates and discovered that there was a current from the hot filament to a positively charged plate. He patented the idea but never used it.

Other early experimenters measured the properties of the particles that flowed in vacuum tubes. Sir Joseph Thompson (1856–1940) measured properties of these particles, later called *electrons*.

Although wireless telegraphic communication dates back to 1844, electronics is basically a 20th century concept that began with the invention of the vacuum tube amplifier. An early vacuum tube that allowed current in only one direction was constructed by John A. Fleming in 1904. Called the Fleming valve, it was the forerunner of vacuum tube diodes. In 1907, Lee DeForest added a grid to the vacuum tube. The new device, called the audiotron, could amplify a weak signal. By adding the control element, DeForest ushered in the electronics revolution. It was an improved version of his device that made transcontinental telephone service and radios possible. In 1912, a radio amateur in San Jose, California, was regularly broadcasting music!

In 1921, the secretary of commerce, Herbert Hoover, issued the first license to a broadcast radio station; within two years over 600 licenses were issued. By the end of the 1920s radios were in many homes. A new type of radio, the superheterodyne radio, invented by Edwin Armstrong, solved problems with high-frequency communication. In 1923, Vladimir Zworykin, an American researcher, invented the first television picture tube, and in 1927 Philo T. Farnsworth applied for a patent for a complete television system.

The 1930s saw many developments in radio, including metal tubes, automatic gain control, "midget" radios, and directional antennas. Also started in this decade was the development of the first electronic computers. Modern computers trace their origins to the work of John Atanasoff at Iowa State University. Beginning in 1937, he envisioned a binary machine that could do complex mathematical work. By 1939, he and graduate student Clifford Berry had constructed a binary machine called ABC, (for Atanasoff-Berry Computer) that used vacuum tubes for logic and condensers (capacitors) for memory. In 1939, the magnetron, a microwave oscillator, was invented in Britain by Henry Boot and John Randall. In the same year, the klystron microwave tube was invented in America by Russell and Sigurd Varian.

The decade of the 1940s opened with World War II. The war spurred rapid advancements in electronics. Radar and very high-frequency communication were made possible by the

Lee DeForest
1873–1961
Born in Iowa, Lee DeForest became an inventor while in college to help defray expenses. He graduated from Yale in 1899 with a PhD. His doctoral thesis, "Reflection of Hertzian Waves from the Ends of Parallel Wires," began his long career in radio. His invention of the vacuum tube triode for use in amplification (audion amplifier) was the most important of his more than 300 inventions. (Photo credit: The National Cyclopedia of American Biography, courtesy AIP Emilio Segrè Visual Archives, T.J.J. See Collection)

John
Bardeen
1908–1991
An electrical engineer and physicist born in Madison, Wisconsin, Dr. Bardeen was on the faculty of the University of Minnesota from 1938 to 1941 and a physicist at the Naval Ordnance Lab from 1941 to 1945. He then joined Bell Labs and remained there until 1951. Some of his fields of interest were conduction in semiconductors and metals, surface properties of semiconductors, and superconductivity. While at Bell Labs he jointly invented the transistor with colleagues Walter Brattain and William Shockley. After leaving Bell Labs in 1951, Dr. Bardeen joined the faculty at the University of Illinois. (Photo credit: AIP Emilio Segrè Visual Archives, W. F. Meggers Gallery of Nobel Laureates)

William
Shockley
1910–1989
An American born in London, England, Dr. Shockley obtained his PhD in 1936 from M.I.T. He joined Bell Labs upon graduation and remained there until 1955. His research emphasis included areas of energy bands in solids, theory of vacuum tubes, photoelectrons, ferromagnetic domains, and transistor physics. While at Bell Labs, Dr. Shockley joined John Bardeen and Walter Brattain in the invention of the transistor in 1947. After leaving Bell Labs, Dr. Shockley spent time at Beckman Instruments and at Stanford University. (Photo credit: AIP Emilio Segrè Visual Archives, Physics Today Collection)

Walter
H. Brattain
1902–1987
An American born in China, Dr. Brattain joined Bell Telephone Laboratories in 1929. One of his main areas of research was the surface properties of semiconductive materials. His chief contributions were the discovery of the photo effect at the surface of a semiconductor and the invention of the point-contact transistor in 1947, which he jointly invented with John Bardeen and William Shockley. (Photo credit: AIP Emilio Segrè Visual Archives, W. F. Meggers Gallery of Nobel Laureates)

magnetron and klystron. Cathode ray tubes were improved for use in radar. Computer work continued during the war. By 1946, John von Neumann had developed the first stored program computer, the Eniac, at the University of Pennsylvania. One of the most significant inventions ever occurred in 1947 with the invention of the transistor. The inventors were Walter Brattain, John Bardeen, and William Shockley. All three won Nobel prizes for their invention. PC (printed circuit) boards were also introduced in 1947. Commercial manufacturing of transistors didn't begin until 1951 in Allentown, Pennsylvania.

The most important invention of the 1950s was the integrated circuit. On September 12, 1958, Jack Kilby, at Texas Instruments, made the first integrated circuit (Figure P–5), for which he was awarded a Nobel prize in the fall of 2000. This invention literally created the modern computer age and brought about sweeping changes in medicine, communication, manufacturing, and the entertainment industry. Many billions of "chips"—as integrated circuits came to be called—have since been manufactured.

► **FIGURE P–5**

The first integrated circuit. (Courtesy of Texas Instruments)

The 1960s saw the space race begin and spurred work on miniaturization and computers. The space race was the driving force behind the rapid changes in electronics that followed. The first successful "op-amp" was designed by Bob Widlar at Fairchild Semiconductor in 1965. Called the μA709, it was very successful but suffered from "latch-up" and other problems. Later, the most popular op-amp ever, the 741, took shape at Fairchild. This op-amp became the industry standard and influenced design of op-amps for years to come. Precursors to the Internet began in the 1960s with remote networked computers. Systems were in place within Lawrence Livermore National Laboratory that connected over 100 terminals to a computer system (colorfully called the "Octopus system"). In an experiment in 1969 with remote computers, an exchange took place between researchers at UCLA and Stanford. The UCLA group hoped to connect to a Stanford computer and began by typing the word "login" on its terminal. A separate telephone connection was set up and the following conversation occurred.

The UCLA group asked over the phone, "Do you see the letter L?"

"Yes, we see the L."

The UCLA group typed an O. "Do you see the letter O?"

"Yes, we see the O."

The UCLA group typed a G. At this point the system crashed. Such was technology, but a revolution was in the making.

By 1971, a new company that had been formed by a group from Fairchild introduced the first microprocessor. The company was Intel and the product was the 4004 chip, which had the same processing power as the Eniac computer. Later in that same year, Intel announced the first 8-bit processor, the 8008. In 1975, the first personal computer was introduced by Altair, and *Popular Science* magazine featured it on the cover of the January 1975 issue. The 1970s also saw the introduction of the pocket calculator and new developments in optical integrated circuits.

By the 1980s, half of all U.S. homes were using cable hookups instead of television antennas. The reliability, speed, and miniaturization of electronics continued throughout the 1980s, including automated testing and calibrating of PC boards. The computer became a part of instrumentation and the virtual instrument was created. Computers became a standard tool on the workbench.

Jack S. Kilby 1923–

Jack Kilby was born in Missouri and earned degrees in electrical engineering from the University of Illinois and the University of Wisconsin. From 1947 to 1958, he worked at the Centralab Division of Globe Union, Inc. in Milwaukee. In 1958, he joined Texas Instruments in Dallas where he was responsible for integrated circuit development and applications. Within a year after joining TI he invented the monolithic integrated circuit and the rest is history. Mr. Kilby left TI in 1970. (Photo credit: Courtesy of Texas Instruments)

The 1990s saw a widespread application of the Internet. In 1993, there were 130 websites; by the start of the new century (in 2001) there were over 24 million. In the 1990s, companies scrambled to establish a home page and many of the early developments of radio broadcasting had parallels with the Internet. The exchange of information and e-commerce fueled the tremendous economic growth of the 1990s. The Internet became especially important to scientists and engineers, becoming one of the most important scientific communication tools ever.

In 1995, the FCC allocated spectrum space for a new service called Digital Audio Radio Service. Digital television standards were adopted in 1996 by the FCC for the nation's next generation of broadcast television. As the 20th century drew toward a close, historians could only breathe a sign of relief. As one person put it, "I'm all for new technologies, but I wish they'd let the old ones wear out first."

The 21st century dawned on January 1, 2001 (although most people celebrated the new century the previous year, known as "Y2K"). The major story was the continuing explosive growth of the Internet; shortly thereafter, scientists were planning a new supercomputer system that would make massive amounts of information accessible in a computer network. The new international data grid will be an even greater resource than the World Wide Web, giving people the capability to access enormous amounts of information and the resources to run simulations on a supercomputer. Research in the 21st century continues along lines of faster and smaller circuits using new technologies. One promising area of research involves carbon nanotubes, which have been found to have properties of semiconductors in certain configurations.

Acknowledgments

Many capable people have been part of this revision for the seventh edition of *Electronic Devices*. It has been thoroughly reviewed and checked for both content and accuracy. Those at Pearson who have contributed greatly to this project throughout the many phases of development and production include Rex Davidson, Kate Linsner, and Dennis Williams. Lois Porter, whose attention to details is amazing, has once more done an outstanding job editing the manuscript. Jane Lopez has once again provided the excellent illustrations and beautiful graphics work used in the text. Toby Boydell has created the circuit files for the Multisim features in this edition. I also wish to thank Mark Fitzgerald, Ron Kolody, and David Mayo for their significant contributions with regard to the ancillaries for this edition.

I wish to express my appreciation to those already mentioned as well as the reviewers who provided many valuable suggestions and constructive criticism that greatly influenced this edition. These reviewers are Howard Carter, DeVry University—Kansas City; Mohamad S. Haj-Mohamadi, North Carolina A&T State University; Max Rabiee, University of Cincinnati; Stan Sluder, Boise State University; Randall Stratton, DeVry University—Irving; and Ronald Tinckham, Santa Fe Community College.

Tom Floyd

Dedication

Once Again, To Sheila

With Love

Brief Contents

Contents

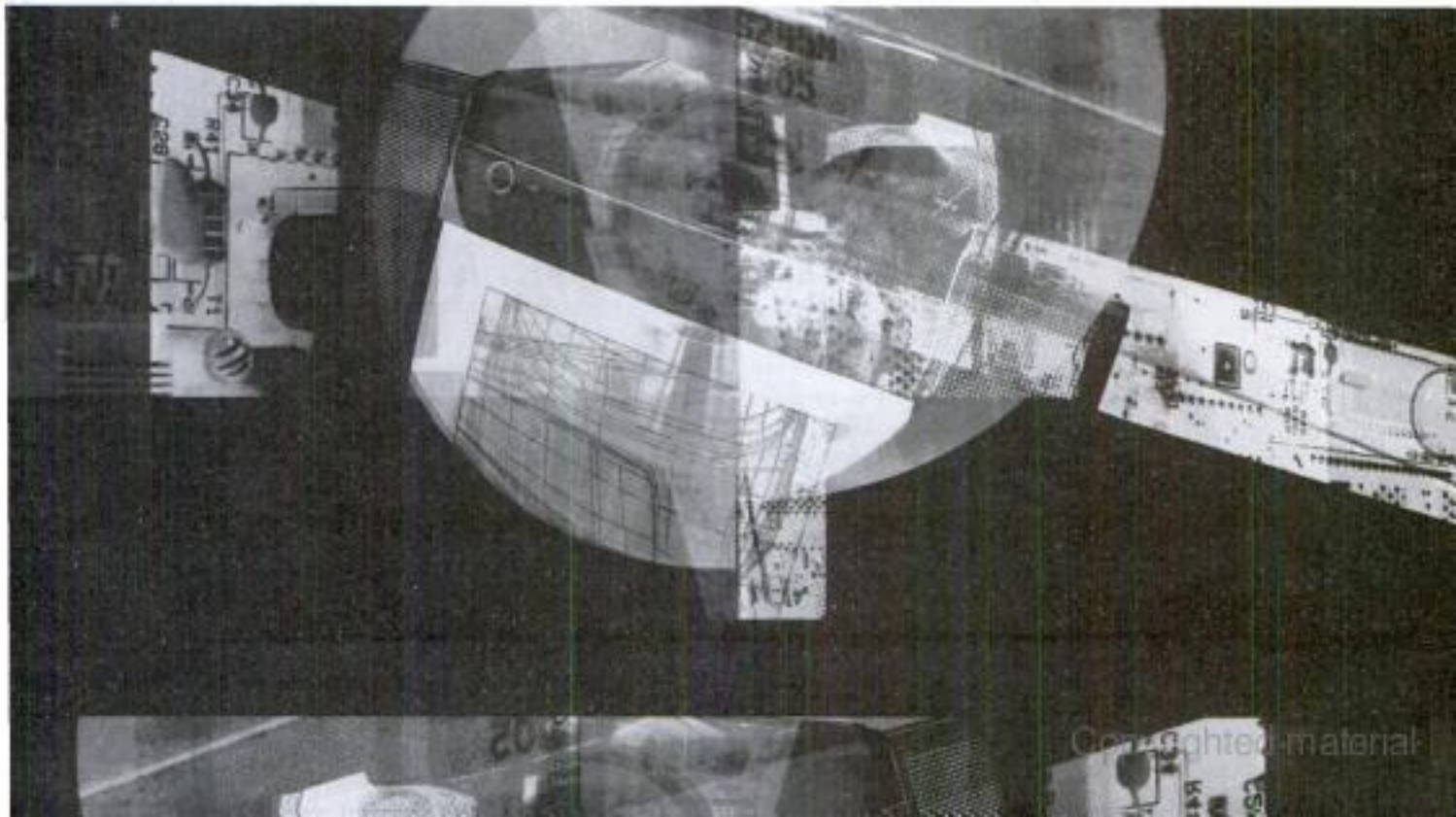
1

SEMICONDUCTOR BASICS

CHAPTER OUTLINE

INTRODUCTION

Electronic devices such as diodes, transistors, and integrated circuits are made of a semiconductive material. To properly understand how these devices work, you should have a basic knowledge of the structure of atoms and the interaction of atomic particles. An important concept introduced in this chapter is that of the *pn* junction that is formed when two different types of semiconductive material are joined. The *pn* junction is fundamental to the operation of devices such as the diode and certain types of transistors.



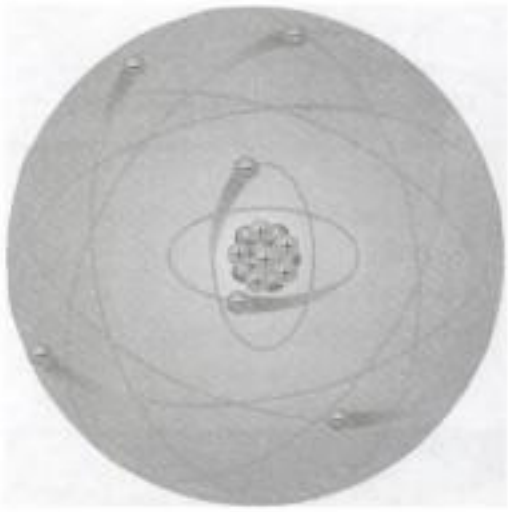
1–1 ATOMIC STRUCTURE

All matter is made of atoms; and all atoms consist of electrons, protons, and neutrons. In this section, you will learn about the structure of the atom, electron orbits and shells, valence electrons, ions, and two semiconductive materials—silicon and germanium. Semiconductive material is important because the configuration of certain electrons in an atom is the key factor in determining how a given material conducts electrical current.

An **atom*** is the smallest particle of an element that retains the characteristics of that element. Each element has a unique atomic structure. According to the classical Bohr model, atoms have a planetary type of structure that consists of a central nucleus surrounded by orbiting electrons, as illustrated in Figure 1–1. The **nucleus** consists of positively charged particles called **protons** and uncharged particles called **neutrons**. The basic particles of negative charge are called **electrons**.

▶ **FIGURE 1–1**

The Bohr model of an atom showing electrons in orbits around the nucleus, which consists of protons and neutrons. The "tails" on the electrons indicate motion.



Each type of atom has a certain number of electrons and protons that distinguishes it from the atoms of all other elements. For example, the simplest atom is that of hydrogen, which has one proton and one electron, as shown in Figure 1–2(a). As another example, the helium atom, shown in Figure 1–2(b), has two protons and two neutrons in the nucleus and two electrons orbiting the nucleus.

Electrons orbit the nucleus of an atom at certain distances from the nucleus. Electrons near the nucleus have less energy than those in more distant orbits.

Each discrete distance **(orbit)** from the nucleus corresponds to a certain energy level. In an atom, the orbits are grouped into energy bands known as **shells**. A given atom has a fixed number of shells. Each shell has a fixed maximum number of electrons at permissible energy levels (orbits). The differences in energy levels within a shell are much smaller than the difference in energy between shells. The shells are designated 1, 2, 3, and so on,

*All bold terms are in the end-of-book glossary.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If a valence electron acquires a sufficient amount of energy, it can actually escape from the outer shell and the atom's influence. The departure of a valence electron leaves a previously neutral atom with an excess of positive charge (more protons than electrons). The process of losing a valence electron is known as **ionization**, and the resulting positively charged atom is called a *positive ion*. For example, the chemical symbol for hydrogen is H. When a neutral hydrogen atom loses its valence electron and becomes a positive ion, it is designated H^+. The escaped valence electron is called a **free electron**. When a free electron loses energy and falls into the outer shell of a neutral hydrogen atom, the atom becomes negatively charged (more electrons than protons) and is called a *negative ion*, designated H^-. The process of raising an atom from the normal state to the ionized state is called *ionization*. Both these processes, excitation and ionization, are *absorption phenomena*.

The maximum number of electrons (N_e) that can exist in each shell of an atom can be calculated by the formula,

Equation 1–1

$$N_e = 2n^2$$

where n is the number of the shell. The innermost shell is number 1, the next shell is number 2, and so on. The maximum number of electrons that can exist in the innermost shell (shell 1) is

$$N_e = 2n^2 = 2(1)^2 = 2$$

The maximum number of electrons that can exist in the second shell is

$$N_e = 2n^2 = 2(2)^2 = 2(4) = 8$$

The maximum number of electrons that can exist in the third shell is

$$N_e = 2n^2 = 2(3)^2 = 2(9) = 18$$

The maximum number of electrons that can exist in the fourth shell is

$$N_e = 2n^2 = 2(4)^2 = 2(16) = 32$$

All shells in a given atom must be completely filled with electrons except the outer (valence) shell.

SECTION 1–1 REVIEW

Answers are at the end of the chapter.

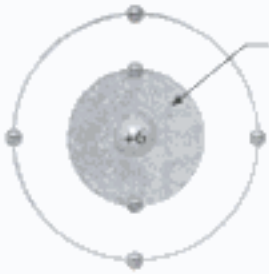
1. Describe an atom.
2. What is an electron?
3. What is a valence electron?
4. What is a free electron?
5. How are ions formed?

1–2 CLASSIFICATION OF MATTER ON THE BASIS OF SEMICONDUCTOR THEORY

In terms of their electrical properties, materials can be classified into three groups: conductors, semiconductors, and insulators. In this section, we will examine the properties of semiconductors and compare them to conductors and insulators.

All materials are made up of atoms. These atoms contribute to the electrical properties of a material, including its ability to conduct electrical current.

An atom can be represented by the valence shell and a **core** that consists of all the inner shells and the nucleus. This concept is illustrated in Figure 1–4 for a carbon atom. Carbon is used in some types of electrical resistors. Notice that the carbon atom has four



◀ **FIGURE 1–4**
Diagram of a carbon atom.

electrons in the valence shell and two electrons in the inner shell. The nucleus consists of six protons and six neutrons so the +6 indicates the positive charge of the six protons. The core has a net charge of +4 (+6 for the nucleus and −2 for the two inner-shell electrons).

Conductors

A **conductor** is a material that easily conducts electrical current. The best conductors are single-element materials, such as copper, silver, gold, and aluminum, which are characterized by atoms with only one valence electron very loosely bound to the atom. These loosely bound valence electrons can easily break away from their atoms and become free electrons. Therefore, a conductive material has many free electrons that, when moving in the same direction, make up the **current**.

Insulators

An **insulator** is a material that does not conduct electrical current under normal conditions. Most good insulators are compounds rather than single-element materials. Valence electrons are tightly bound to the atoms; therefore, there are very few free electrons in an insulator. Some examples of insulators are wood, glass, and diamond.

Semiconductors

A **semiconductor** is a material that is between conductors and insulators in its ability to conduct electrical current. A semiconductor in its pure state is neither a good conductor nor a good insulator. The most common single-element semiconductors are silicon, **germanium**, and **carbon**. Compound semiconductors such as gallium arsenide are also commonly used. The single-element semiconductors are characterized by atoms with four valence electrons. Pure semiconductors are known as *intrinsic semiconductors* and impure semiconductors are known as *extrinsic semiconductors*.

Energy Bands

Electrons of an atom revolve around the nucleus in permitted energy levels. The electrons in the outermost shell are not strongly bound to the nucleus. These electrons, as already discussed, are known as valence electrons. The band formed by energy levels with valence electrons is known as the *valence band*. When an electron acquires enough additional energy, it can leave the valence shell, become a *free electron*, and exist in what is known as the *conduction band*. In this band electron can move freely and is not tied to any given atom. This band is empty in the case of insulators and may be partially filled in most of the cases.

The difference in energy between the valence band and the conduction band is called an *energy gap*. This is the amount of energy that a valence electron must have in order to jump from the valence band to the conduction band. The energy gap between the valence band and the conduction band is known as *forbidden energy band* because there is no allowed energy state in this region.

▶ **FIGURE 1–5**

Energy diagrams for the three types of materials.

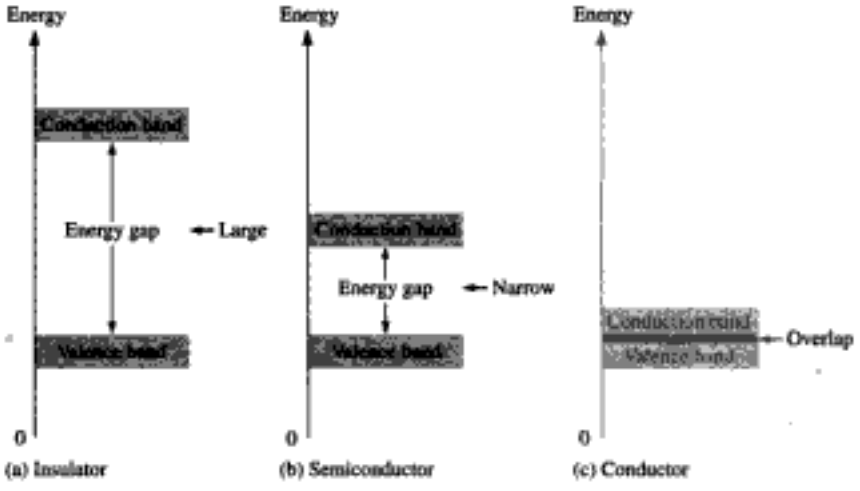


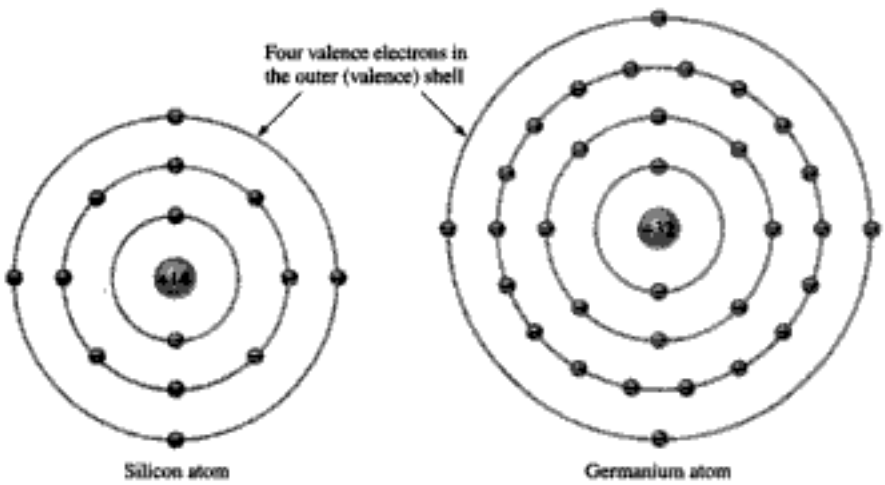
Figure 1–5 shows energy diagrams for insulators, semiconductors, and conductors. In part (a), the insulator has a very wide energy gap. Valence electrons do not jump into the conduction band except under breakdown conditions where extremely high voltages are applied across the material. In part (b), the semiconductor has a much narrower energy gap. This gap permits some valence electrons to jump into the conduction band and become free electrons. In germanium the energy gap is of the order of 0.7 ev and for silicon it is of the order 1.1 ev. At 0 K semiconductors behave as insulators because free electrons do not exist in the conduction band, and the valence band is totally filled. As temperature increases, the conduction band gets free electrons and starts conducting. Part (c) illustrates, the energy bands in conductors overlap. In a conductive material there is always a large number of free electrons.

Atomic Structure of Silicon and Germanium

The atomic structures of silicon and germanium are compared in Figure 1–6. **Silicon** is the most widely used material in diodes, transistors, integrated circuits, and other semiconductor devices. Both silicon and germanium have the characteristic four valence electrons.

▶ **FIGURE 1–6**

Diagrams of the silicon and germanium atoms.



The valence electrons in germanium are in the fourth shell while those in silicon are in the third shell, closer to the nucleus. This means that the germanium valence electrons are at higher energy levels than those in silicon and, therefore, require a smaller amount of additional energy to escape from the atom. This property makes germanium more unstable at high temperatures, and this is a basic reason why silicon is the most widely used semiconductive material.

SECTION 1–2 REVIEW

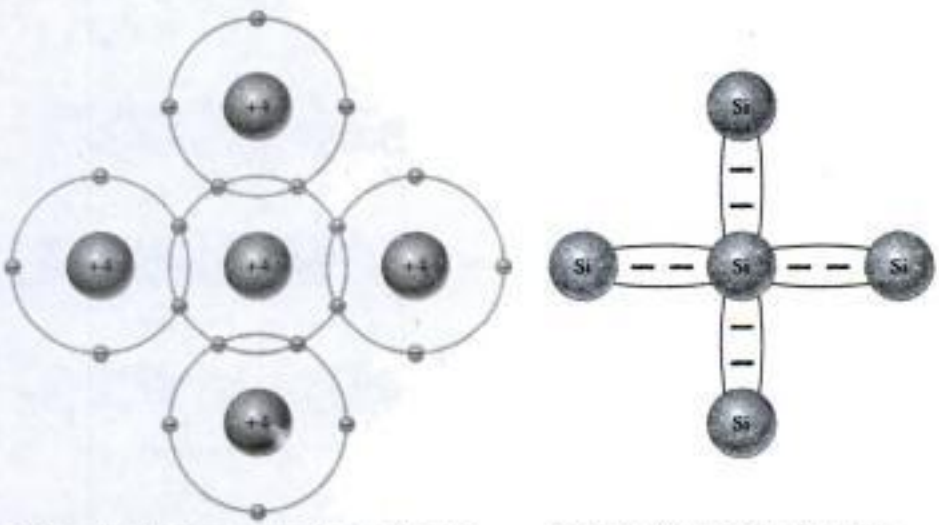
1. What is the basic difference between conductors and insulators?
2. How do semiconductors differ from conductors and insulators?
3. How many valence electrons does a conductor such as copper have?
4. How many valence electrons does a semiconductor have?
5. Name three of the best conductive materials.
6. What is the most widely used semiconductive material?
7. Why does a semiconductor have fewer free electrons than a conductor?

1–3 COVALENT BONDS

When atoms combine to form a solid, crystalline material, they arrange themselves in a symmetrical pattern. The atoms within the crystal structure are held together by covalent bonds, which are created by the interaction of the valence electrons of the atoms. Silicon is a crystalline material.

Figure 1–7 shows how each silicon atom positions itself with four adjacent silicon atoms to form a silicon **crystal**. A silicon (Si) atom with its four valence electrons shares an electron with each of its four neighbors. This effectively creates eight shared valence electrons for each atom and produces a state of chemical stability. Also, this sharing of valence electrons produces the **covalent** bonds that hold the atoms together; each valence electron is attracted equally by the two adjacent atoms which share it. Covalent bonding in an intrinsic silicon crystal is shown in Figure 1–8. An **intrinsic** crystal is one that has no impurities. Covalent bonding for germanium is similar because it also has four valence electrons.

◀ **FIGURE 1–7**
Illustration of covalent bonds in silicon.

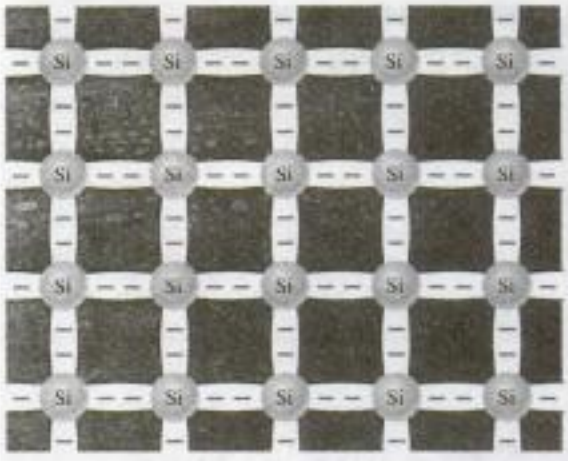


(a) The center silicon atom shares an electron with each of the four surrounding silicon atoms, creating a covalent bond with each. The surrounding atoms are in turn bonded to other atoms, and so on.

(b) Bonding diagram. The negative signs represent the shared valence electrons.

► FIGURE 1–8

Covalent bonds in a silicon crystal.



SECTION 1–3 REVIEW

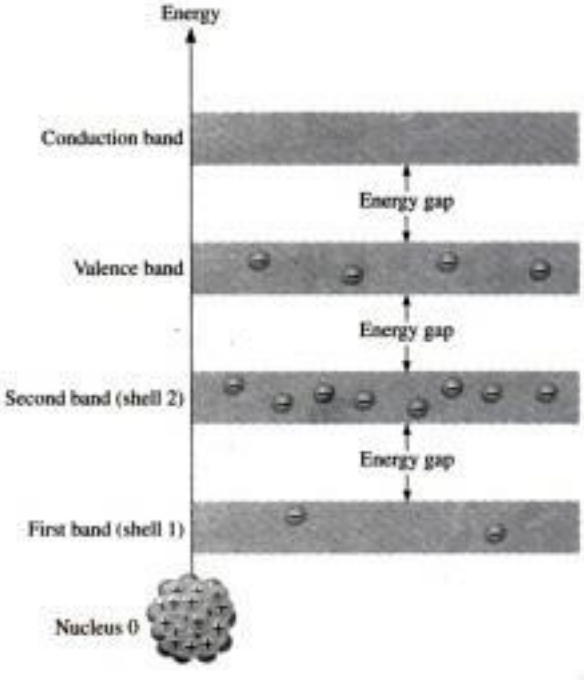
1. How are covalent bonds formed?
2. What is meant by the term *intrinsic*?
3. What is a crystal?
4. Effectively, how many valence electrons are there in each atom within a silicon crystal?

1–4 CONDUCTION IN SEMICONDUCTORS

The electrons of an atom can exist only within prescribed energy bands. Each shell around the nucleus corresponds to a certain energy band and is separated from adjacent shells by energy gaps, in which no electrons can exist. Figure 1–9 shows the energy band diagram for an unexcited (no external energy such as heat) atom in a pure silicon crystal. This condition occurs *only* at a temperature of absolute 0 Kelvin.

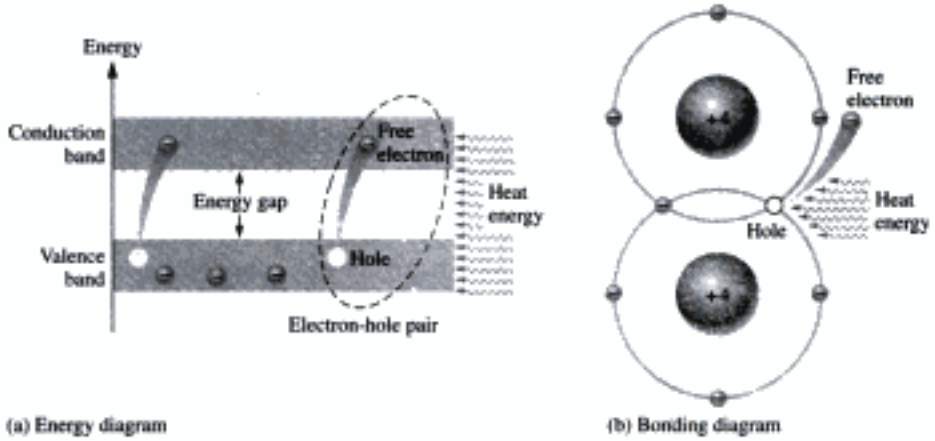
► FIGURE 1–9

Energy band diagram for an unexcited atom in a pure (intrinsic) silicon crystal. There are no electrons in the conduction band.



Conduction Electrons and Holes

An intrinsic (pure) silicon crystal at room temperature has sufficient heat (thermal) energy for some valence electrons to jump the gap from the valence band into the conduction band, becoming free electrons. Free electrons are also called **conduction electrons**. This is illustrated in the energy diagram of Figure 1–10(a) and in the bonding diagram of Figure 1–10(b).



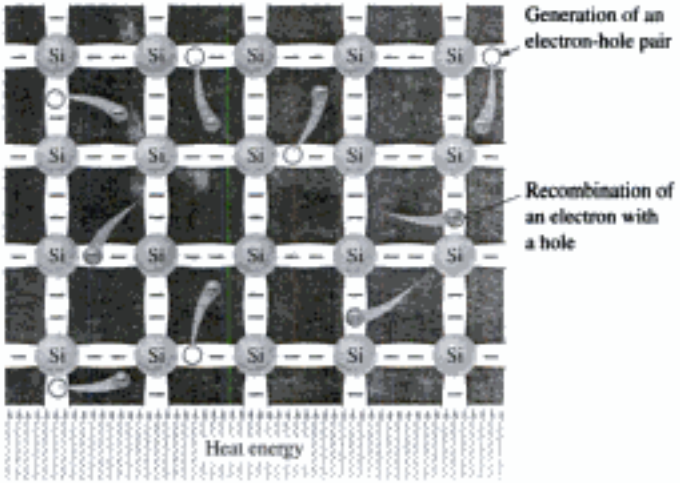
(a) Energy diagram (b) Bonding diagram

◀ FIGURE 1–10

Creation of electron-hole pairs in a silicon crystal. Electrons in the conduction band are free electrons.

When an electron jumps to the conduction band, a vacancy is left in the valence band within the crystal. This vacancy is called a **hole**. For every electron raised to the conduction band by external energy, there is one hole left in the valence band, creating what is called an **electron-hole pair**. **Recombination** occurs when a conduction-band electron loses energy and falls back into a hole in the valence band.

A piece of intrinsic silicon at room temperature has, at any instant, a number of conduction-band (free) electrons that are unattached to any atom and are essentially drifting randomly throughout the material. There is also an equal number of holes in the valence band created when these electrons jump into the conduction band. This is illustrated in Figure 1–11.



◀ FIGURE 1–11

Electron-hole pairs in a silicon crystal. Free electrons are being generated continuously while some recombine with holes.

Electron and Hole Current

When a voltage is applied across a piece of intrinsic silicon, as shown in Figure 1–12, the thermally generated free electrons in the conduction band, which are free to move randomly in the crystal structure, are now easily attracted toward the positive end. This movement of free electrons is one type of current in a semiconductive material and is called *electron current*.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Conductivity

In metals, conductivity takes place because of their free electrons. In the case of semiconductors, conduction also takes place due to electrons *and* holes. In the case of semiconductor we have to consider electrons in the conduction band and the holes in the valence band.

The conductivity of a metal is given by

$$\sigma = n_e \mu_e.$$

Let n: Electron density in the conduction band per unit volume.
p: Hole density in the valence band.
μ_e: Electron mobility.
μ_h: Hole mobility.

The conductivity (σ_n) of the semiconductor due to electrons is given by

$$\sigma_n = n_e \mu_e$$

and the conductivity (σ_p) of the semiconductor due to holes is given by

$$\sigma_p = p_e \mu_h$$

The total conductivity,

$$\sigma = \sigma_n + \sigma_p$$
$$= e(n\mu_e + p\mu_h).$$

In the case of pure semiconductors, we have a number of electrons (n) = a number of holes (p). Hence, the conductivity is given by

$$\sigma_{ins} = en(\mu_e + \mu_h)$$

Intrinsic concentration

The relation between intrinsic concentration and temperature is given by

$$n_i^2 = A_0 T^2 \exp[-E_G/K_T]$$

where A_0 is constant;
k is the Boltzman constant and
E_G is the energy gap at 0 K.

This expression shows that the intrinsic concentration increases with temperature, which, in turn, increases the conductivity.

Energy gap

The energy gap for silicon is given by $E_G = 1.21 - 3.60 \times 10^{-4} T$ and for germanium (E_G) = $0.785 - 2.23 \times 10^{-4} T$ where 'T' is the temperature. At room temperature E_G for silicon is equal to 0.72 ev and for germanium, it is equal to 1.1 ev.

Mobility

Electrons move faster than holes. For silicon, (mobility) m is 2.5 for electrons and 2.7 for holes. For germanium m is equal to 1.66 for electrons and 2.33 for holes.

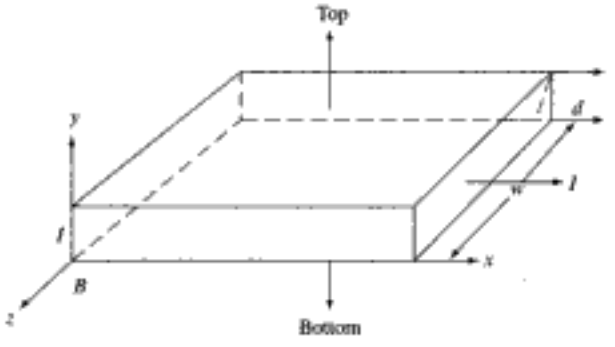
Hall effect

With a semiconductor, it is necessary to know whether it is a n-type or p-type, its carrier concentration and the mobility of its charge carriers. These parameters can be determined by using the **Hall Effect**.

If a metal or semiconductor carrying a current (I) is placed in a magnetic field (B) perpendicular to current, an electric field (E) is induced in the direction perpendicular to both current (I) and magnetic field B as illustrated in Figure 1–14. This phenomenon is known as the *Hall Effect*.

Let us assume that the current (I) is in the positive x-direction and the magnetic field (B) is in the positive z-direction. This exerts a force in the negative y-direction. If the material considered is an n-type semiconductor, then the charge carriers are electrons. Because of the negative force these electrons are forced to the bottom. This indicates that the bottom will

▶ FIGURE 1–14



be more negatively charged than the top. This produces a voltage difference between the two surfaces. Hence, a potential known as Hall Voltage (V_H) appears between the two surfaces. When in equilibrium, the electric field intensity (E) is equal to the magnetic force (B).

Therefore, $eE = Bev$

where V is the drift velocity of the electrons; B is the magnetic field intensity.

$E = Bv$;

The value of $E = \dfrac{V_H}{d}$

where V_H is the Hall voltage and d is the thickness of the semiconductor.

Let current density $J = \dfrac{I}{wd}$

where I is the current, w is the width and d is the thickness.
We have

$$V_H = Ed \text{ and } E = Bv$$
$$\therefore V_H = Bvd$$

But $v = \dfrac{J}{\rho}$ where ρ is the charge density.

$$= \frac{BJd}{\rho}$$

But $J = \dfrac{I}{wd}$

$$\therefore V_H = \frac{BId}{\rho wd} = \frac{BI}{\rho w}$$

$$\therefore V_H = \frac{BI}{\rho w}$$

If the semiconductor is a p-type then the bottom of the field is more positive than the top. We have $\rho = n \times e$ or $\rho = p \times e$ depending upon the type of material.

$$\rho = \frac{BI}{V_H w}$$

$$\therefore R_H = \frac{V_H w}{BI}$$

where R_H is the Hall Coefficient. It is equal to $1/\rho$. For an n-type semiconductor,

$$\sigma = ne\mu, \quad \text{but } ne = \rho$$
$$\therefore \sigma = \rho \times \mu$$
$$= \frac{1}{R_H} \times \mu$$

$$\therefore \mu = \sigma \times R_H = \sigma \times \frac{Bl}{V_H w}$$

The above expression is obtained on the assumption that the *drift velocity* is the same for all carriers. But this is not true for all practical considerations. Experiments have shown that the results obtained are more accurate if $1/R_H$ is taken as $3\pi/8\rho$

$$\therefore \mu = \frac{8\sigma}{3\pi} \times R_H$$

The product *Bev* is known as the **Lorentz force**. This shows that, the majority of carriers in semiconductors will move in a direction perpendicular to the magnetic field.

1–6 N-TYPE AND P-TYPE SEMICONDUCTORS

Semiconductive materials do not conduct current well and are of limited value in their intrinsic state. This is because of the limited number of free electrons in the conduction band and holes in the valence band. Intrinsic silicon or germanium must be modified by increasing the number of free electrons or holes to increase its conductivity and make it useful in electronic devices. This is done by adding impurities to the intrinsic material. Two types of extrinsic (impure) semiconductive materials, *n*-type and *p*-type, are the key building blocks for most types of electronic devices.

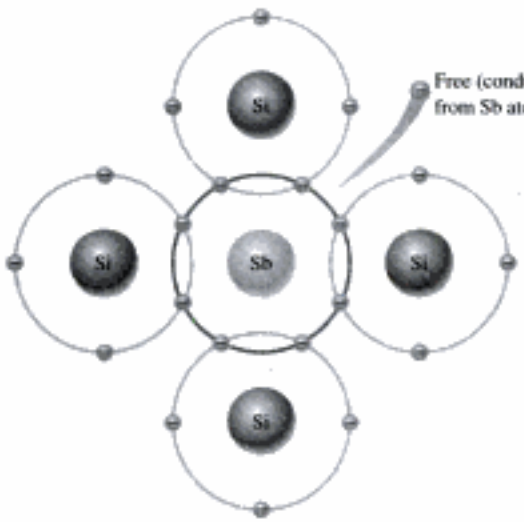
Doping

The conductivity of silicon and germanium can be drastically increased by the controlled addition of impurities to the intrinsic (pure) semiconductive material. This process, called **doping**, increases the number of current carriers (electrons or holes). The two categories of impurities are *n*-type and *p*-type.

N-Type Semiconductor

To increase the number of conduction-band electrons in intrinsic silicon, **pentavalent** impurity atoms are added. These are atoms with five valence electrons such as arsenic (As), phosphorus (P), bismuth (Bi), and antimony (Sb).

As illustrated in Figure 1–15, each pentavalent atom (antimony, in this case) forms covalent bonds with four adjacent silicon atoms. Four of the antimony atom's valence



◀ FIGURE 1–15

Pentavalent impurity atom in a silicon crystal structure. An antimony (Sb) impurity atom is shown in the center. The extra electron from the Sb atom becomes a free electron.

electrons are used to form the covalent bonds with silicon atoms, leaving one extra electron. This extra electron becomes a conduction electron because it is not attached to any atom. Because the pentavalent atom gives up an electron, it is often called a *donor atom*. The number of conduction electrons can be carefully controlled by the number of impurity atoms added to the silicon. A conduction electron created by this doping process does not leave a hole in the valence band because it is in excess of the number required to fill the valence band.

Majority and Minority Carriers Since most of the current carriers are electrons, silicon (or germanium) doped with pentavalent atoms is an *n*-type semiconductor (the *n* stands for the negative charge on an electron). The electrons are called the **majority carriers** in *n*-type material. Although the majority of current carriers in *n*-type material are electrons, there are also a few holes that are created when electron-hole pairs are thermally generated. These holes are *not* produced by the addition of the pentavalent impurity atoms. Holes in an *n*-type material are called **minority carriers**.

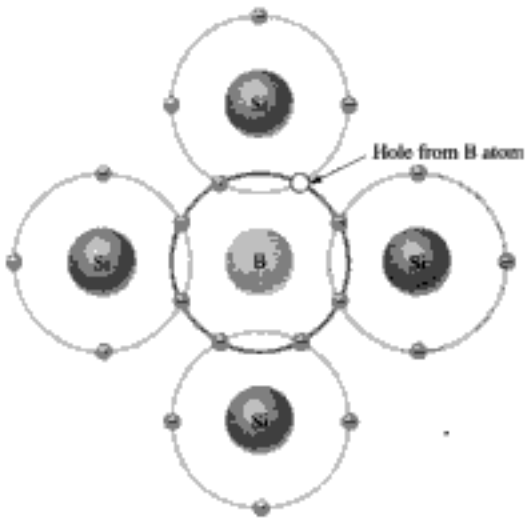
p-Type Semiconductor

To increase the number of holes in intrinsic silicon, **trivalent** impurity atoms are added. These are atoms with three valence electrons such as boron (B), indium (In), and gallium (Ga). As illustrated in Figure 1–16, each trivalent atom (boron, in this case) forms covalent bonds with four adjacent silicon atoms. All three of the boron atom's valence electrons are used in the covalent bonds; and, since four electrons are required, a hole results when each trivalent atom is added. Because the trivalent atom can take an electron, it is often referred to as an *acceptor atom*. The number of holes can be carefully controlled by the number of trivalent impurity atoms added to the silicon. A hole created by this doping process is *not* accompanied by a conduction (free) electron.

Majority and Minority Carriers Since most of the current carriers are holes, silicon (or germanium) doped with trivalent atoms is called a *p*-type semiconductor. Holes can be thought of as positive charges because the absence of an electron leaves a net positive charge on the atom. The holes are the majority carriers in *p*-type material. Although the majority of current carriers in *p*-type material are holes, there are also a few free electrons that are created when electron-hole pairs are thermally generated. These free electrons are *not* produced by the addition of the trivalent impurity atoms. Electrons in *p*-type material are the minority carriers.

► **FIGURE 1–16**

Trivalent impurity atom in a silicon crystal structure. A boron (B) impurity atom is shown in the center.



SECTION 1–6 REVIEW

1. Define *doping*.
2. What is the difference between a pentavalent atom and a trivalent atom? What are other names for these atoms?
3. How is an *n*-type semiconductor formed?
4. How is a *p*-type semiconductor formed?
5. What is the majority carrier in an *n*-type semiconductor?
6. What is the majority carrier in a *p*-type semiconductor?
7. By what process are the majority carriers produced?
8. By what process are the minority carriers produced?
9. What is the difference between intrinsic and extrinsic semiconductors?

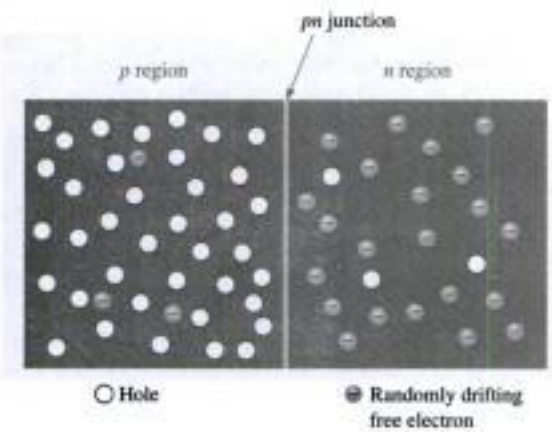
1–7 THE DIODE

If a block of silicon is doped with a trivalent impurity and the other part with a pentavalent impurity, a boundary called the *pn* junction is formed between the resulting *p*-type and *n*-type portions and a basic diode is created. A **diode** is a device that conducts current in only one direction. The *pn* junction is the feature that allows diodes, certain transistors, and other devices to work.

A *p*-type material consists of silicon atoms and trivalent impurity atoms such as boron. The boron atom adds a hole when it bonds with the silicon atoms. However, since the number of protons and the number of electrons are equal throughout the material, there is no net charge in the material and so it is neutral.

An *n*-type silicon material consists of silicon atoms and pentavalent impurity atoms such as antimony. As you have seen, an impurity atom releases an electron when it bonds with four silicon atoms. Since there is still an equal number of protons and electrons throughout the material, there is no net charge in the material and so it is neutral.

If a piece of intrinsic silicon is doped so that part is *n*-type and the other part is *p*-type, a ***pn* junction** forms at the boundary between the two regions and a diode is created, as indicated in Figure 1–17. The *p* region has many holes (majority carriers) from the impurity atoms and only a few thermally generated free electrons (minority carriers). The *n* region has many free electrons (majority carriers) from the impurity atoms and only a few thermally generated holes (minority carriers).



◀ FIGURE 1–17

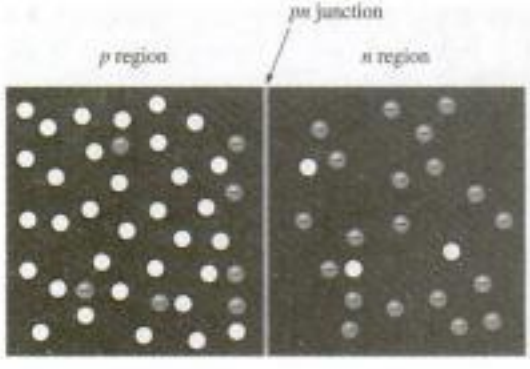
The basic diode structure at the instant of junction formation showing only the majority and minority carriers.

Formation of the Depletion Region

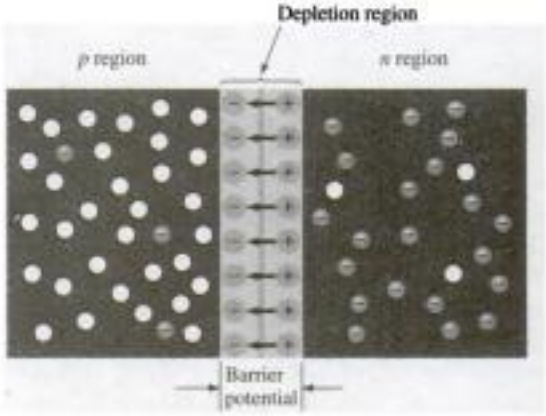
The free electrons in the *n* region are randomly drifting in all directions. At the instant of the *pn* junction formation, the free electrons near the junction in the *n* region begin to diffuse across the junction into the *p* region where they combine with holes near the junction, as shown in Figure 1–18(a).

Before the *pn* junction is formed, recall that there are as many electrons as protons in the *n*-type material, making the material neutral in terms of net charge. The same is true for the *p*-type material.

When the *pn* junction is formed, the *n* region loses free electrons as they diffuse across the junction. This creates a layer of positive charges (pentavalent ions) near the junction. As the electrons move across the junction, the *p* region loses holes as the electrons and holes combine. This creates a layer of negative charges (trivalent ions) near the junction. These two layers of positive and negative charges form the **depletion region**, as shown in Figure 1–18(b). The term *depletion* refers to the fact that the region near the *pn* junction is depleted of charge carriers (electrons and holes) due to diffusion across the junction. The depletion region is formed very quickly and is very thin compared to the *n* region and *p* region.



(a) At the instant of junction formation, free electrons in the *n* region near the *pn* junction begin to diffuse across the junction and fall into holes near the junction in the *p* region.



(b) For every electron that diffuses across the junction and combines with a hole, a positive charge is left in the *n* region and a negative charge is created in the *p* region, forming a barrier potential. This action continues until the voltage of the barrier repels further diffusion.

▲ FIGURE 1–18

Formation of the depletion region. The width of the depletion region is exaggerated for illustration purposes.

After the initial surge of free electrons across the *pn* junction, the depletion region has expanded to a point where equilibrium is established and there is no further diffusion of electrons across the junction. This occurs as follows. As electrons continue to diffuse across the junction, more and more positive and negative charges are created near the junction as the depletion region is formed. A point is reached where the total negative charge in the depletion region repels any further diffusion of electrons (negatively charged particles) into the *p* region (like charges repel) and the diffusion stops. In other words, the depletion region acts as a barrier to the further movement of electrons across the junction.

Barrier Potential Any time there is a positive charge and a negative charge near each other, there is a force acting on the charges as described by Coulomb's law. In the depletion region there are many positive charges and many negative charges on opposite sides of the *pn* junction. The forces between the opposite charges form a "field of forces" called an *electric field*,

as illustrated in Figure 1–18(b) by the arrows between the positive charges and the negative charges. This electric field is a barrier to the free electrons in the *n* region, and energy must be expended to move an electron through the electric field. That is, external energy must be applied to get the electrons to move across the barrier of the electric field in the depletion region.

The potential difference of the electric field across the depletion region is the amount of voltage required to move electrons through the electric field. This potential difference is called the **barrier potential** and is expressed in volts. A certain amount of voltage equal to the barrier potential and with the proper polarity must be applied across a *pn* junction before electrons will begin to flow across the junction.

The barrier potential of a *pn* junction depends on several factors, including the type of semiconductive material, the amount of doping, and the temperature. The typical barrier potential is approximately 0.7 V for silicon and 0.3 V for germanium at 25°C. Throughout the rest of the book, silicon will be used unless otherwise stated.

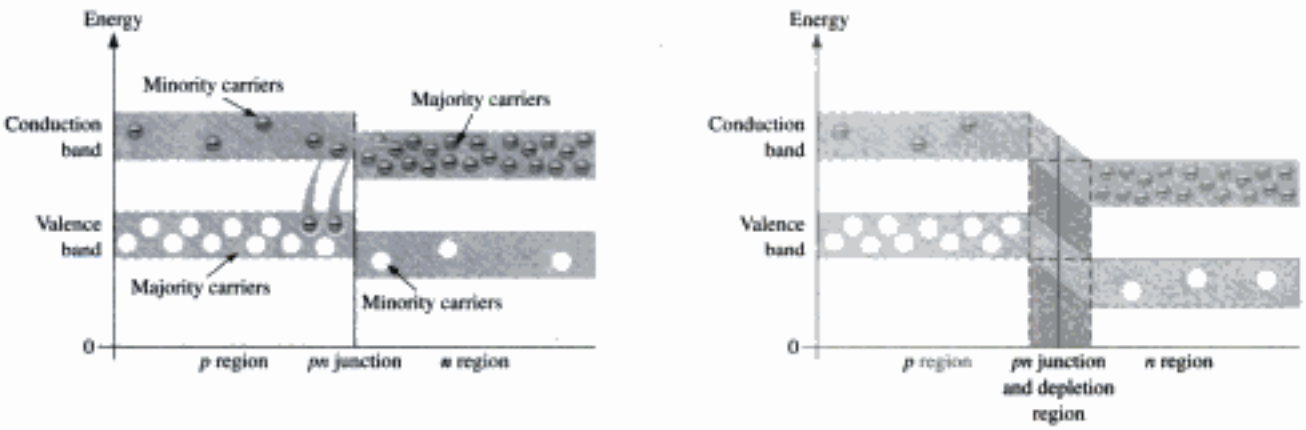
Energy Diagrams of the *PN* Junction and Depletion Region

The valence and conduction bands in an *n*-type material are at slightly lower energy levels than the valence and conduction bands in a *p*-type material. This is due to differences in the atomic characteristics of the pentavalent and the trivalent impurity atoms.

An energy diagram for a *pn* junction at the instant of formation is shown in Figure 1–19(a). The valence and conduction bands in the *n* region are at lower energy levels than those in the *p* region, but there is a significant amount of overlapping.

The free electrons in the *n* region that occupy the upper part of the conduction band in terms of their energy can easily diffuse across the junction (they do not have to gain additional energy) and temporarily become free electrons in the lower part of the *p*-region conduction band. After crossing the junction, the electrons quickly lose energy and fall into the holes in the *p*-region valence band as indicated in Figure 1–19(a).

As the diffusion continues, the depletion region begins to form and the energy level of the *n*-region conduction band decreases. The decrease in the energy level of the conduction band in the *n* region is due to the loss of the higher-energy electrons that have diffused across the junction to the *p*-region. Soon, there are no electrons left in the *n*-region conduction band with enough energy to get across the junction to the *p*-region conduction band, as indicated by the alignment of the top of the *n*-region conduction band and the bottom of the *p*-region conduction band in Figure 1-19(b). At this point, the junction is at equilibrium; and the depletion region is complete because diffusion has ceased. There is an energy gradiant across the depletion region which acts as an "energy hill" that an *n*-region electron must climb to get to the *p*-region.



(a) At the instant of junction formation

(b) At equilibrium

▲ FIGURE 1–19

Energy diagrams illustrating the formation of the *pn* junction and depletion region.

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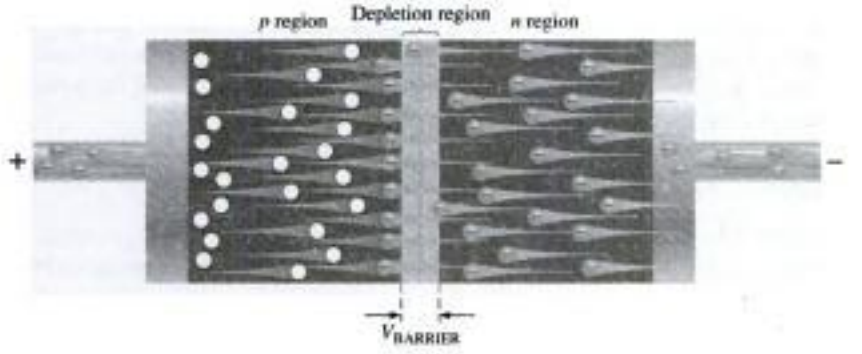
Once in the *p* region, these conduction electrons have lost enough energy to immediately combine with holes in the valence band.

Now, the electrons are in the valence band in the *p* region, simply because they have lost too much energy overcoming the barrier potential to remain in the conduction band. Since unlike charges attract, the positive side of the bias-voltage source attracts the valence electrons toward the left end of the *p* region. The holes in the *p* region provide the medium or



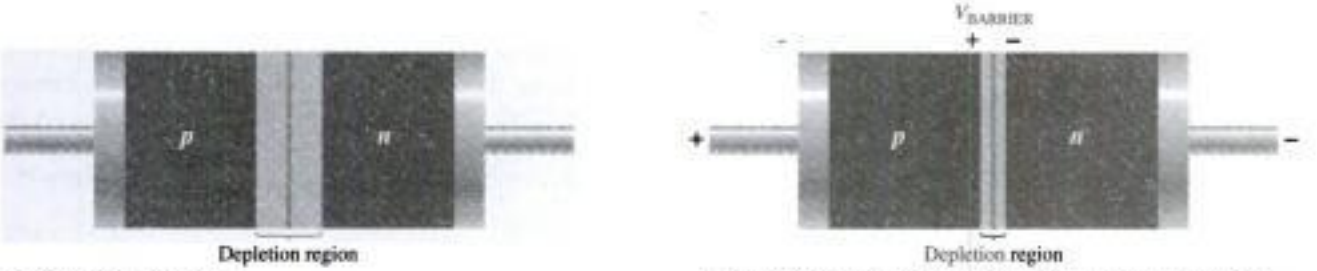
◀ FIGURE 1–21

A forward-biased diode showing the flow of majority carriers and the voltage due to the barrier potential across the depletion region.

"pathway" for these valence electrons to move through the *p* region. The electrons move from one hole to the next toward the left. The holes, which are the majority carriers in the *p* region, effectively (not actually) move to the right toward the junction, as you can see in Figure 1–21. This *effective* flow of holes is called the *hole current*. You can also view the hole current as being created by the flow of valence electrons through the *p* region, with the holes providing the only means for these electrons to flow.

As the electrons flow out of the *p* region through the external connection (conductor) and to the positive side of the bias-voltage source, they leave holes behind in the *p* region; at the same time, these electrons become conduction electrons in the metal conductor. So, there is a continuous availability of holes effectively moving toward the *pn* junction to combine with the continuous stream of electrons as they come across the junction into the *p* region.

The Effect of Forward Bias on the Depletion Region As more electrons flow into the depletion region, the number of positive ions is reduced. As more holes effectively flow into the depletion region on the other side of the *pn* junction, the number of negative ions is reduced. This reduction in positive and negative ions during forward bias causes the depletion region to narrow, as indicated in Figure 1–22.



(a) At equilibrium (no bias)

(b) Forward bias narrows the depletion region and produces a voltage drop across the *pn* junction equal to the barrier potential.

▲ FIGURE 1–22

The depletion region narrows and a voltage drop is produced across the *pn* junction when the diode is forward-biased.

The Effect of the Barrier Potential During Forward Bias Recall that the electric field between the positive and negative ions in the depletion region on either side of the junction

creates an "energy hill" that prevents free electrons from diffusing across the junction at equilibrium (see Figure 1–19(b)). This is known as the *barrier potential*.

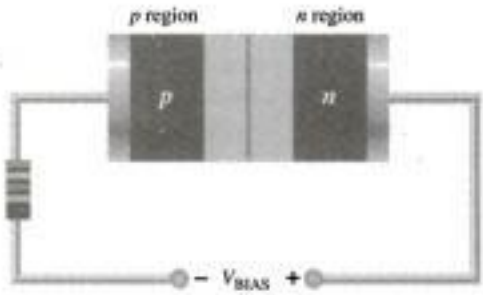
When forward bias is applied, the free electrons are provided with enough energy from the bias-voltage source to overcome the barrier potential and effectively "climb the energy hill" and cross the depletion region. The energy that the electrons require in order to pass through the depletion region is equal to the barrier potential. In other words, the electrons give up an amount of energy equivalent to the barrier potential when they cross the depletion region. This energy loss results in a voltage drop across the *pn* junction equal to the barrier potential (0.7 V), as indicated in Figure 1–22(b). An additional small voltage drop occurs across the *p* and *n* regions due to the internal resistance of the material. For doped semiconductive material, this resistance, called the **dynamic resistance**, is very small and can usually be neglected.

Reverse Bias

Reverse bias is the condition that essentially prevents current through the diode. Figure 1–23 shows a dc voltage source connected across a diode in the direction to produce reverse bias. This external bias voltage is designated as V_{BIAS} just as it was for forward bias. Notice that the positive side of V_{BIAS} is connected to the *n* region of the diode and the negative side is connected to the *p* region. Also note that the depletion region is shown much wider than in forward bias or equilibrium.

▶ FIGURE 1–23

A diode connected for reverse bias. A limiting resistor is shown although it is not important in reverse bias because there is essentially no current.



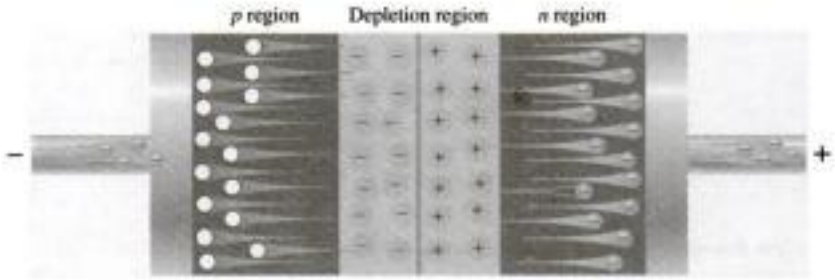
An illustration of what happens when a diode is reverse-biased is shown in Figure 1–24. Because unlike charges attract, the positive side of the bias-voltage source "pulls" the free electrons, which are the majority carriers in the *n* region, away from the *pn* junction. As the electrons flow toward the positive side of the voltage source, additional positive ions are created. This results in a widening of the depletion region and a depletion of majority carriers.

In the *p* region, electrons from the negative side of the voltage source enter as valence electrons and move from hole to hole toward the depletion region where they create additional negative ions. This results in a widening of the depletion region and a depletion of majority carriers. The flow of valence electrons can be viewed as holes being "pulled" toward the positive side.

The initial flow of charge carriers is transitional and lasts for only a very short time after the reverse-bias voltage is applied. As the depletion region widens, the availability of majority

▶ FIGURE 1–24

The diode during the short transition time immediately after reverse-bias voltage is applied.



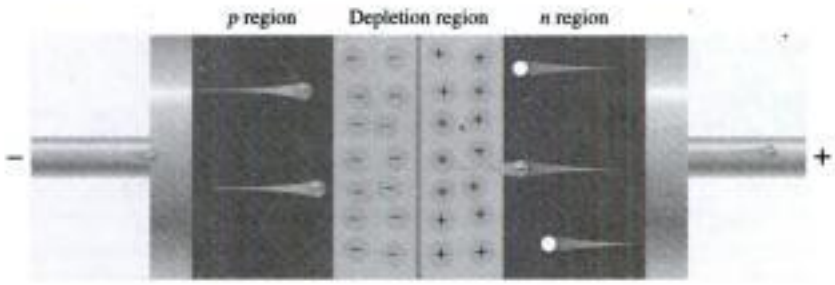
carriers decreases. As more of the *n* and *p* regions become depleted of majority carriers, the electric field between the positive and negative ions increases in strength until the potential across the depletion region equals the bias voltage, V_{BIAS}. At this point, the transition current essentially ceases except for a very small reverse current that can usually be neglected.

Reverse Current The extremely small current that exists in reverse bias after the transition current dies out is caused by the minority carriers in the *n* and *p* regions that are produced by thermally generated electron-hole pairs. The small number of free minority electrons in the *p* region are "pushed" toward the *pn* junction by the negative bias voltage. When these electrons reach the wide depletion region, they "fall down the energy hill" and combine with the minority holes in the *n* region as valence electrons and flow toward the positive bias voltage, creating a small hole current.

The conduction band in the *p* region is at a higher energy level than the conduction band in the *n* region. Therefore, the minority electrons easily pass through the depletion region because they require no additional energy. Reverse current is illustrated in Figure 1–25.

Reverse Breakdown Normally, the reverse current is so small that it can be neglected. However, if the external reverse-bias voltage is increased to a value called the *breakdown voltage*, the reverse current will drastically increase.

The high reverse-bias voltage imparts energy to the free minority electrons so that as they speed through the *p* region, they collide with atoms with enough energy to knock valence



◄ FIGURE 1–25

The extremely small reverse current in a reverse-biased diode is due to the minority carriers from thermally generated electron-hole pairs.

electrons out of orbit and into the conduction band. The newly created conduction electrons are also high in energy and repeat the process. If one electron knocks only two others out of their valence orbit during its travel through the *p* region, the numbers quickly multiply. As these high-energy electrons go through the depletion region, they have enough energy to go through the *n* region as conduction electrons, rather than combining with holes.

The multiplication of conduction electrons just discussed is known as **avalanche** and results in a very high reverse current that can damage the diode because of excessive heat dissipation.

SECTION 1–8 REVIEW

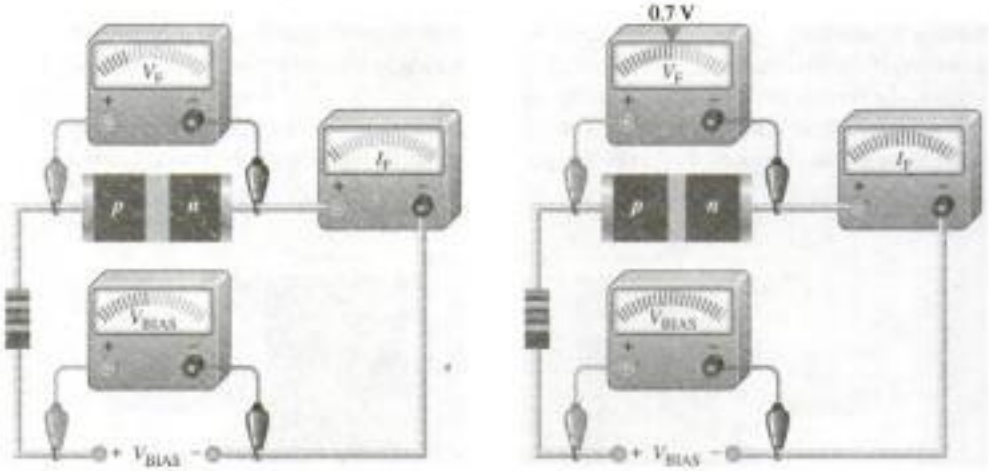
1. Describe forward bias of a diode.
2. Explain how to forward-bias a diode.
3. Describe reverse bias of a diode.
4. Explain how to reverse-bias a diode.
5. Compare the depletion regions in forward bias and reverse bias.
6. Which bias condition produces majority carrier current?
7. How is reverse current in a diode produced?
8. When does reverse breakdown occur in a diode?
9. Define *avalanche* as applied to diodes.

1–9 VOLTAGE-CURRENT CHARACTERISTIC OF A DIODE

Forward bias produces current through a diode and reverse bias essentially prevents current, except for a negligible reverse current. Reverse bias prevents current as long as the reverse-bias voltage does not equal or exceed the breakdown voltage of the junction.

V-I Characteristic for Forward Bias

When a forward-bias voltage is applied across a diode, there is current. This current is called the *forward current* and is designated I_F. Figure 1–26 illustrates what happens as the forward-bias voltage is increased positively from 0 V. The resistor is used to limit the forward current to a value that will not overheat the diode and cause damage.



(a) Small forward-bias voltage ($V_F < 0.7$ V), very small forward current.

(b) Forward voltage reaches and remains at approximately 0.7 V. Forward current continues to increase as the bias voltage is increased.

▲ FIGURE 1–26

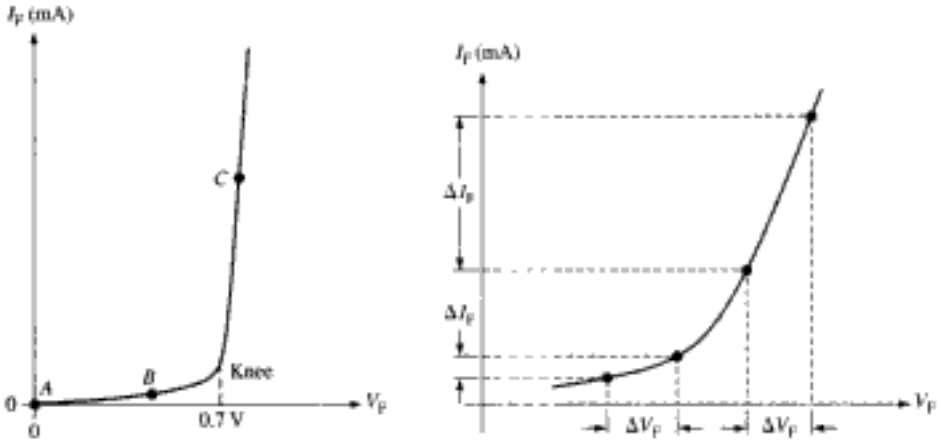
Forward-bias measurements show general changes in V_F and I_F as V_{BIAS} is increased.

With 0 V across the diode, there is no forward current. As you gradually increase the forward-bias voltage, the forward current *and* the voltage across the diode gradually increase, as shown in Figure 1–26(a). A portion of the forward-bias voltage is dropped across the limiting resistor. When the forward-bias voltage is increased to a value where the voltage across the diode reaches approximately 0.7 V (barrier potential), the forward current begins to increase rapidly, as illustrated in Figure 1–26(b).

As you continue to increase the forward-bias voltage, the current continues to increase very rapidly, but the voltage across the diode increases only gradually above 0.7 V. This small increase in the diode voltage above the barrier potential is due to the voltage drop across the internal dynamic resistance of the semiconductive material.

Graphing the V-I Curve If you plot the results of the type of measurements shown in Figure 1–26 on a graph, you get the ***V-I* characteristic** curve for a forward-biased diode, as shown in Figure 1–27(a). The diode forward voltage (V_F) increases to the right along the horizontal axis, and the forward current (I_F) increases upward along the vertical axis.

As you can see in Figure 1–27(a), the forward current increases very little until the forward voltage across the *pn* junction reaches approximately 0.7 V at the knee of the curve.



(a) *V-I* characteristic curve for forward bias.

(b) Expanded view of a portion of the curve in part (a). The dynamic resistance r'_d decreases as you move up the curve, as indicated by the decrease in the value of $\Delta V_F / \Delta I_F$.

◀ FIGURE 1–27

Relationship of voltage and current in a forward-biased diode.

After this point, the forward voltage remains at approximately 0.7 V, but I_F increases rapidly. As previously mentioned, there is a slight increase in V_F above 0.7 V as the current increases due mainly to the voltage drop across the dynamic resistance. *Normal operation for a forward-biased diode is above the knee of the curve.* The I_F scale is typically in mA, as indicated.

Three points *A*, *B*, and *C* are shown on the curve in Figure 1–27(a). Point *A* corresponds to a zero-bias condition. Point *B* corresponds to Figure 1–26(a) where the forward voltage is less than the barrier potential of 0.7 V. Point *C* corresponds to Figure 1–26(a) where the forward voltage *approximately* equals the barrier potential. As the external bias voltage and forward current continue to increase above the knee, the forward voltage will increase slightly above 0.7 V. In reality, the forward voltage can be as much as approximately 0.90 V, depending on the forward current.

Dynamic Resistance Figure 1–27(b) is an expanded view of the *V-I* characteristic curve in part (a) and illustrates dynamic resistance. Unlike a linear resistance, the resistance of the forward-biased diode is not constant over the entire curve. Because the resistance changes as you move along the *V-I* curve, it is called *dynamic* or *ac resistance*. Internal resistances of electronic devices are usually designated by lowercase italic *r* with a prime, instead of the standard *R*. The dynamic resistance of a diode is designated r'_d.

Below the knee of the curve the resistance is greatest because the current increases very little for a given change in voltage ($r'_d = \Delta V_F / \Delta I_F$). The resistance begins to decrease in the region of the knee of the curve and becomes smallest above the knee where there is a large change in current for a given change in voltage.

V-I Characteristic for Reverse Bias

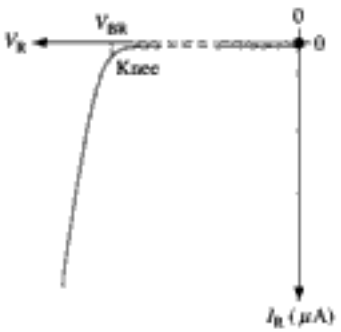
When a reverse-bias voltage is applied across a diode, there is only an extremely small reverse current (I_R) through the *pn* junction. With 0 V across the diode, there is no reverse current. As you gradually increase the reverse-bias voltage, there is a very small reverse current and the voltage across the diode increases. When the applied bias voltage is increased to a value where the reverse voltage across the diode (V_R) reaches the breakdown value (V_{BR}), the reverse current begins to increase rapidly.

As you continue to increase the bias voltage, the current continues to increase very rapidly, but the voltage across the diode increases very little above V_{BR}. *Breakdown, with exceptions, is not a normal mode of operation for most pn junction devices.*

Graphing the V-I Curve If you plot the results of reverse-bias measurements on a graph, you get the *V-I* characteristic curve for a reverse-biased diode. A typical curve is shown in Figure 1–28. The diode reverse voltage (V_R) increases to the left along the horizontal axis, and the reverse current (I_R) increases downward along the vertical axis.

▶ FIGURE 1–28

V-I characteristic curve for a reverse-biased diode.



There is very little reverse current (usually μA or nA) until the reverse voltage across the diode reaches approximately the breakdown value (V_{BR}) at the knee of the curve. After this point, the reverse voltage remains at approximately V_{BR}, but I_R increases very rapidly, resulting in overheating and possible damage. The breakdown voltage for a typical silicon diode can vary, but a minimum value of 50 V is not unusual.

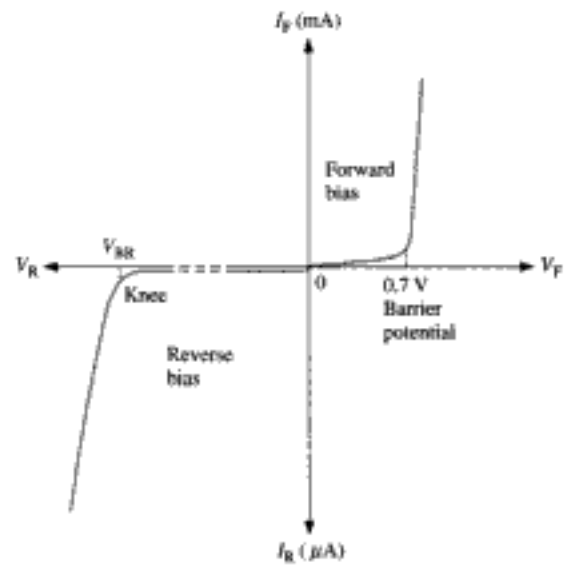
The Complete *V-I* Characteristic Curve

Combine the curves for both forward bias and reverse bias, and you have the complete *V-I* characteristic curve for a diode, as shown in Figure 1–29. Notice that the I_F scale is in mA compared to the I_R scale in μA.

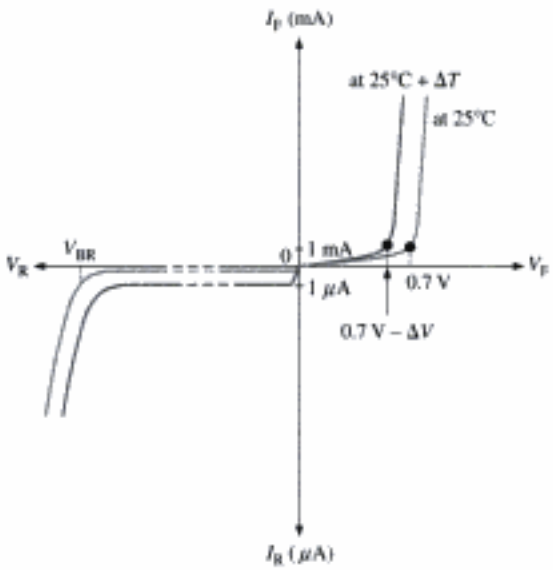
Temperature Effects For a forward-biased diode, as temperature is increased, the forward current increases for a given value of forward voltage. Also, for a given value of forward current, the forward voltage decreases. This is shown with the *V-I* characteristic curves in Figure 1–30. The gray curve is at room temperature (25°C) and the black curve is at an elevated temperature (25°C + ΔT). Notice that the barrier potential decreases as temperature increases.

▶ FIGURE 1–29

The complete *V-I* characteristic curve for a diode.



For a reverse-biased diode, as temperature is increased, the reverse current increases. The difference in the two curves is exaggerated on the graph in Figure 1–30 for illustration. Keep in mind that the reverse current below breakdown remains extremely small and can usually be neglected.



◀ FIGURE 1–30

Temperature effect on the diode *V-I* characteristic. The 1 mA and 1 μA marks on the vertical axis are given as a basis for a relative comparison of the current scales.

SECTION 1–9 REVIEW

1. Discuss the significance of the knee of the characteristic curve in forward bias.
2. On what part of the curve is a forward-biased diode normally operated?
3. Which is greater, the breakdown voltage or the barrier potential?
4. On what part of the curve is a reverse-biased diode normally operated?
5. What happens to the barrier potential when the temperature increases?

1–10 DIODE MODELS

You have learned that a diode is a *pn* junction device. In this section, you will learn the electrical symbol for a diode and how the diode can be modeled for circuit analysis using three levels of complexity. Also, diode packaging and terminal identification are introduced. (See Fig 1-31)

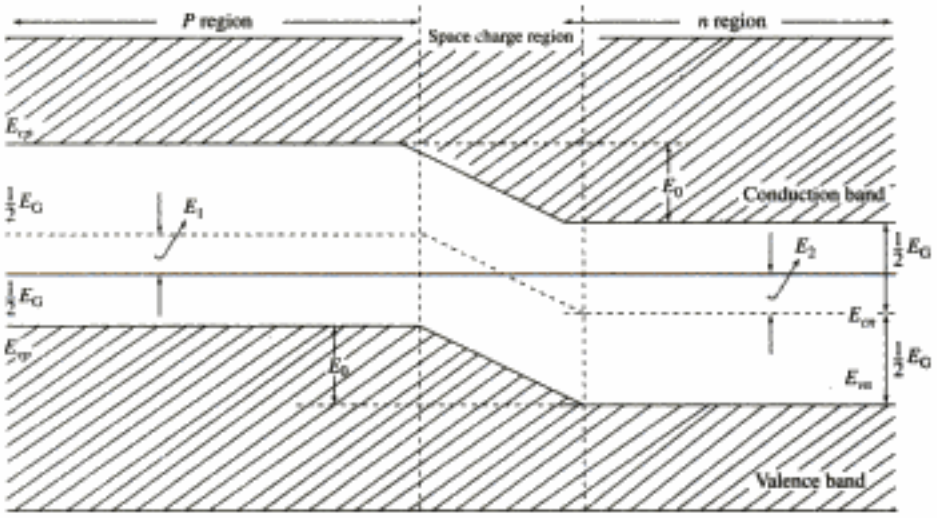
Diode Structure and Symbol

A diode is a single *pn* junction device with conductive contacts and wire leads connected to each region, as shown in Figure 1–32(a). Part of the diode is an *n*-type semiconductor and the other part is a *p*-type semiconductor.

There are several types of diodes, but the schematic symbol for a general-purpose or rectifier diode, such as introduced in this chapter, is shown in Figure 1–32(b). The *n* region is called the **cathode** and the *p* region is called the **anode**. The "arrow" in the symbol points in the direction of conventional current (opposite to electron flow).

▶ **FIGURE 1–31**

Energy band structure of an open circuit *pn* junction diode.



▶ **FIGURE 1–32**

Diode structure and schematic symbol.

(a) Basic diode structure

(b) Schematic symbol

Forward-Bias Connection A diode is forward-biased when a voltage source is connected as shown in Figure 1–33(a). The positive terminal of the source is connected to the anode through a current-limiting resistor. The negative terminal of the source is connected to the cathode. The forward current (I_F) is from anode to cathode as indicated. The forward voltage drop (V_F) due to the barrier potential is from positive at the anode to negative at the cathode.

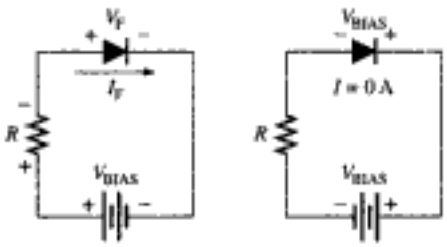
Reverse-Bias Connection A diode is reverse-biased when a voltage source is connected as shown in Figure 1–33(b). The negative terminal of the source is connected to the anode side of the circuit, and the positive terminal is connected to the cathode side. A resistor is not necessary in reverse bias but it is shown for circuit consistency. The reverse current is extremely small and can be considered to be zero. Notice that the entire bias voltage (V_{BIAS}) appears across the diode.

The Ideal Diode Model

The ideal model of a diode is a simple switch. When the diode is forward-biased, it acts like a closed (on) switch, as shown in Figure 1–34(a). When the diode is reverse-biased, it acts like an open (off) switch, as shown in part (b). The barrier potential, the forward dynamic resistance, and the reverse current are all neglected.

In Figure 1–34(c), the ideal *V-I* characteristic curve graphically depicts the ideal diode operation. Since the barrier potential and the forward dynamic resistance are neglected, the diode is assumed to have a zero voltage across it when forward-biased, as indicated by the portion of the curve on the positive vertical axis.

$$V_F = 0\text{ V}$$



(a) Forward bias (b) Reverse bias

◄ FIGURE 1–33

Forward-bias and reverse-bias connections showing the diode symbol.

The forward current is determined by the bias voltage and the limiting resistor using Ohm's law.

$$I_F = \frac{V_{BIAS}}{R_{LIMIT}}$$

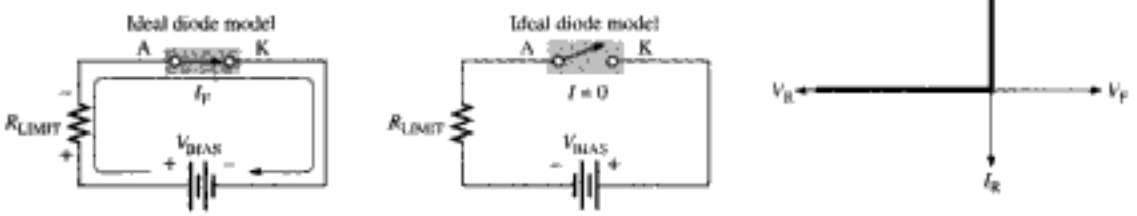
Equation 1–2

Since the reverse current is neglected, its value is assumed to be zero, as indicated in Figure 1–34(c) by the portion of the curve on the negative horizontal axis.

$$I_R = 0\text{ A}$$

The reverse voltage equals the bias voltage.

$$V_R = V_{BIAS}$$



(a) Forward bias (b) Reverse bias (c) Ideal characteristic curve (black)

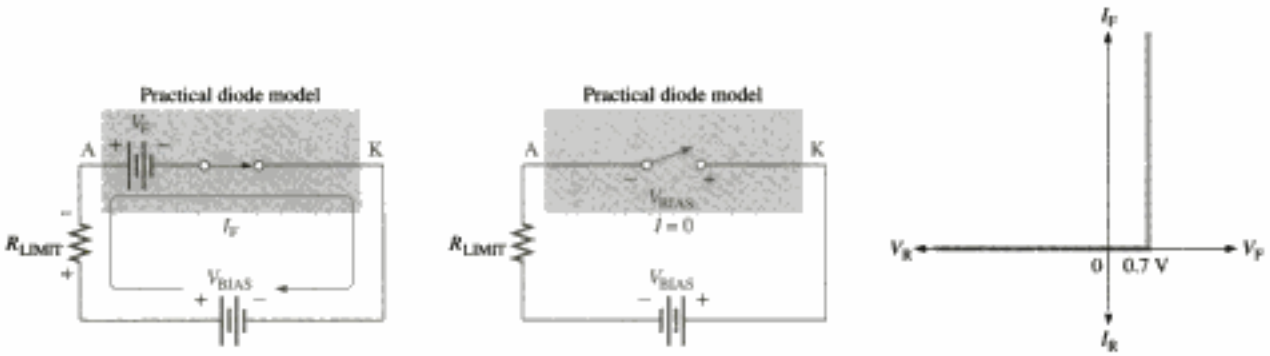
▲ FIGURE 1–34

The ideal model of a diode.

You may want to use the ideal model when you are troubleshooting or trying to figure out the operation of a circuit and are not concerned with more exact values of voltage or current.

The Practical Diode Model

The practical model adds the barrier potential to the ideal switch model. When the diode is forward-biased, it is equivalent to a closed switch in series with a small equivalent voltage source equal to the barrier potential (0.7 V) with the positive side toward the anode, as indicated in Figure 1–35(a). This equivalent voltage source represents the fixed voltage drop (V_T) produced across the forward-biased *pn* junction of the diode and is not an active source of voltage.



(a) Forward bias (b) Reverse bias (c) Characteristic curve (silicon)

▲ FIGURE 1–35

The practical model of a diode.

When the diode is reverse-biased, it is equivalent to an open switch just as in the ideal model, as shown in Figure 1–35(b). The barrier potential does not affect reverse bias, so it is not a factor.

The characteristic curve for the practical diode model is shown in Figure 1–35(c). Since the barrier potential is included and the dynamic resistance is neglected, the diode is assumed to have a voltage across it when forward-biased, as indicated by the portion of the curve to the right of the origin.

$$V_F = 0.7\text{ V}$$

The forward current is determined as follows by first applying Kirchhoff's voltage law to Figure 1–35(a):

$$V_{BIAS} - V_F - V_{R_{LIMIT}} = 0$$

$$V_{R_{LIMIT}} = I_F R_{LIMIT}$$

Substituting and solving for I_F,

Equation 1–3

$$I_F = \frac{V_{BIAS} - V_F}{R_{LIMIT}}$$

The diode is assumed to have zero reverse current, as indicated by the portion of the curve on the negative horizontal axis.

$$I_R = 0\text{ A}$$

$$V_R = V_{BIAS}$$

The Complete Diode Model

The complete model of a diode consists of the barrier potential, the small forward dynamic resistance (r'_d), and the large internal reverse resistance (r'_R). The reverse resistance is taken into account because it provides a path for the reverse current, which is included in this diode model.

When the diode is forward-biased, it acts as a closed switch in series with the barrier potential voltage and the small forward dynamic resistance (r'_d), as indicated in Figure 1–36(a). When the diode is reverse-biased, it acts as an open switch in parallel with the large internal reverse resistance (r'_R), as shown in Figure 1–36(b). The barrier potential does not affect reverse bias, so it is not a factor.

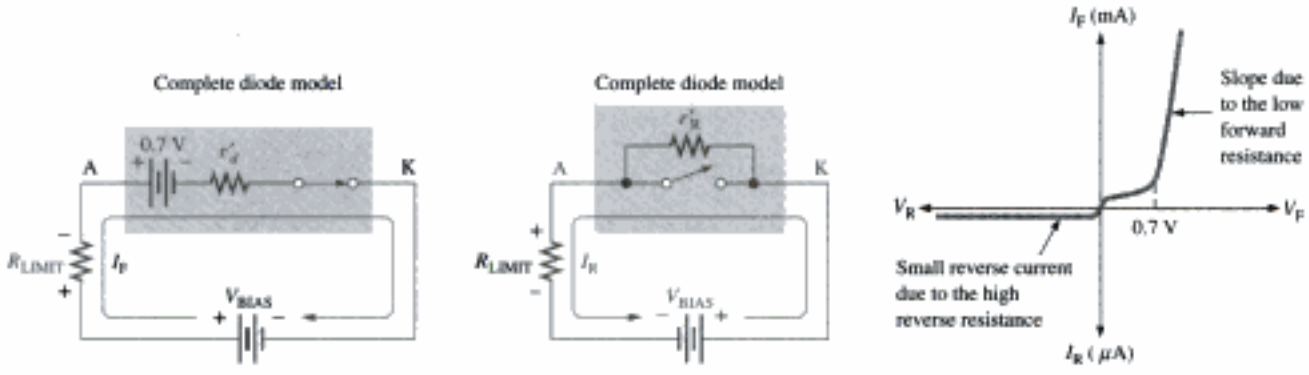
The characteristic curve for the complete diode model is shown in Figure 1–36(c). Since the barrier potential and the forward dynamic resistance are included, the diode is assumed to have a voltage across it when forward-biased. This voltage (V_F) consists of the barrier potential voltage plus the small voltage drop across the dynamic resistance, as indicated by the portion of the curve to the right of the origin. The curve slopes because the voltage drop due to dynamic resistance increases as the current increases. For the complete model of a silicon diode, the following formulas apply:

$$V_F = 0.7\text{ V} + I_F r'_d \qquad \textbf{Equation 1–4}$$

$$I_F = \frac{V_{BIAS} - 0.7\text{ V}}{R_{LIMIT} + r'_d} \qquad \textbf{Equation 1–5}$$

The reverse current is taken into account with the parallel resistance and is indicated by the portion of the curve to the left of the origin. The breakdown portion of the curve is not shown because breakdown is not a normal mode of operation for most diodes.

Although the ideal and practical models are predominately used in this textbook, the following example illustrates the differences in all three diode models in the analysis of a simple circuit.



(a) Forward bias (b) Reverse bias (c) Characteristic curve (silicon)

▲ FIGURE 1–36

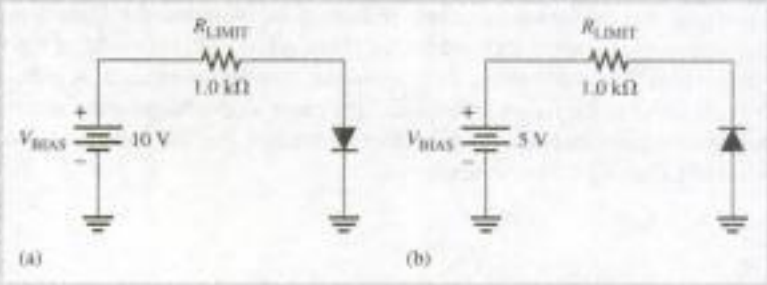
The complete model of a diode.

EXAMPLE 1–1

(a) Determine the forward voltage and forward current for the diode in Figure 1–37(a) for each of the diode models. Also find the voltage across the limiting resistor in each case. Assume $r'_d = 10\ \Omega$ at the determined value of forward current.

(b) Determine the reverse voltage and reverse current for the diode in Figure 1–37(b) for each of the diode models. Also find the voltage across the limiting resistor in each case. Assume $I_R = 1\ \mu$A.

► FIGURE 1–37



Solution (a) Ideal model:

$$V_F = \mathbf{0\ V}$$

$$I_F = \frac{V_{BIAS}}{R_{LIMIT}} = \frac{10\ V}{1.0\ k\Omega} = \mathbf{10\ mA}$$

$$V_{R_{LIMIT}} = I_F R_{LIMIT} = (10\ mA)(1.0\ k\Omega) = \mathbf{10\ V}$$

Practical model:

$$V_F = \mathbf{0.7\ V}$$

$$I_F = \frac{V_{BIAS} - V_F}{R_{LIMIT}} = \frac{10\ V - 0.7\ V}{1.0\ k\Omega} = \frac{9.3\ V}{1.0\ k\Omega} = \mathbf{9.3\ mA}$$

$$V_{R_{LIMIT}} = I_F R_{LIMIT} = (9.3\ mA)(1.0\ k\Omega) = \mathbf{9.3\ V}$$

Complete model:

$$I_F = \frac{V_{BIAS} - 0.7\ V}{R_{LIMIT} + r'_d} = \frac{10\ V - 0.7\ V}{1.0\ k\Omega + 10\ \Omega} = \frac{9.3\ V}{1010\ \Omega} = \mathbf{9.21\ mA}$$

$$V_F = 0.7\ V + I_F r'_d = 0.7\ V + (9.21\ mA)(10\ \Omega) = \mathbf{792\ mV}$$

$$V_{R_{LIMIT}} = I_F R_{LIMIT} = (9.21\ mA)(1.0\ k\Omega) = \mathbf{9.21\ V}$$

$$I_R = \mathbf{0\ A}$$

$$V_R = V_{BIAS} = \mathbf{5\ V}$$

$$V_{R_{LIMIT}} = \mathbf{0\ V}$$

Practical model:

$$I_R = \mathbf{0\ A}$$

$$V_R = V_{BIAS} = \mathbf{5\ V}$$

$$V_{R_{LIMIT}} = \mathbf{0\ V}$$

Complete model:

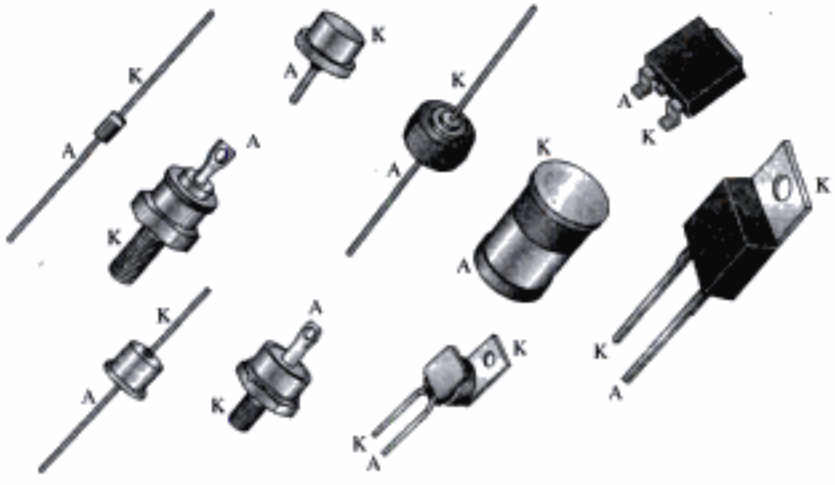
$$I_R = \mathbf{1\ \mu A}$$

$$V_{R_{LIMIT}} = I_R R_{LIMIT} = (1\ \mu A)(1.0\ k\Omega) = \mathbf{1\ mV}$$

$$V_R = V_{BIAS} - V_{R_{LIMIT}} = 5\ V - 1\ mV = \mathbf{4.999\ V}$$

Typical Diodes

Several common physical configurations of diodes are illustrated in Figure 1–38. The anode and cathode are indicated on a diode in several ways, depending on the type of package. The cathode is usually marked by a band, a tab, or some other feature. On those packages where one lead is connected to the case, the case is the cathode. Always check the data sheet, which will be introduced in Chapter 2, for the pin configuration if there is uncertainty.



◀ **FIGURE 1–38**

Typical diode **packages with terminal** identification.

SECTION 1–10 REVIEW

1. What are the two conditions under which the diode is operated?
2. Under what condition is the diode never intentionally operated?
3. What is the simplest way to visualize a diode?
4. To more accurately represent a diode, what factors must be included?
5. Which diode models will be used in this book?

1–11 TESTING A DIODE

A multimeter can be used as a fast and simple way to check a diode. A good diode will show an extremely high resistance (ideally an open) with reverse bias and a very low resistance with forward bias. A defective open diode will show an extremely high resistance (or open) for both forward and reverse bias. A defective shorted or resistive diode will show zero or a low resistance for both forward and reverse bias. An open diode is the most common type of failure.

▶ FIGURE 1–39

DMM diode test on a properly functioning diode.

(a) Forward-bias test (b) Reverse-bias test

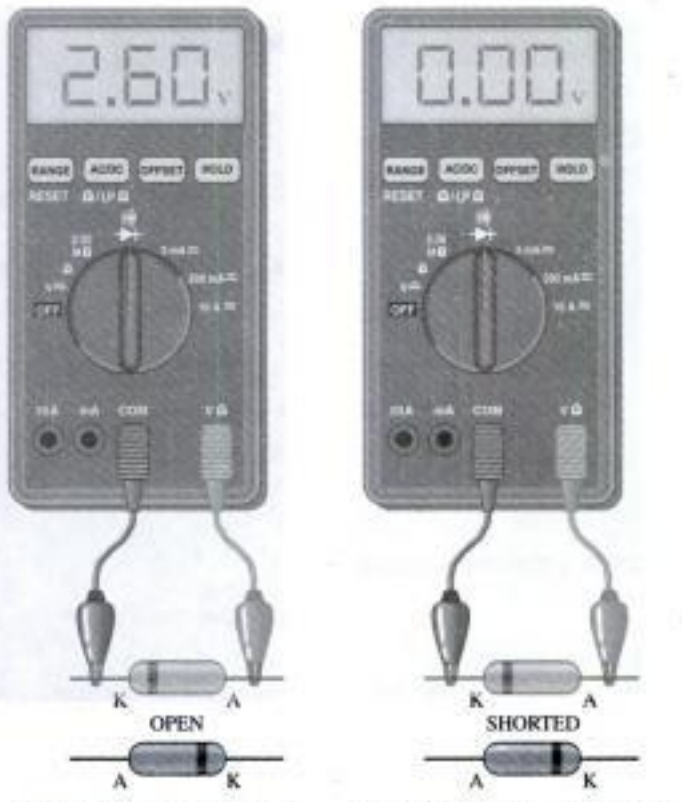
The DMM Diode Test Position Many digital multimeters (DMMs) have a diode test position that provides a convenient way to test a diode. A typical DMM, as shown in Figure 1–39, has a small diode symbol to mark the position of the function switch. When set to *diode test*, the meter provides an internal voltage sufficient to forward-bias and reverse-bias a diode. This internal voltage may vary among different makes of DMM, but 2.5 V to 3.5 V is a typical range of values. The meter provides a voltage reading or other indication to show the condition of the diode under test.

When the Diode Is Working In Figure 1–39(a), the gray (positive) lead of the meter is connected to the anode and the black (negative) lead is connected to the cathode to forward-bias the diode. If the diode is good, you will get a reading of between approximately 0.5 V and 0.9 V, with 0.7 V being typical for forward bias.

In Figure 1–39(b), the diode is turned around to reverse-bias the diode as shown. If the diode is working properly, you will get a voltage reading based on the meter's internal voltage source. The 2.6 V shown in the figure represents a typical value and indicates that the diode has an extremely high reverse resistance with essentially all of the internal voltage appearing across it.

When the Diode Is Defective When a diode has failed open, you get an open circuit voltage reading (2.6 V is typical) or "OL" indication for both the forward-bias and the reverse-bias condition, as illustrated in Figure 1–40(a). If a diode is shorted, the meter reads 0 V in both forward- and reverse-bias tests, as indicated in part (b). Sometimes, a failed diode may exhibit a small resistance for both bias conditions rather than a pure short. In this case, the meter will show a small voltage much less than the correct open voltage. For example, a resistive diode may result in a reading of 1.1 V in both directions rather than the correct readings of 0.7 V for forward bias and 2.6 V for reverse bias.

Checking a Diode with the OHMs Function DMMs that do not have a diode test position can be used to check a diode by setting the function switch on an OHMs range. For a



(a) Forward- and reverse-bias tests for an open diode give the same indication. Some meters will display OL.

(b) Forward- and reverse-bias tests for a shorted diode give the same 0 V reading. If the diode is resistive, the reading is less than 2.6 V.

◀ **FIGURE 1–40**
Testing a defective diode.

forward-bias check of a good diode, you will get a resistance reading that can vary depending on the meter's internal battery. Many meters do not have sufficient voltage on the OHMs setting to fully forward-bias a diode and you may get a reading of from several hundred to several thousand ohms. For the reverse-bias check of a good diode, you will get some type of out-of-range indication such as "OL" on most DMMs because the reverse resistance is too high for the meter to measure.

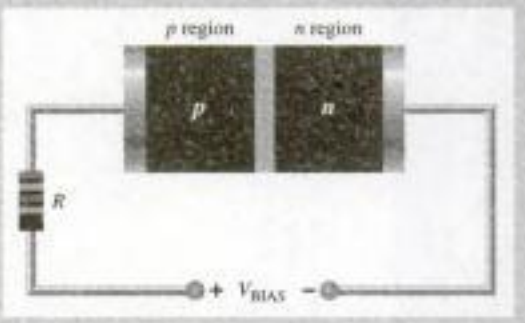
Even though you may not get accurate forward- and reverse-resistance readings on a DMM, the relative readings indicate that a diode is functioning properly, and that is usually all you need to know. The out-of-range indication shows that the reverse resistance is extremely high, as you expect. The reading of a few hundred to a few thousand ohms for forward bias is relatively small compared to the reverse resistance, indicating that the diode is working properly. The actual resistance of a forward-biased diode is typically much less than 100 Ω.

SECTION 1–11 REVIEW

1. A properly functioning diode will produce a reading in what range when forward-biased?
2. What reading might a DMM produce when a diode is reverse-biased?

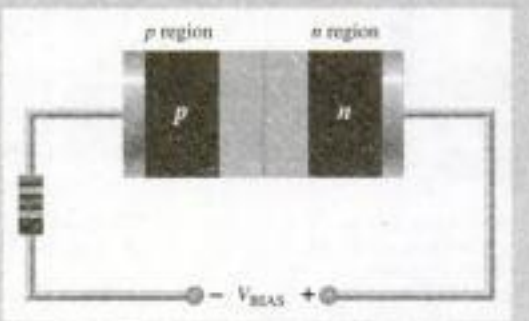
SUMMARY OF DIODE BIAS

FORWARD BIAS: PERMITS MAJORITY-CARRIER CURRENT



- Bias voltage connections: positive to *p* region; negative to *n* region.
- The bias voltage must be greater than the barrier potential.
- Barrier potential: 0.7 V for silicon.
- Majority carriers flow toward the *pn* junction.
- Majority carriers provide the forward current.
- The depletion region narrows.

REVERSE BIAS: PREVENTS MAJORITY-CARRIER CURRENT



- Bias voltage connections: positive to *n* region; negative to *p* region.
- The bias voltage must be less than the breakdown voltage.
- Majority carriers flow away from the *pn* junction during short transition time.
- Minority carriers provide the extremely small reverse current.
- There is no majority carrier current after transition time.
- The depletion region widens.

CHAPTER SUMMARY

- According to the classical Bohr model, the atom is viewed as having a planetary-type structure with electrons orbiting at various distances around the central nucleus.
- The nucleus of an atom consists of protons and neutrons. The protons have a positive charge and the neutrons are uncharged. The number of protons is the atomic number of the atom.
- Electrons have a negative charge and orbit around the nucleus at distances that depend on their energy level. An atom has discrete bands of energy called *shells* in which the electrons orbit. Atomic structure allows a certain maximum number of electrons in each shell. In their natural state, all atoms are neutral because they have an equal number of protons and electrons.
- The outermost shell or band of an atom is called the *valence band*, and electrons that orbit in this band are called *valence electrons*. These electrons have the highest energy of all those in the atom. If a valence electron acquires enough energy from an outside source such as heat, it can jump out of the valence band and break away from its atom.
- Semiconductor atoms have four valence electrons. Silicon is the most widely used semiconductive material.
- Materials that are conductors have a large number of free electrons and conduct current very well. Insulating materials have very few free electrons and do not conduct current at all under normal circumstances. Semiconductive materials fall in between conductors and insulators in their ability to conduct current.
- Semiconductor atoms bond together in a symmetrical pattern to form a solid material called a *crystal*. The bonds that hold a crystal together are called *covalent bonds*. Within the crystal structure, the valence electrons that manage to escape from their parent atom are called *conduction electrons* or *free electrons*. They have more energy than the electrons in the valence band and are free to drift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36. When a diode is forward-biased,
(a) the only current is hole current **(b)** the only current is electron current
(c) the only current is produced by majority carriers
(d) the current is produced by both holes and electrons

37. Although current is blocked in reverse bias,
(a) there is some current due to majority carriers
(b) there is a very small current due to minority carriers
(c) there is an avalanche current

38. For a silicon diode, the value of the forward-bias voltage typically
(a) must be greater than 0.3 V **(b)** must be greater than 0.7 V
(c) depends on the width of the depletion region
(d) depends on the concentration of majority carriers

39. When forward-biased, a diode
(a) blocks current **(b)** conducts current
(c) has a high resistance **(d)** drops a large voltage

40. When a voltmeter is placed across a forward-biased diode, it will read a voltage approximately equal to
(a) the bias battery voltage **(b)** 0 V
(c) the diode barrier potential **(d)** the total circuit voltage

41. A silicon diode is in series with a 1.0 kΩ resistor and a 5 V battery. If the anode is connected to the positive battery terminal, the cathode voltage with respect to the negative battery terminal is
(a) 0.7 V **(b)** 0.3 V **(c)** 5.7 V **(d)** 4.3 V

42. The positive lead of an ohmmeter is connected to the anode of a diode and the negative lead is connected to the cathode. The diode is
(a) reversed-biased **(b)** open **(c)** forward-biased
(d) faulty **(e)** answers (b) and (d)

PROBLEMS

Answers to selected problems are at the end of the book.

BASIC PROBLEMS

SECTION 1–1 Atomic Structure

1. If the atomic number of a neutral atom is 6, how many electrons does the atom have? How many protons?

2. What is the maximum number of electrons that can exist in the 3rd shell of an atom?

SECTION 1–2 Classification of Matter on the Basis of Semiconductor Theory

3. For each of the energy diagrams in Figure 1–41, determine the class of material based on relative comparisons.

4. A certain atom has four valence electrons. What type of atom is it?

SECTION 1–3 Covalent Bonds

5. In a silicon crystal, how many covalent bonds does a single atom form?

SECTION 1–4 Conduction in Semiconductors

6. What happens when heat is added to silicon?

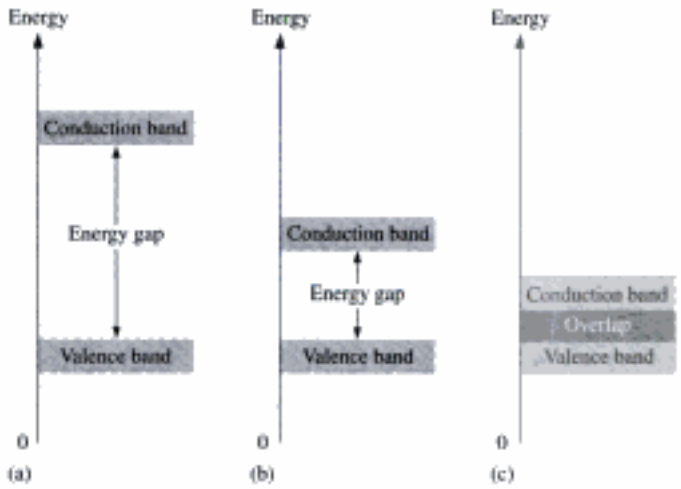
7. Name the two energy bands at which current is produced in silicon.

SECTION 1–5 Electrical Properties of Semiconductors and the Hall Effect

SECTION 1–6 *N*-Type and *P*-Type Semiconductors

8. Describe the process of doping and explain how it alters the atomic structure of silicon.

9. What is antimony? What is boron?



◀ **FIGURE 1–41**

SECTION 1–7 The Diode

10. How is the electric field across the *pn* junction created?

11. Because of its barrier potential, can a diode be used as a voltage source? Explain.

SECTION 1–8 Biasing a Diode

12. To forward-bias a diode, to which region must the positive terminal of a voltage source be connected?

13. Explain why a series resistor is necessary when a diode is forward-biased.

SECTION 1–9 Voltage-Current Characteristic of a Diode

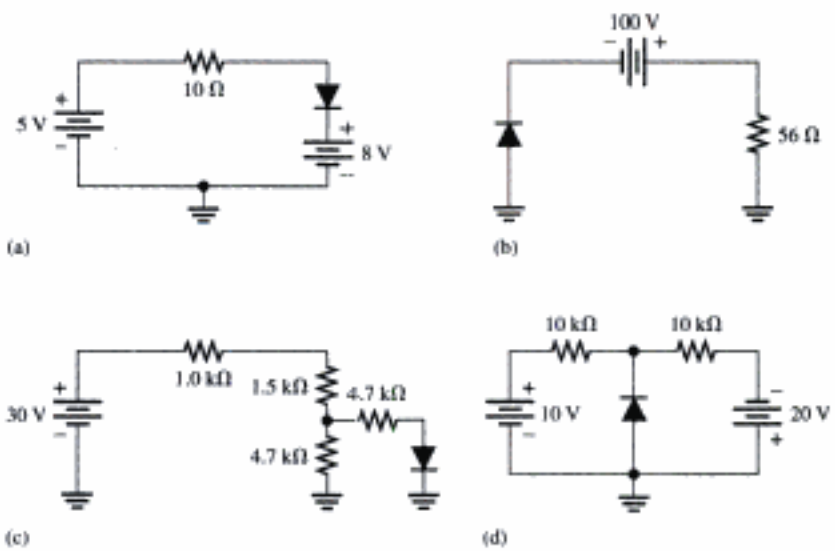
14. Explain how to generate the forward-bias portion of the characteristic curve.

15. What would cause the barrier potential to decrease from 0.7 V to 0.6 V?

SECTION 1–10 Diode Models

16. Determine whether each diode in Figure 1–42 is forward-biased or reverse-biased.

17. Determine the voltage across each diode in Figure 1–42, assuming the practical model.



◀ **FIGURE 1–42**

Multisim file circuits are identified with a CD logo and are in the Problems folder on your CD-ROM. Filenames correspond to figure numbers (e.g., F01–42).

ANSWERS

SECTION REVIEWS

SECTION 1–1 Atomic Structure

1. An atom is the smallest particle of an element that retains the characteristics of that element.
2. An electron is the basic particle of negative electrical charge.
3. A valence electron is an electron in the outermost shell of an atom.
4. A free electron is one that has acquired enough energy to break away from the valence band of the parent atom.
5. When a neutral atom loses an electron, the atom becomes a positive ion. When a neutral atom gains an electron, the atom becomes a negative ion.

SECTION 1–2 Classification of Matter on the Basis of Semiconductor Theory

1. Conductors have many free electrons and easily conduct current. Insulators have essentially no free electrons and do not conduct current.
2. Semiconductors do not conduct current as well as conductors do. In terms of conductivity, they are between conductors and insulators.
3. Conductors such as copper have one valence electron.
4. Semiconductors have four valence electrons.
5. Gold, silver, and copper are the best conductors.
6. Silicon is the most widely used semiconductor.
7. The valence electrons of a semiconductor are more tightly bound to the atom than those of conductors.

SECTION 1–3 Covalent Bonds

1. Covalent bonds are formed by the sharing of valence electrons with neighboring atoms.
2. An intrinsic material is one that is in a pure state.
3. A crystal is a solid material formed by atoms bonding together in a fixed pattern.
4. There are eight shared valence electrons in each atom of a silicon crystal.

SECTION 1–4 Conduction in Semiconductors

1. Free electrons are in the conduction band.
2. Free (conduction) electrons are responsible for current in a material.
3. A hole is the absence of an electron in the valence band.
4. Hole current occurs at the valence level.

SECTION 1–5 Electrical Properties of Semiconductors and the Hall Effect

SECTION 1–6 *N*-Type and *P*-Type Semiconductors

1. Doping is the process of adding impurity atoms to a semiconductor in order to modify its conductive properties.
2. A pentavalent atom (donor) has five valence electrons and a trivalent atom (acceptor) has three valence electrons.
3. An *n*-type material is formed by the addition of pentavalent impurity atoms to the intrinsic semiconductive material.
4. A *p*-type material is formed by the addition of trivalent impurity atoms to the intrinsic semiconductive material.
5. The majority carrier in an *n*-type semiconductor is the free electron.
6. The majority carrier in a *p*-type semiconductor is the hole.

7. Majority carriers are produced by doping.
8. Minority carriers are thermally produced when electron-hole pairs are generated.
9. A pure semiconductor is intrinsic. A doped (impure) semiconductor is extrinsic.

SECTION 1–7 The Diode

1. A *pn* junction is the boundary between *p*-type and *n*-type semiconductors in a diode.
2. Diffusion is the movement of the free electrons (majority carriers) in the *n*-region across the *pn* junction and into the *p* region.
3. The depletion region is the thin layers of positive and negative ions that exist on both sides of the *pn* junction.
4. The barrier potential is the potential difference of the electric field in the depletion region and is the amount of energy required to move electrons through the depletion region.
5. The barrier potential for a silicon diode is approximately 0.7 V.
6. The barrier potential for a germanium diode is approximately 0.3 V.

SECTION 1–8 Biasing a Diode

1. When forward-biased, a diode conducts current. The free electrons in the *n* region move across the *pn* junction and combine with the holes in the *p* region.
2. To forward-bias a diode, the positive side of an external bias voltage is applied to the *p* region and the negative side to the *n* region.
3. When reverse-biased, a diode does not conduct current except for an extremely small reverse current.
4. To reverse-bias a diode, the positive side of an external bias voltage is applied to the *n* region and the negative side to the *p* region.
5. The depletion region for forward bias is much narrower than for reverse bias.
6. Majority carrier current is produced by forward bias.
7. Reverse current is produced by the minority carriers.
8. Reverse breakdown occurs when the reverse-bias voltage equals or exceeds the breakdown voltage of the *pn* junction of a diode.
9. Avalanche is the rapid multiplication of current carriers in reverse breakdown.

SECTION 1–9 Voltage-Current Characteristic of a Diode

1. The knee of the characteristic curve in forward bias is the point at which the barrier potential is overcome and the current increases drastically.
2. A forward-biased diode is normally operated above the knee of the curve.
3. Breakdown voltage is always much greater than the barrier potential.
4. A reverse-biased diode is operated below the breakdown point on the knee of the curve.
5. Barrier potential decreases as temperature increases.

SECTION 1–10 Diode Models

1. The diode is operated in forward bias and reverse bias.
2. The diode should never be operated in reverse breakdown.
3. The diode can be ideally viewed as a switch.
4. A diode includes barrier potential, dynamic resistance, and reverse resistance in the complete model.
5. The ideal and practical diode models (barrier potential) are used.

SECTION 1–11 Testing a Diode

1. 0.5 V to 0.9 V
2. 2.60 V

OBJECTIVE-TYPE QUESTIONS

1. (a)	**2.** (c)	**3.** (c)	**4.** (a)	**5.** (a)	**6.** (c)	**7.** (b)	**8.** (a)	**9.** (c)
10. (d)	**11.** (a)	**12.** (d)	**13.** (d)	**14.** (d)	**15.** (b)	**16.** (a)	**17.** (d)	**18.** (c)
19. (b)	**20.** (a)	**21.** (d)	**22.** (c)	**23.** (d)	**24.** (e)	**25.** (d)	**26.** (a)	**27.** (b)
28. (c)	**29.** (c)	**30.** (a)	**31.** (c)	**32.** (d)	**33.** (d)	**34.** (c)	**35.** (d)	**36.** (d)
37. (b)	**38.** (b)	**39.** (b)	**40.** (c)	**41.** (d)	**42.** (c)			

2

DIODE APPLICATIONS

CHAPTER OUTLINE

INTRODUCTION

The importance of the diode in electronic circuits cannot be overemphasized. Its ability to conduct current in one direction while blocking current in the other direction is essential to the operation of many types of circuits. One circuit in particular is the ac rectifier, which is covered in this chapter. Other important applications are circuits such as diode limiters, diode clampers, and diode voltage multipliers. A data sheet is discussed for specific diodes.

2–1 HALF-WAVE RECTIFIERS

Because of their ability to conduct current in one direction and block current in the other direction, diodes are used in circuits called rectifiers that convert ac voltage into dc voltage. Rectifiers are found in all dc power supplies that operate from an ac voltage source.

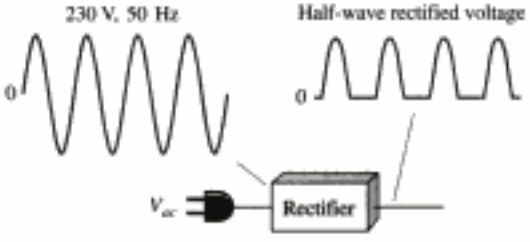
The Basic DC Power Supply

The dc **power supply** converts the standard 230 V, 50 Hz ac available at wall outlets into a constant dc voltage. The dc voltage produced by a power supply is used to power all types of electronic circuits, such as television receivers, stereo systems, VCRs, CD players, and most laboratory equipment.

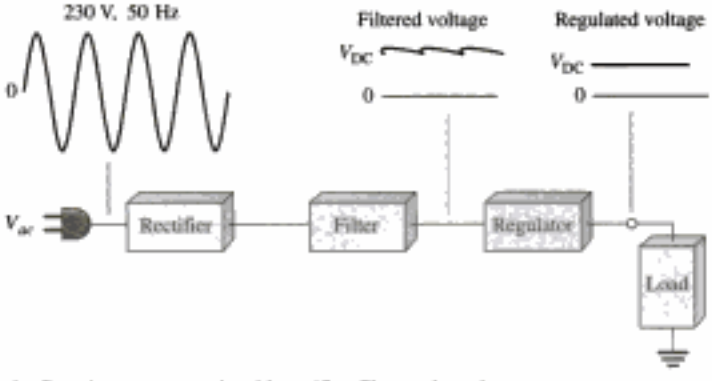
Basic block diagrams for a rectifier and complete power supply are shown in Figure 2–1. The **rectifier** can be either a half-wave rectifier or a full-wave rectifier. The rectifier converts the ac input voltage to a pulsating dc voltage, which is half-wave rectified as shown in Figure 2–1(a). A block diagram for a complete power supply is shown in part (b). The **filter** eliminates the fluctuations in the rectified voltage and produces a relatively smooth dc voltage. The **regulator** is a circuit that maintains a constant dc voltage for variations in the input line voltage or in the load. Regulators vary from a single device to more complex integrated circuits. The load is a circuit or device for which the power supply is producing the dc voltage and load current.

▶ FIGURE 2–1

Block diagram of a rectifier and a dc power supply with a load.



(a) Half-wave rectifier



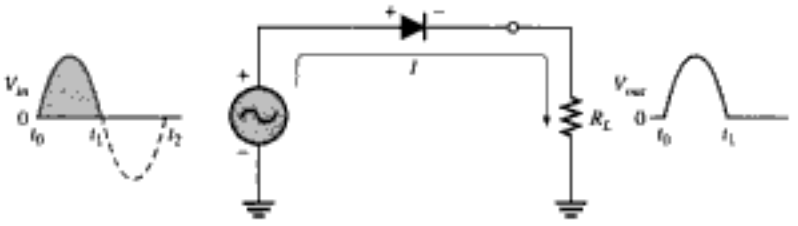
(b) Complete power supply with rectifier, filter, and regulator

The Half-Wave Rectifier

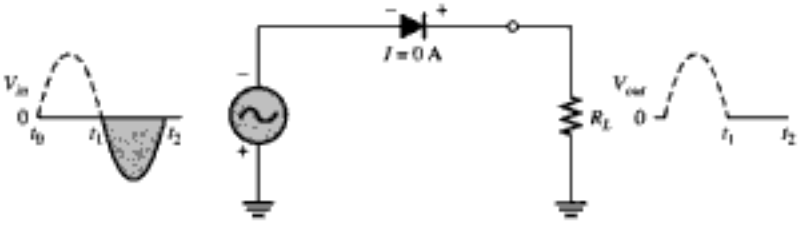
Figure 2–2 illustrates the process called *half-wave rectification*. A diode is connected to an ac source and to a load resistor, R_L, forming a **half-wave rectifier**. Let's examine what happens during one cycle of the input voltage using the ideal model for the diode.

When the sinusoidal input voltage (V_{in}) goes positive, the diode is forward-biased and conducts current through the load resistor, as shown in part (a). The current produces an output voltage across the load R_L, which has the same shape as the positive half-cycle of the input voltage.

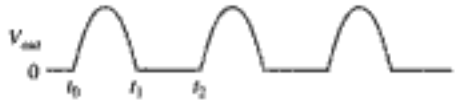
When the input voltage goes negative during the second half of its cycle, the diode is reverse-biased. There is no current, so the voltage across the load resistor is 0 V, as shown in Figure 2–2(b). The net result is that only the positive half-cycles of the ac input voltage appear across the load. Since the output does not change polarity, it is a pulsating dc voltage with a frequency of 50 Hz, as shown in part (c).



(a) During the positive alternation of the 50 Hz input voltage, the output voltage looks like the positive half of the input voltage.



(b) During the negative alternation of the input voltage, the current is 0, so the output voltage is also 0.



(c) 50 Hz half-wave output voltage for three input cycles

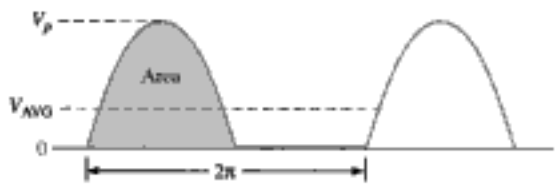
◀ **FIGURE 2–2**

Half-wave rectifier operation. The diode is considered to be ideal.

Average Value of the Half-Wave Output Voltage The average value of the half-wave rectified output voltage is the value you would measure on a dc voltmeter. Mathematically, it is determined by finding the area under the curve over a full cycle, as illustrated in Figure 2–3, and then dividing by 2π, the number of radians in a full cycle. The result of this is expressed in Equation 2–1, where V_p is the peak value of the voltage. This equation shows that V_{AVG} is approximately 31.8% of V_p for a half-wave rectified voltage.

$$V_{AVG} = \frac{V_p}{\pi}$$

Equation 2–1



◀ **FIGURE 2–3**

Average value of the half-wave rectified signal.

EXAMPLE 2–1

What is the average value of the half-wave rectified voltage in Figure 2–4?

▲ FIGURE 2–4

Solution

$$V_{AVG} = \frac{V_p}{\pi} = \frac{50\text{ V}}{\pi} = 15.9\text{ V}$$

Notice that V_{AVG} is 31.8% of V_p.

Effect of the Barrier Potential on the Half-Wave Rectifier Output

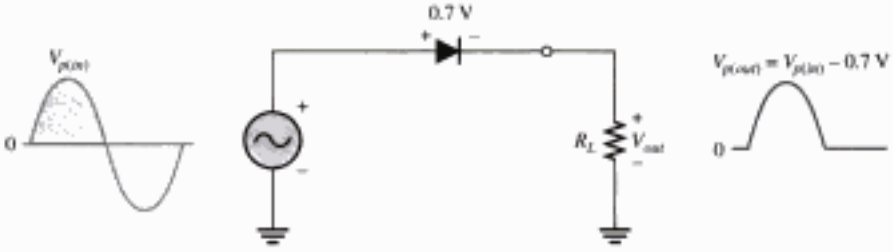
When the practical diode model is used with the barrier potential of 0.7 V taken into account, this is what happens. During the positive half-cycle, the input voltage must overcome the barrier potential before the diode becomes forward-biased. This results in a half-wave output with a peak value that is 0.7 V less than the peak value of the input, as shown in Figure 2–5. The expression for the peak output voltage is

Equation 2–2

$$V_{p(out)} = V_{p(in)} - 0.7\text{ V}$$

▶ **FIGURE 2–5**

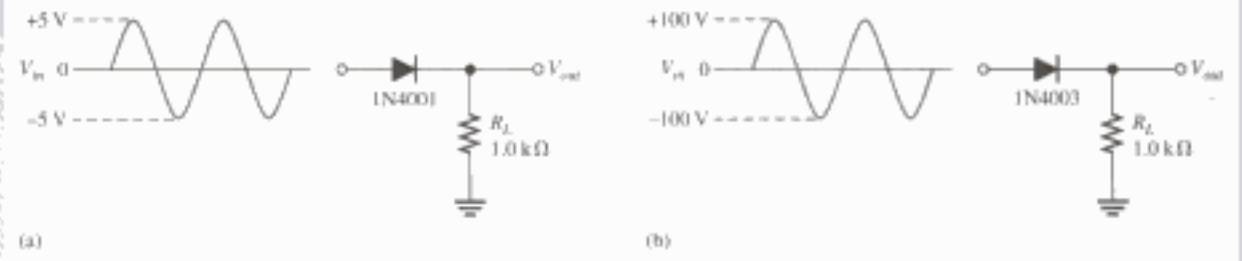
The effect of the barrier potential on the half-wave rectified output voltage is to reduce the peak value of the input by about 0.7 V.



It is usually acceptable to use the ideal diode model, which neglects the effect of the barrier potential, when the peak value of the applied voltage is much greater than the barrier potential (at least 10 V, as a rule of thumb). However, we will use the practical model of a diode, taking the 0.7 V barrier potential into account unless stated otherwise.

EXAMPLE 2–2

Draw the output voltages of each rectifier for the indicated input voltages, as shown in Figure 2–6. The 1N4001 and 1N4003 are specific rectifier diodes.



▲ FIGURE 2–6

Solution The peak output voltage for circuit (a) is

$$V_{p(out)} = V_{p(in)} - 0.7\text{ V} = 5\text{ V} - 0.7\text{ V} = \mathbf{4.30\text{ V}}$$

The peak output voltage for circuit (b) is

$$V_{p(out)} = V_{p(in)} - 0.7\text{ V} = 100\text{ V} - 0.7\text{ V} = \mathbf{99.3\text{ V}}$$

The output voltage waveforms are shown in Figure 2–7. Note that the barrier potential could have been neglected in circuit (b) with very little error (0.7 percent); but, if it is neglected in circuit (a), a significant error results (14 percent).

▶ FIGURE 2–7

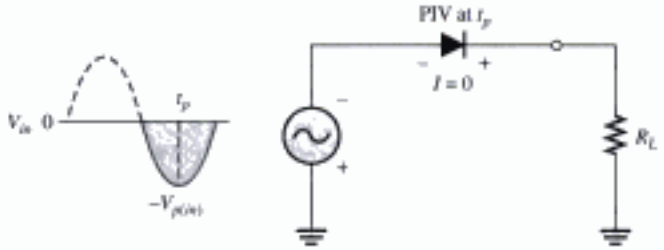
Output voltages for the circuits in Figure 2–6. Obviously, they are not shown on the same scale.

Peak Inverse Voltage (PIV)

The **peak inverse voltage (PIV)** equals the peak value of the input voltage, and the diode must be capable of withstanding this amount of repetitive reverse voltage. For the diode in Figure 2–8, the maximum value of reverse voltage, designated as PIV, occurs at the peak of each negative alternation of the input voltage when the diode is reverse-biased.

$$\text{PIV} = V_{p(in)}$$

Equation 2–3

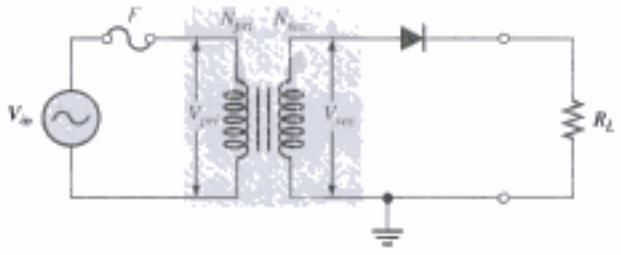


◀ FIGURE 2–8

The PIV occurs at the peak of each half-cycle of the input voltage when the diode is reverse-biased. In this circuit, the PIV occurs at the peak of each negative half-cycle.

Half-Wave Rectifier with Transformer-Coupled Input Voltage

A transformer is often used to couple the ac input voltage from the source to the rectifier, as shown in Figure 2–9. Transformer coupling provides two advantages. First, it allows the source voltage to be stepped up or stepped down as needed. Second, the ac source is electrically isolated from the rectifier, thus preventing a shock hazard in the secondary circuit.



◀ FIGURE 2–9

Half-wave rectifier with transformer-coupled input voltage.

From your study of basic ac circuits recall that the secondary voltage of a transformer equals the turns ratio, n, times the primary voltage, as expressed in Equation 2–4. We will define the turns ratio as the ratio of secondary turns, N_{sec}, to the primary turns, N_{pri}: $n = N_{sec}/N_{pri}$.

$$V_{sec} = nV_{pri}$$

Equation 2–4

If $n > 1$, the secondary voltage is greater than the primary voltage. If $n < 1$, the secondary voltage is less than the primary voltage. If $n = 1$, then $V_{sec} = V_{pri}$.

The peak secondary voltage, $V_{p(sec)}$, in a transformer-coupled half-wave rectifier is the same as $V_{p(in)}$ in Equation 2–2. Therefore, Equation 2–2 written in terms of $V_{p(sec)}$ is

$$V_{p(out)} = V_{p(sec)} - 0.7\text{ V}$$

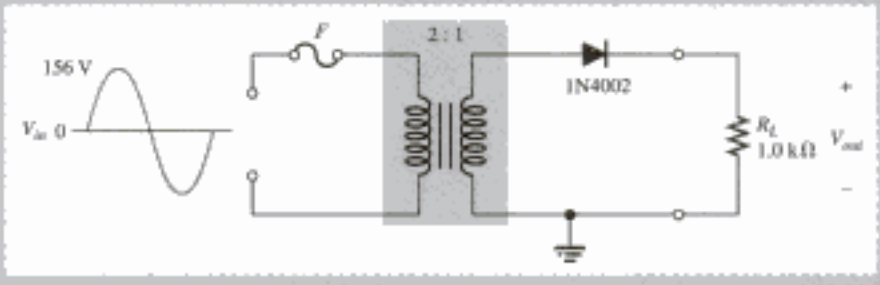
and Equation 2–3 in terms of $V_{p(sec)}$ is

$$\text{PIV} = V_{p(sec)}$$

EXAMPLE 2–3

Determine the peak value of the output voltage for Figure 2–10 if the turns ratio is 0.5.

▶ FIGURE 2–10



Solution

$$V_{p(pri)} = V_{p(in)} = 156\text{ V}$$

The peak secondary voltage is

$$V_{p(sec)} = nV_{p(pri)} = 0.5(156\text{ V}) = 78\text{ V}$$

The rectified peak output voltage is

$$V_{p(out)} = V_{p(sec)} - 0.7\text{ V} = 78\text{ V} - 0.7\text{ V} = \mathbf{77.3\text{ V}}$$

where $V_{p(sec)}$ is the input to the rectifier.

SECTION 2–1 REVIEW

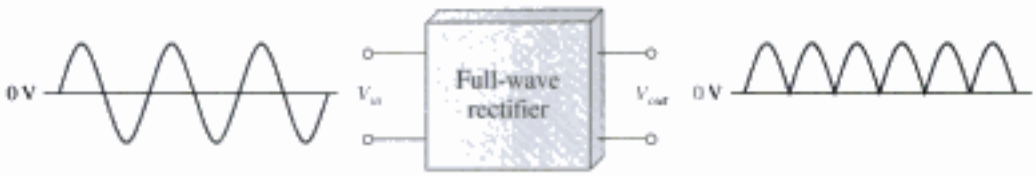
Answers are at the end of the chapter.

1. At what point on the input cycle does the PIV occur?
2. For a half-wave rectifier, there is current through the load for approximately what percentage of the input cycle?
3. What is the average of a half-wave rectified voltage with a peak value of 10 V?
4. What is the peak value of the output voltage of a half-wave rectifier with a peak sine wave input of 25 V?
5. What PIV rating must a diode have to be used in a rectifier with a peak output voltage of 50 V?

2–2 FULL-WAVE RECTIFIERS

Although half-wave rectifiers have some applications, the full-wave rectifier is the most commonly used type in dc power supplies.

A **full-wave rectifier** allows unidirectional (one-way) current through the load during the entire 360° of the input cycle, whereas a half-wave rectifier allows current through the load only during one-half of the cycle. The result of full-wave rectification is an output voltage with a frequency twice the input frequency that pulsates every half-cycle of the input, as shown in Figure 2–11.



▲ FIGURE 2–11

Full-wave rectification.

The number of positive alternations that make up the full-wave rectified voltage is twice that of the half-wave voltage for the same time interval. The average value, which is the value measured on a dc voltmeter, for a full-wave rectified sinusoidal voltage is twice that of the half-wave, as shown in the following formula:

Equation 2–5

$$V_{AVG} = \frac{2V_p}{\pi}$$

V_{AVG} is approximately 63.7% of V_p for a full-wave rectified voltage.

EXAMPLE 2–4

Find the average value of the full-wave rectified voltage in Figure 2–12.

▶ FIGURE 2–12

Solution

$$V_{AVG} = \frac{2V_p}{\pi} = \frac{2(15\text{ V})}{\pi} = \mathbf{9.55\text{ V}}$$

V_{AVG} is 63.7% of V_p.

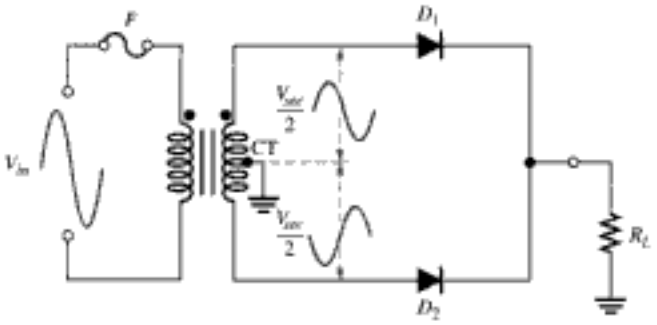
The Center-Tapped Full-Wave Rectifier

A **center-tapped rectifier** is a type of full-wave rectifier that uses two diodes connected to the secondary of a center-tapped transformer, as shown in Figure 2–13. The input voltage is coupled through the transformer to the center-tapped secondary. Half of the total secondary voltage appears between the center tap and each end of the secondary winding as shown.

For a positive half-cycle of the input voltage, the polarities of the secondary voltages are as shown in Figure 2–14(a). This condition forward-biases diode D_1 and reverse-biases diode D_2. The current path is through D_1 and the load resistor R_L, as indicated. For a negative half-cycle of the input voltage, the voltage polarities on the secondary are as shown in Figure 2–14(b). This condition reverse-biases D_1 and forward-biases D_2. The current path is through D_2 and R_L, as indicated. Because the output current during both the positive and

▶ **FIGURE 2–13**

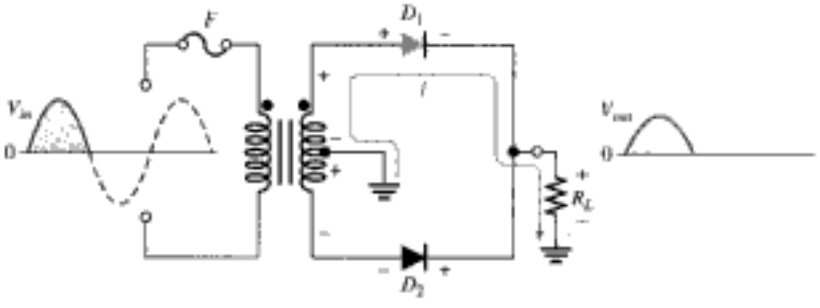
A center-tapped full-wave rectifier.



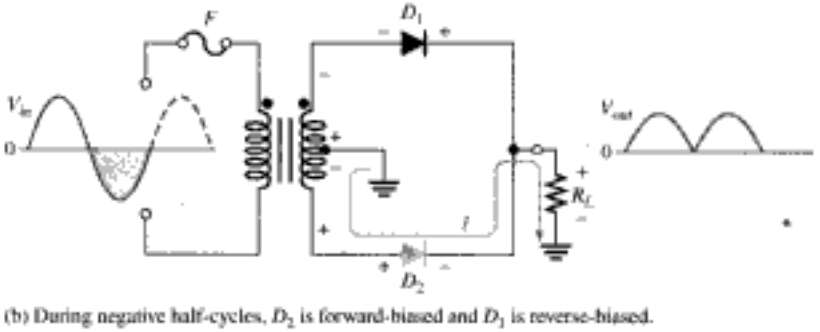
negative portions of the input cycle is in the same direction through the load, the output voltage developed across the load resistor is a full-wave rectified dc voltage, as shown.

▶ **FIGURE 2–14**

Basic operation of a center-tapped full-wave rectifier. Note that the current through the load resistor is in the same direction during the entire input cycle, so the output voltage always has the same polarity.



(a) During positive half-cycles, D_1 is forward-biased and D_2 is reverse-biased.



(b) During negative half-cycles, D_2 is forward-biased and D_1 is reverse-biased.

Effect of the Turns Ratio on the Output Voltage If the transformer's turns ratio is 1, the peak value of the rectified output voltage equals half the peak value of the primary input voltage less the barrier potential, as illustrated in Figure 2–15. Half of the primary voltage appears across each half of the secondary winding ($V_{p(sec)} = V_{p(pri)}$). We will begin referring to the forward voltage due to the barrier potential as the **diode drop**.

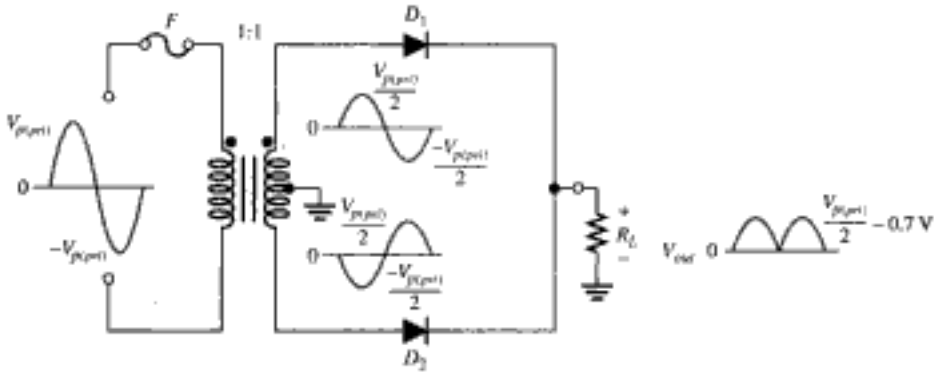
In order to obtain an output voltage with a peak equal to the input peak (less the diode drop), a step-up transformer with a turns ratio of $n = 2$ must be used, as shown in Figure 2–16. In this case, the total secondary voltage (V_{sec}) is twice the primary voltage ($2V_{pri}$), so the voltage across each half of the secondary is equal to V_{pri}.

In any case, the output voltage of a center-tapped full-wave rectifier is always one-half of the total secondary voltage less the diode drop, no matter what the turns ratio.

Equation 2–6

$$V_{out} = \frac{V_{sec}}{2} - 0.7\text{ V}$$

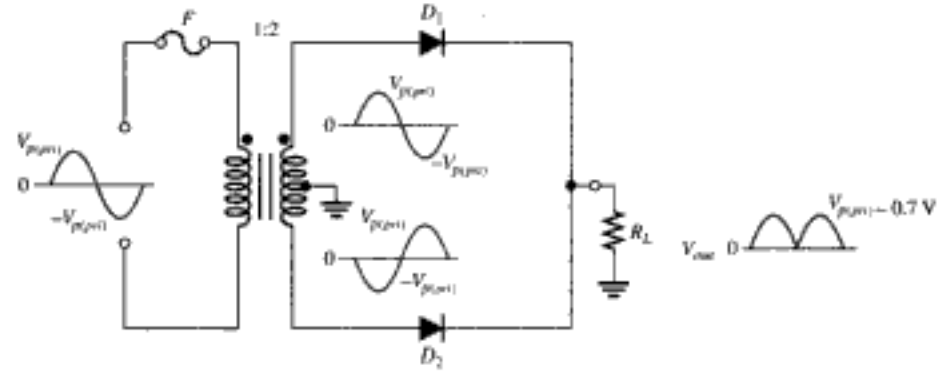
Peak Inverse Voltage Each diode in the full-wave rectifier is alternately forward-biased and then reverse-biased. The maximum reverse voltage that each diode must withstand



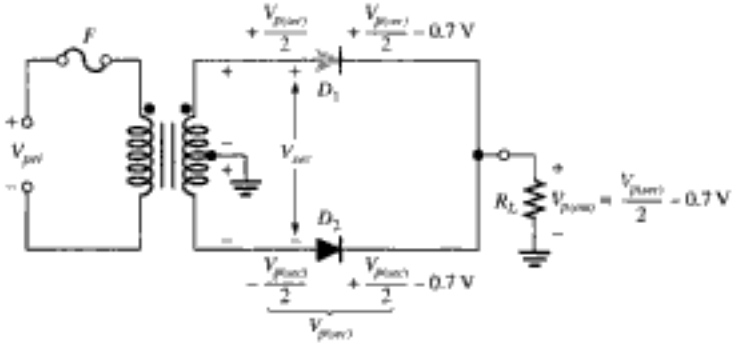
◀ **FIGURE 2–15**
Center-tapped full-wave rectifier with a transformer turns ratio of 1. $V_{p(pri)}$ is the peak value of the primary voltage.

is the peak secondary voltage $V_{p(sec)}$. This is shown in Figure 2–17 where D_2 is assumed to be reverse-biased and D_1 is assumed to be forward-biased to illustrate the concept.

When the total secondary voltage V_{sec} has the polarity shown, the maximum anode voltage of D_1 is $+V_{p(sec)}/2$ and the maximum anode voltage of D_2 is $-V_{p(sec)}/2$. Since D_1 is assumed to be forward-biased, its cathode is at the same voltage as its anode minus the diode drop; this is also the voltage on the cathode of D_2.



◀ **FIGURE 2–16**
Center-tapped full-wave rectifier with a transformer turns ratio of 2.



◀ **FIGURE 2–17**
Diode reverse voltage (D_2 shown reverse-biased and D_1 shown forward-biased).

The peak inverse voltage across D_2 is

$$\text{PIV} = \left(\frac{V_{p(sec)}}{2} - 0.7\text{ V}\right) - \left(-\frac{V_{p(sec)}}{2}\right) = \frac{V_{p(sec)}}{2} + \frac{V_{p(sec)}}{2} - 0.7\text{ V}$$
$$= V_{p(sec)} - 0.7\text{ V}$$

Since $V_{p(out)} = V_{p(sec)}/2 - 0.7$ V, then by multiplying each term by 2 and transposing,

$$V_{p(sec)} = 2V_{p(out)} + 1.4\text{ V}$$

Therefore, by substitution, the peak inverse voltage across either diode in a full-wave center-tapped rectifier is

Equation 2–7

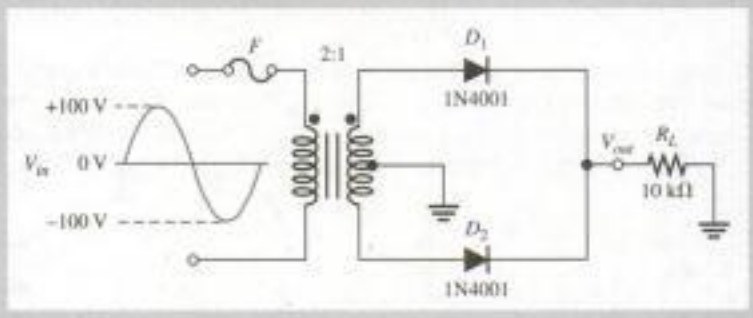
$$PIV = 2V_{p(out)} + 0.7\text{ V}$$

EXAMPLE 2–5

(a) Show the voltage waveforms across each half of the secondary winding and across R_L when a 100 V peak sine wave is applied to the primary winding in Figure 2–18.

(b) What minimum PIV rating must the diodes have?

▶ **FIGURE 2–18**

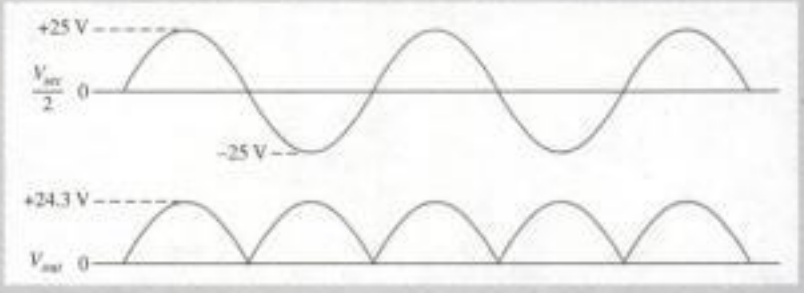


Solution (a) The transformer turns ratio $n = 0.5$. The total peak secondary voltage is

$$V_{p(sec)} = nV_{p(pri)} = 0.5(100\text{ V}) = 50\text{ V}$$

There is a 25 V peak across each half of the secondary with respect to ground. The output load voltage has a peak value of 25 V, less the 0.7 V drop across the diode. The waveforms are shown in Figure 2–19.

▶ **FIGURE 2–19**



(b) Each diode must have a minimum PIV rating of

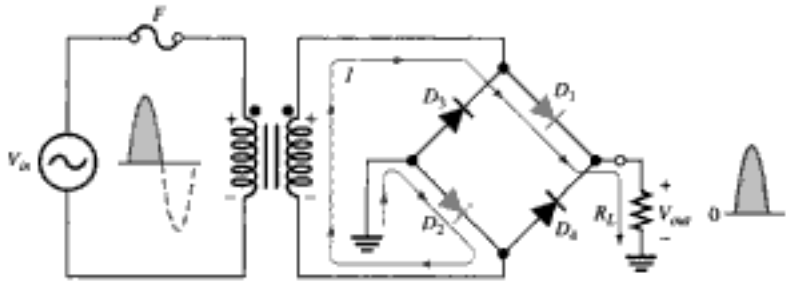
$$PIV = 2V_{p(out)} + 0.7\text{ V} = 2(24.3\text{ V}) + 0.7\text{ V} = \mathbf{49.3\text{ V}}$$

The Bridge Full-Wave Rectifier

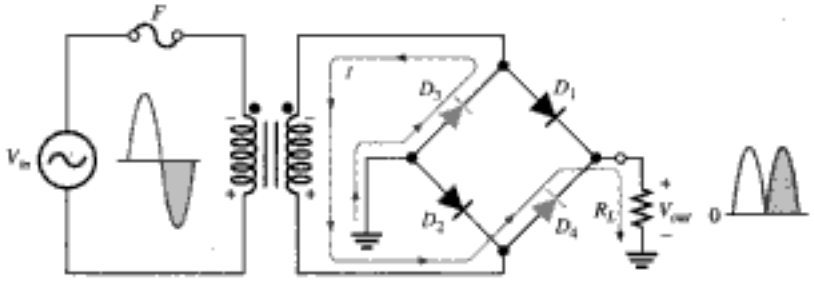
The **bridge rectifier** uses four diodes connected as shown in Figure 2–20. When the input cycle is positive as in part (a), diodes D_1 and D_2 are forward-biased and conduct current in the direction shown. A voltage is developed across R_L that looks like the positive half of the input cycle. During this time, diodes D_3 and D_4 are reverse-biased.

When the input cycle is negative as in Figure 2–20(b), diodes D_3 and D_4 are forward-biased and conduct current in the same direction through R_L as during the positive half-cycle. During the negative half-cycle, D_1 and D_2 are reverse-biased. A full-wave rectified output voltage appears across R_L as a result of this action.

Bridge Output Voltage A bridge rectifier with a transformer-coupled input is shown in Figure 2–21(a). During the positive half-cycle of the total secondary voltage, diodes D_1 and D_2



(a) During the positive half-cycle of the input, D_1 and D_2 are forward-biased and conduct current. D_3 and D_4 are reverse-biased.



(b) During the negative half-cycle of the input, D_3 and D_4 are forward-biased and conduct current. D_1 and D_2 are reverse-biased.

◀ **FIGURE 2–20**

Operation of a bridge rectifier.

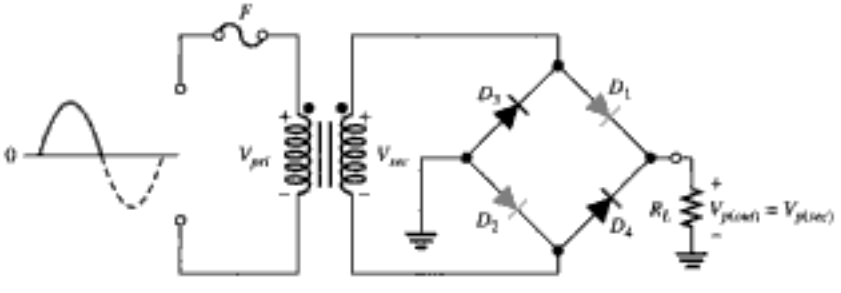
are forward-biased. Neglecting the diode drops, the secondary voltage appears across the load resistor. The same is true when D_3 and D_4 are forward-biased during the negative half-cycle.

$$V_{p(out)} = V_{p(sec)}$$

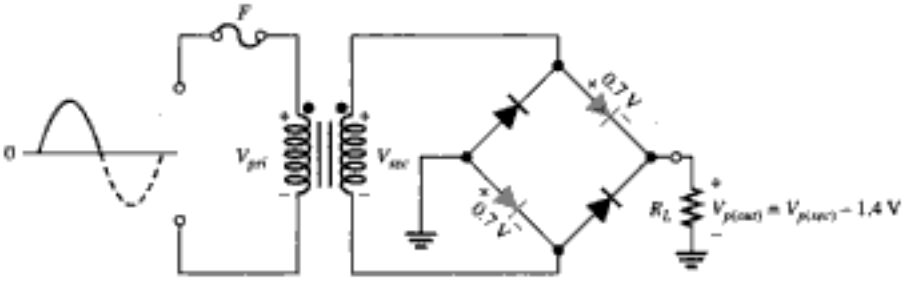
As you can see in Figure 2–21(b), two diodes are always in series with the load resistor during both the positive and negative half-cycles. If these diode drops are taken into account, the output voltage is

$$V_{p(out)} = V_{p(sec)} - 1.4\,\text{V}$$

Equation 2–8



(a) Ideal diodes



(b) Practical diodes (Diode drops included)

◀ **FIGURE 2–21**

Bridge operation during a positive half-cycle of the primary and secondary voltages.

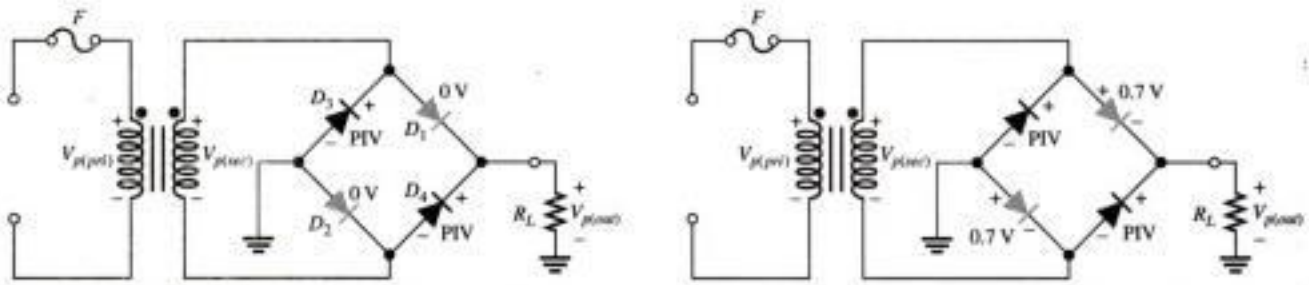
Peak Inverse Voltage Let's assume that D_1 and D_2 are forward-biased and examine the reverse voltage across D_3 and D_4. Visualizing D_1 and D_2 as shorts (ideal model), as in Figure 2–22(a), you can see that D_3 and D_4 have a peak inverse voltage equal to the peak secondary voltage. Since the output voltage is *ideally* equal to the secondary voltage,

$$\text{PIV} = V_{p(out)}$$

If the diode drops of the forward-biased diodes are included as shown in Figure 2–22(b), the peak inverse voltage across each reverse-biased diode in terms of $V_{p(out)}$ is

Equation 2–9

$$\text{PIV} = V_{p(out)} + 0.7\text{ V}$$



(a) For the ideal diode model (forward-biased diodes D_1 and D_2 are shown in gray), PIV = $V_{p(out)}$.

(b) For the practical diode model (forward-biased diodes D_1 and D_2 are shown in gray), PIV = $V_{p(out)}$ + 0.7 V.

▲ FIGURE 2–22

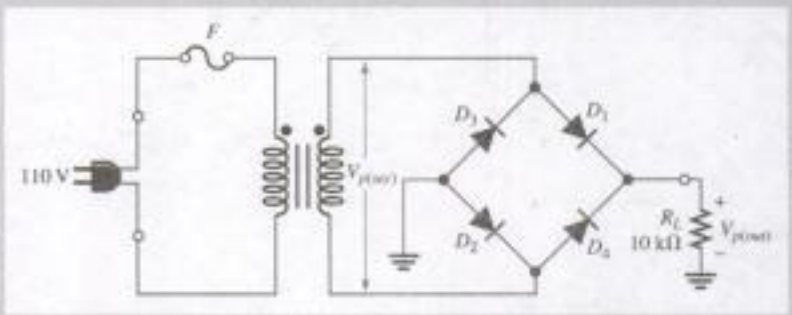
Peak inverse voltages across diodes D_3 and D_4 in a bridge rectifier during the positive half-cycle of the secondary voltage.

The PIV rating of the bridge diodes is less than that required for the center-tapped configuration. If the diode drop is neglected, the bridge rectifier requires diodes with half the PIV rating of those in a center-tapped rectifier for the same output voltage.

EXAMPLE 2–6

Determine the peak output voltage for the bridge rectifier in Figure 2–23. Assuming the practical model, what PIV rating is required for the diodes? The transformer is specified to have a 12 V rms secondary voltage for the standard 110 V across the primary.

► FIGURE 2–23



Solution The peak output voltage (taking into account the two diode drops) is

$$V_{p(sec)} = 1.414\,V_{rms} = 1.414(12\text{ V}) \cong 17\text{ V}$$
$$V_{p(out)} = V_{p(sec)} - 1.4\text{ V} = 17\text{ V} - 1.4\text{ V} = \mathbf{15.6\text{ V}}$$

The PIV rating for each diode is

$$\text{PIV} = V_{p(out)} + 0.7\text{ V} = 15.6\text{ V} + 0.7\text{ V} = \mathbf{16.3\text{ V}}$$

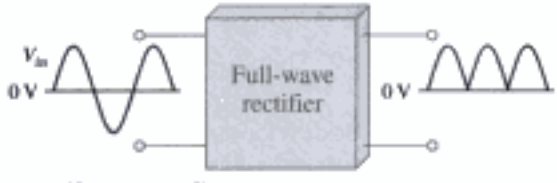
SECTION 2–2 REVIEW

1. How does a full-wave voltage differ from a half-wave voltage?
2. What is the average value of a full-wave rectified voltage with a peak value of 60 V?
3. Which type of full-wave rectifier has the greater output voltage for the same input voltage and transformer turns ratio?
4. For a peak output voltage of 45 V, in which type of rectifier would you use diodes with a PIV rating of 50 V?
5. What PIV rating is required for diodes used in the type of rectifier that was not selected in Question 4?

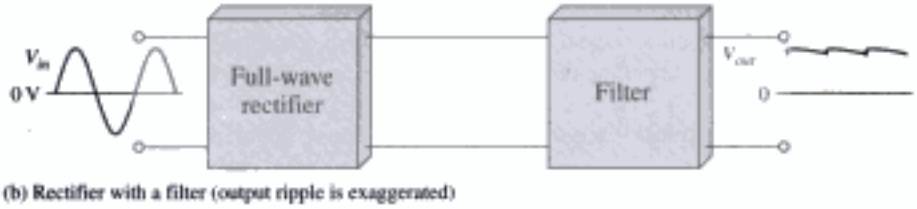
2–3 POWER SUPPLY FILTERS AND CAPACITOR FILTER

A power supply filter ideally eliminates the fluctuations in the output voltage of a half-wave or full-wave rectifier and produces a constant-level dc voltage. Filtering is necessary because electronic circuits require a constant source of dc voltage and current to provide power and biasing for proper operation. Filters are implemented with capacitors. Voltage regulation in power supplies is usually done with integrated circuit voltage regulators. A voltage regulator prevents changes in the filtered dc voltage due to variations in input voltage or load.

In most power supply applications, the standard 50 Hz ac power line voltage must be converted to an approximately constant dc voltage. The 50 Hz pulsating dc output of a half-wave rectifier or the 100 Hz pulsating output of a full-wave rectifier must be filtered to reduce the large voltage variations. Figure 2–24 illustrates the filtering concept showing a nearly smooth dc output voltage from the filter. The small amount of fluctuation in the filter output voltage is called *ripple*.



(a) Rectifier without a filter



(b) Rectifier with a filter (output ripple is exaggerated)

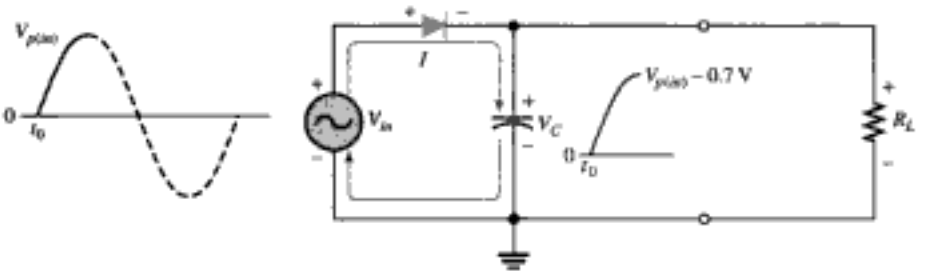
◀ **FIGURE 2–24**
Power supply filtering.

Capacitor-Input Filter

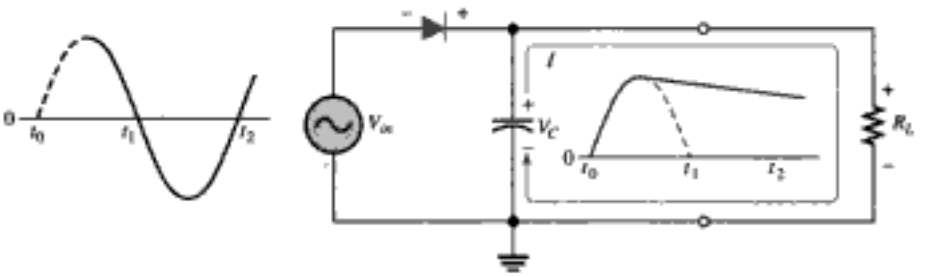
A half-wave rectifier with a capacitor-input filter is shown in Figure 2–25. The filter is simply a capacitor connected from the rectifier output to ground. R_L represents the equivalent resistance of a load. We will use the half-wave rectifier to illustrate the basic principle and then expand the concept to full-wave rectification.

▶ FIGURE 2–25

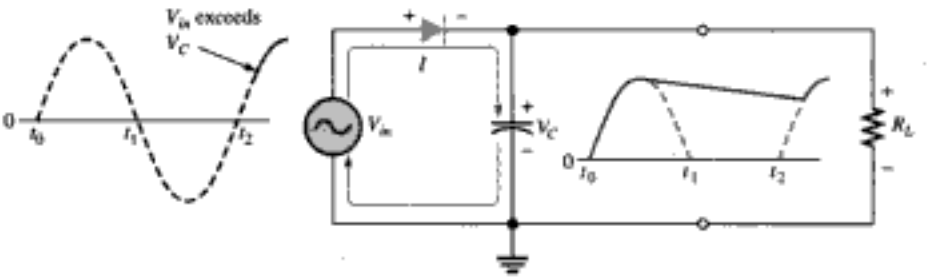
Operation of a half-wave rectifier with a capacitor-input filter. The current indicates charging or discharging of the capacitor.



(a) Initial charging of the capacitor (diode is forward-biased) happens only once when power is turned on.



(b) The capacitor discharges through R_L after peak of positive alternation when the diode is reverse-biased. This discharging occurs during the portion of the input voltage indicated by the solid curve.



(c) The capacitor charges back to peak of input when the diode becomes forward-biased. This charging occurs during the portion of the input voltage indicated by the solid curve.

During the positive first quarter-cycle of the input, the diode is forward-biased, allowing the capacitor to charge to within 0.7 V of the input peak, as illustrated in Figure 2–25(a). When the input begins to decrease below its peak, as shown in part (b), the capacitor retains its charge and the diode becomes reverse-biased because the cathode is more positive than the anode. During the remaining part of the cycle, the capacitor can discharge only through the load resistance at a rate determined by the R_LC time constant, which is normally long compared to the period of the input. The larger the time constant, the less the capacitor will discharge. During the first quarter of the next cycle, as illustrated in part (c), the diode will again become forward-biased when the input voltage exceeds the capacitor voltage by approximately 0.7 V.

Ripple Voltage As you have seen, the capacitor quickly charges at the beginning of a cycle and slowly discharges through R_L after the positive peak of the input voltage (when the diode is reverse-biased). The variation in the capacitor voltage due to the charging and discharging is called the **ripple voltage**. Generally, ripple is undesirable; thus, the smaller the ripple, the better the filtering action, as illustrated in Figure 2–26.

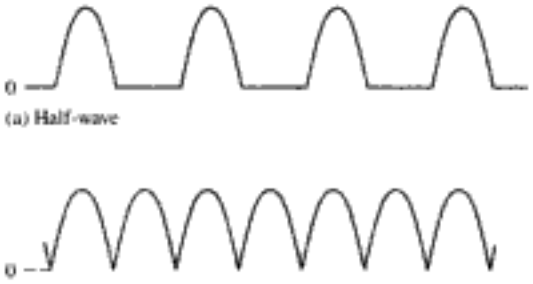
For a given input frequency, the output frequency of a full-wave rectifier is twice that of a half-wave rectifier, as illustrated in Figure 2–27. This makes a full-wave rectifier easier to filter because of the shorter time between peaks. When filtered, the full-wave rectified voltage has a smaller ripple than does a half-wave voltage for the same load resistance and

(a) Larger ripple means less effective filtering.

(b) Smaller ripple means more effective filtering. Generally, the larger the capacitor value, the smaller the ripple for the same input and load.

▲ FIGURE 2–26

Half-wave ripple voltage.

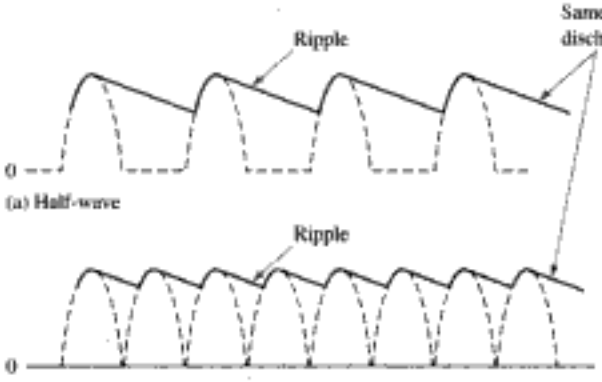


(a) Half-wave

(b) Full-wave

◀ FIGURE 2–27

The frequency of a full-wave rectified voltage is twice that of a half-wave rectified voltage.



(a) Half-wave

(b) Full-wave

◀ FIGURE 2–28

Comparison of ripple voltages for half-wave and full-wave rectified voltages with the same filter capacitor and load and derived from the same sinusoidal input voltage.

capacitor values. The capacitor discharges less during the shorter interval between full-wave pulses, as shown in Figure 2–28.

Ripple Factor The **ripple factor** (r) is an indication of the effectiveness of the filter and is defined as

$$r = \frac{V_{r(pp)}}{V_{DC}}$$

Equation 2–10

where $V_{r(pp)}$ is the peak-to-peak ripple voltage and V_{DC} is the dc (average) value of the filter's output voltage, as illustrated in Figure 2–29. The lower the ripple factor, the better the filter. The ripple factor can be lowered by increasing the value of the filter capacitor or increasing the load resistance.

For a full-wave rectifier with a capacitor-input filter, approximations for the peak-to-peak ripple voltage, $V_{r(pp)}$, and the dc value of the filter output voltage, V_{DC}, are given in the following expressions. The variable $V_{p(rect)}$ is the unfiltered peak rectified voltage.

$$V_{r(pp)} \cong \left(\frac{1}{fR_LC}\right)V_{p(rect)}$$

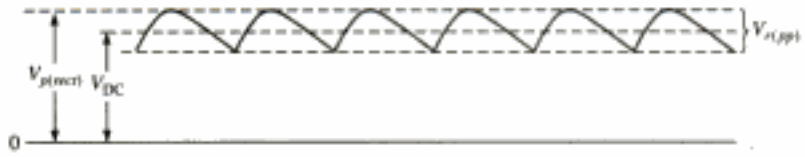
Equation 2–11

$$V_{DC} \cong \left(1 - \frac{1}{2fR_LC}\right)V_{p(rect)}$$

Equation 2–12

▶ **FIGURE 2–29**

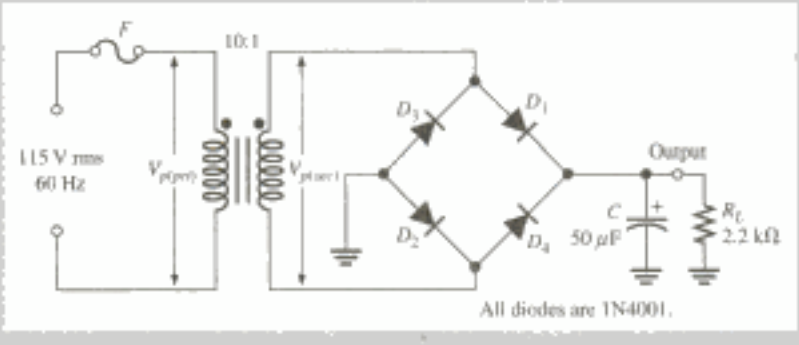
V_r and V_{DC} determine the ripple factor.



EXAMPLE 2–7

Determine the ripple factor for the filtered bridge rectifier with a load as indicated in Figure 2–30.

▶ **FIGURE 2–30**



Solution The transformer turns ratio is $n = 0.1$. The peak primary voltage is

$$V_{p(pri)} = 1.414V_{rms} = 1.414(115\text{ V}) = 163\text{ V}$$

The peak secondary voltage is

$$V_{p(sec)} = nV_{p(pri)} = 0.1(163\text{ V}) = 16.3\text{ V}$$

The unfiltered peak full-wave rectified voltage is

$$V_{p(rect)} = V_{p(sec)} - 1.4\text{ V} = 16.3\text{ V} - 1.4\text{ V} = 14.9\text{ V}$$

The frequency of a full-wave rectified voltage is 120 Hz. The approximate peak-to-peak ripple voltage at the output is

$$V_{r(pp)} \cong \left(\frac{1}{fR_LC}\right)V_{p(rect)} = \left(\frac{1}{(120\text{ Hz})(2.2\text{ k}\Omega)(50\ \mu\text{F})}\right)14.9\text{ V} = 1.13\text{ V}$$

The approximate dc value of the output voltage is determined as follows:

$$V_{DC} = \left(1 - \frac{1}{2fR_LC}\right)V_{p(rect)} = \left(1 - \frac{1}{(240\text{ Hz})(2.2\text{ k}\Omega)(50\ \mu\text{F})}\right)14.9\text{ V} = 14.3\text{ V}$$

The resulting ripple factor is

$$r = \frac{V_{r(pp)}}{V_{DC}} = \frac{1.13\text{ V}}{14.3\text{ V}} = \mathbf{0.079}$$

The percent ripple is 7.9%.

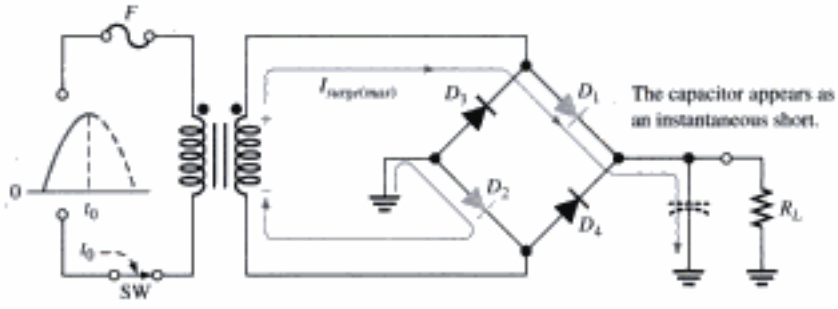
Surge Current in the Capacitor-Input Filter Before the switch in Figure 2–31(a) is closed, the filter capacitor is uncharged. At the instant the switch is closed, voltage is connected to the bridge and the uncharged capacitor appears as a short, as shown. This produces an initial surge of current, I_{surge}, through the two forward-biased diodes D_1 and D_2. The worst-case situation occurs when the switch is closed at a peak of the secondary voltage and a maximum surge current, $I_{surge(max)}$, is produced, as illustrated in the figure.

It is possible that the surge current could destroy the diodes, and for this reason a surge-limiting resistor is sometimes connected, as shown in Figure 2–31(b). The value of this resistor

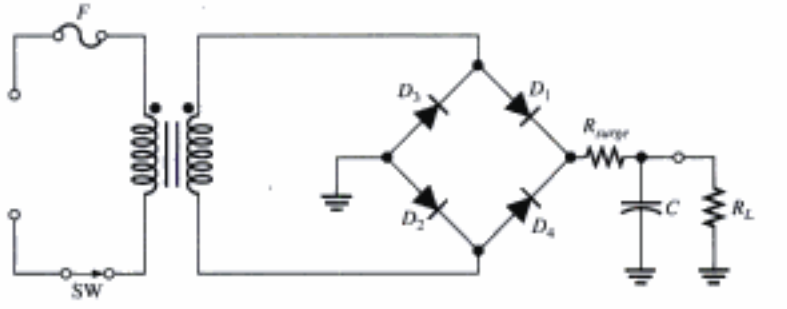
must be small compared to R_L. Also, the diodes must have a maximum forward surge current rating such that they can withstand the momentary surge of current. This rating is specified on diode data sheets as I_{FSM}. The minimum surge resistor value can be calculated as follows:

$$R_{surge} = \frac{V_{p(sec)} - 1.4\text{ V}}{I_{FSM}}$$

Equation 2–13



(a) Maximum surge current occurs when switch is closed at peak of an input cycle.



(b) A series resistor (R_{surge}) limits the surge current.

◀ FIGURE 2–31

Surge current in a capacitor-input filter.

SECTION 2–3 REVIEW

1. When a 60 Hz sinusoidal voltage is applied to the input of a half-wave rectifier, what is the output frequency?
2. When a 60 Hz sinusoidal voltage is applied to the input of a full-wave rectifier, what is the output frequency?
3. What causes the ripple voltage on the output of a capacitor-input filter?
4. If the load resistance connected to a filtered power supply is decreased, what happens to the ripple voltage?
5. Define *ripple factor*.
6. What is the difference between input (line) regulation and load regulation?

2–4 INTEGRATED CIRCUIT VOLTAGE REGULATORS

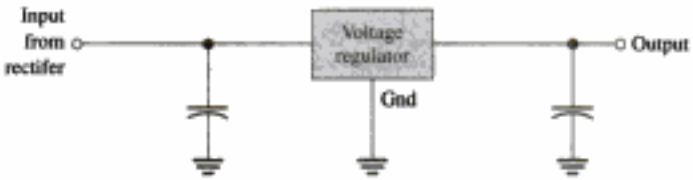
While filters can reduce the ripple from power supplies to a low value, the most effective approach is a combination of a capacitor-input filter used with a voltage regulator. A voltage regulator is connected to the output of a filtered rectifier and maintains a constant output voltage (or current) despite changes in the input, the load current, or the temperature. The capacitor-input filter reduces the input ripple to the regulator to an acceptable level. The combination of a large capacitor and a voltage regulator helps produce an excellent power supply.

Most regulators are integrated circuits and have three terminals—an input terminal, an output terminal, and a reference (or adjust) terminal. The input to the regulator is first filtered with a capacitor to reduce the ripple to <10%. The regulator reduces the ripple to a negligible amount. In addition, most regulators have an internal voltage reference, short-circuit protection, and thermal shutdown circuitry. They are available in a variety of voltages, including positive and negative outputs, and can be designed for variable outputs with a minimum of external components. Typically, voltage regulators can furnish a constant output of one or more amps of current with high ripple rejection.

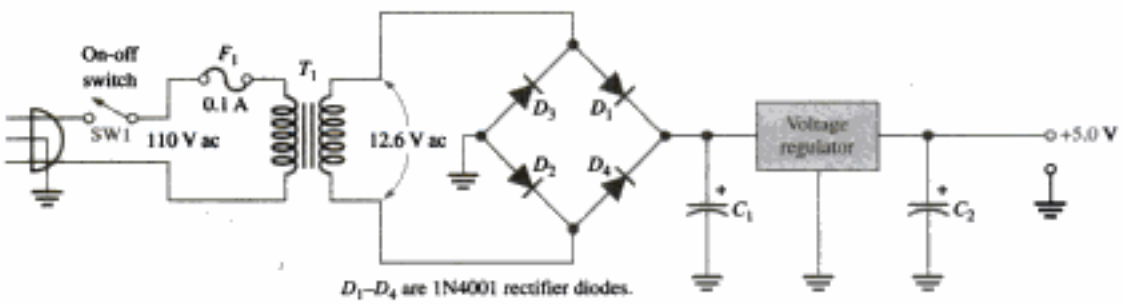
Three-terminal regulators designed for fixed output voltages require only external capacitors to complete the regulation portion of the power supply, as shown in Figure 2–32. Filtering is accomplished by a large-value capacitor between the input voltage and ground. An output capacitor (typically 0.1 μF to 1.0 μF) is connected from the output to ground to improve the transient response.

▶ FIGURE 2–32

A voltage regulator with input and output capacitors.



A basic fixed power supply with a +5 V voltage regulator is shown in Figure 2–33. Several types of both linear and switching regulators are available in integrated circuit (IC) form. Generally, the linear regulators are three-terminal devices that provide either positive or negative output voltages that can be either fixed or adjustable. In this section, typical linear and switching IC regulators are introduced.



▲ FIGURE 2–33

A basic +5.0 V regulated power supply.

Fixed Positive Linear Voltage Regulators

Although many types of IC regulators are available, the 78XX series of IC regulators is representative of three-terminal devices that provide a fixed positive output voltage. The three terminals are input, output, and ground as indicated in the standard fixed voltage configuration in Figure 2–34(a). The last two digits in the part number designate the output voltage. For example, the 7805 is a +5.0 V regulator. Other available output voltages are given in Figure 2–34(b) and common packages are shown in part (c).

Capacitors, although not always necessary, are sometimes used on the input and output as indicated in Figure 2–34(a). The output capacitor acts basically as a line filter to improve transient response. The input capacitor is used to prevent unwanted oscillations when the regulator is some distance from the power supply filter such that the line has a significant inductance.


image
not
available

Adjustable Positive Linear Voltage Regulators

The LM317 is an example of a three-terminal positive regulator with an adjustable output voltage. The standard configuration is shown in Figure 2–36. The capacitors are for decoupling and do not affect the dc operation. Notice that there is an input, an output, and an adjustment terminal. The external fixed resistor R_1 and the external variable resistor R_2 provide the output voltage adjustment. V_{out} can be varied from 1.2 V to 37 V depending on the resistor values. The LM317 can provide over 1.5 A of output current to a load.

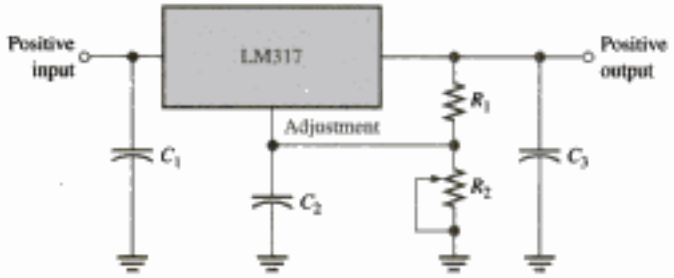
The LM317 is operated as a "floating" regulator because the adjustment terminal is not connected to ground, but floats to whatever voltage is across R_2. This allows the output voltage to be much higher than that of a fixed-voltage regulator.

Basic Operation As indicated in Figure 2–37, a constant 1.25 V reference voltage (V_{REF}) is maintained by the regulator between the output terminal and the adjustment terminal. This constant reference voltage produces a constant current (I_{REF}) through R_1, regardless of the value of R_2. I_{REF} is also through R_2.

$$I_{REF} = \frac{V_{REF}}{R_1} = \frac{1.25\text{ V}}{R_1}$$

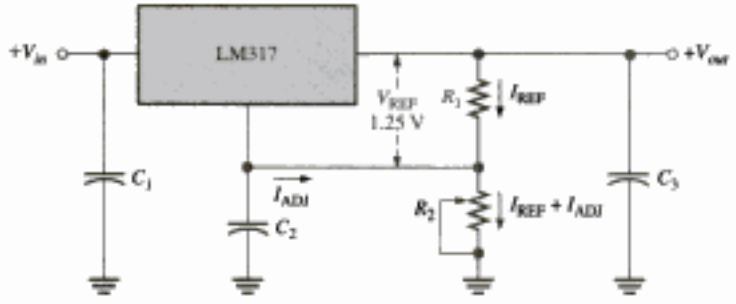
▶ FIGURE 2–36

The LM317 three-terminal adjustable positive voltage regulator.



▶ FIGURE 2–37

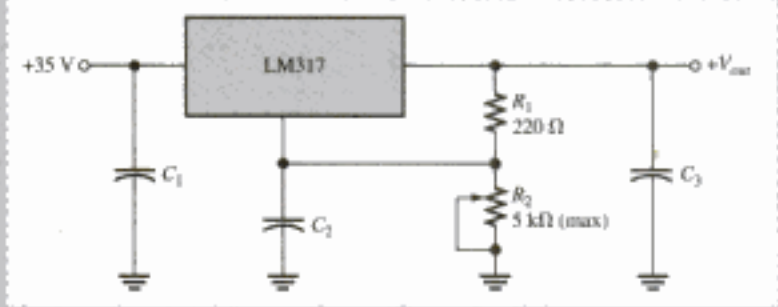
Operation of the LM317 adjustable voltage regulator.



EXAMPLE 2–8

Determine the minimum and maximum output voltages for the voltage regulator in Figure 2–38. Assume $I_{ADJ} = 50\ \mu A$.

▶ FIGURE 2–38



Solution $V_{R1} = V_{REF} = 1.25\text{ V}$

When R_2 is set at its minimum of 0 Ω,

$$V_{out(min)} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2 = 1.25\text{ V}(1) = \mathbf{1.25\text{ V}}$$

When R_2 is set at its maximum of 5 kΩ,

$$V_{out(max)} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2 = 1.25\text{ V}\left(1 + \frac{5\text{ k}\Omega}{220\ \Omega}\right) + (50\ \mu\text{A})5\text{ k}\Omega$$

There is a very small constant current at the adjustment terminal of approximately 50 μA called I_{ADJ}, which is through R_2. A formula for the output voltage is developed as follows.

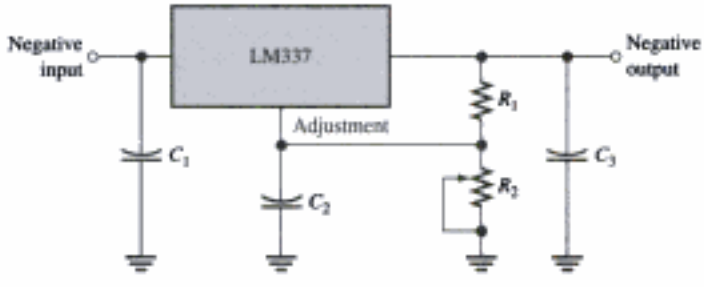
$$V_{out} = V_{R1} + V_{R2} = I_{REF}R_1 + I_{REF}R_2 + I_{ADJ}R_2$$
$$= I_{REF}(R_1 + R_2) + I_{ADJ}R_2 = \frac{V_{REF}}{R_1}(R_1 + R_2) + I_{ADJ}R_2$$

$$V_{out} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{ADJ}R_2 \qquad \textbf{Equation 2–14}$$

As you can see, the output voltage is a function of both R_1 and R_2. Once the value of R_1 is set, the output voltage is adjusted by varying R_2.

Adjustable Negative Linear Voltage Regulators

The LM337 is the negative output counterpart of the LM317 and is a good example of this type of IC regulator. Like the LM317, the LM337 requires two external resistors for output voltage adjustment as shown in Figure 2–39. The output voltage can be adjusted from −1.2 V to −37 V, depending on the external resistor values. The capacitors are for decoupling and do not affect the dc operation.



◀ FIGURE 2–39
The LM337 three-terminal adjustable negative voltage regulator.

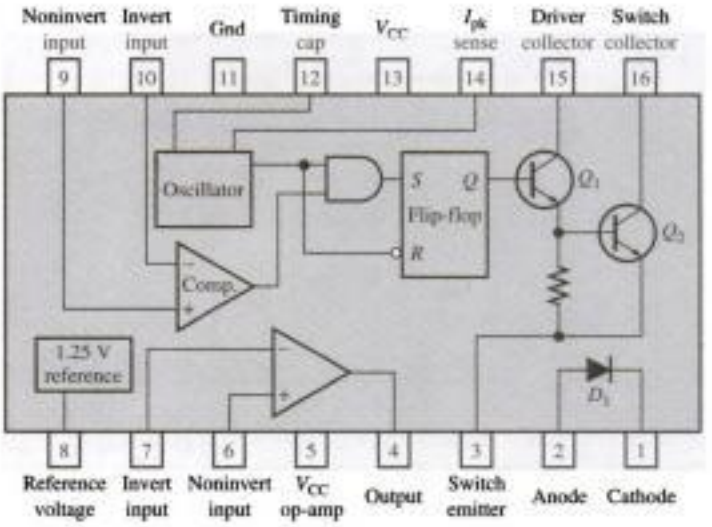
Switching Voltage Regulators

As an example of an IC switching voltage regulator, let's look at the 78S40. This is a universal device that can be used with external components to provide step-up, step-down, and inverting operation.

The internal circuitry of the 78S40 is shown in Figure 2–40. This circuit can be compared to the basic switching regulators that were covered in Section 18–4. For example, look back at Figure 18–16(a). The oscillator and comparator functions are directly comparable. The gate and flip-flop in the 78S40 were not included in the basic circuit of Figure 18–16(a), but they provide additional regulating action. Transistors Q_1 and Q_2 effectively perform the same function as Q_1 in the basic circuit. The 1.25 V reference block in the 78S40 has the same purpose as the zener diode in the basic circuit, and diode D_1 in the 78S40 corresponds to D_1 in the basic circuit.

▶ FIGURE 2–40

The 78S40 switching regulator.



The 78S40 also has an "uncommited" op-amp thrown in for good measure. It is not used in any of the regulator configurations. External circuitry is required to make this device operate as a regulator, as you will see in Section 18–5.

Percent Regulation

The regulation expressed as a percentage is a figure of merit used to specify the performance of a voltage regulator. It can be in terms of input (line) regulation or load regulation. **Line regulation** specifies how much change occurs in the output voltage for a given change in the input voltage. It is typically defined as a ratio of a change in output voltage for a corresponding change in the input voltage expressed as a percentage.

Equation 2–15

$$\text{Line regulation} = \left(\frac{\Delta V_{out}}{\Delta V_{in}}\right)100\%$$

Load regulation specifies how much change occurs in the output voltage over a certain range of load current values, usually from minimum current (no load, NL) to maximum current (full load, FL). It is normally expressed as a percentage and can be calculated with the following formula:

Equation 2–16

$$\text{Load regulation} = \left(\frac{V_{NL} - V_{FL}}{V_{FL}}\right)100\%$$

where V_{NL} is the output voltage with no load and V_{FL} is the output voltage with full (maximum) load.

EXAMPLE 2–9

A certain 7805 regulator has a measured no-load output voltage of 5.18 V and a full-load output of 5.15 V. What is the load regulation expressed as a percentage?

Solution

$$\text{Load regulation} = \left(\frac{V_{NL} - V_{FL}}{V_{FL}}\right)100\% = \left(\frac{5.18\text{ V} - 5.15\text{ V}}{5.15\text{ V}}\right)100\% = \mathbf{0.58\%}$$

2–5 DIODE LIMITING AND CLAMPING CIRCUITS

Diode circuits, called limiters or clippers, are sometimes used to clip off portions of signal voltages above or below certain levels. Another type of diode circuit, called a clamper, is used to add or restore a dc level to an electrical signal. Both limiter and clamper diode circuits will be examined in this section.

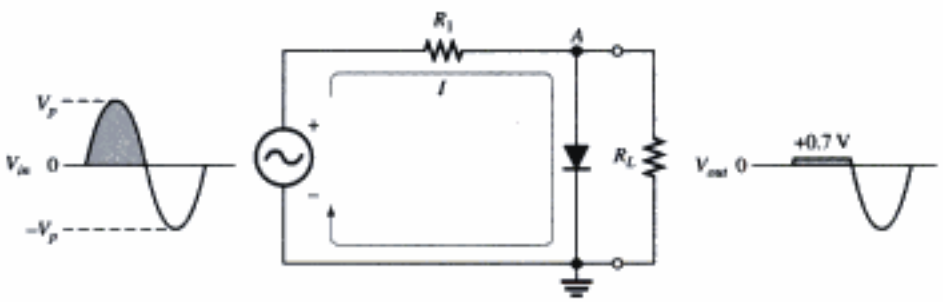
Diode Limiters

Figure 2–41(a) shows a diode **limiter** (also called **clipper**) that limits or clips the positive part of the input voltage. As the input voltage goes positive, the diode becomes forward-biased and conducts current. Because the cathode is at ground potential (0 V), the anode cannot exceed 0.7 V (assuming silicon). So point *A* is limited to +0.7 V when the input voltage exceeds this value. When the input voltage goes back below 0.7 V, the diode is reverse-biased and appears as an open. The output voltage looks like the negative part of the input voltage, but with a magnitude determined by the voltage divider formed by R_1 and the load resistor, R_L, as follows:

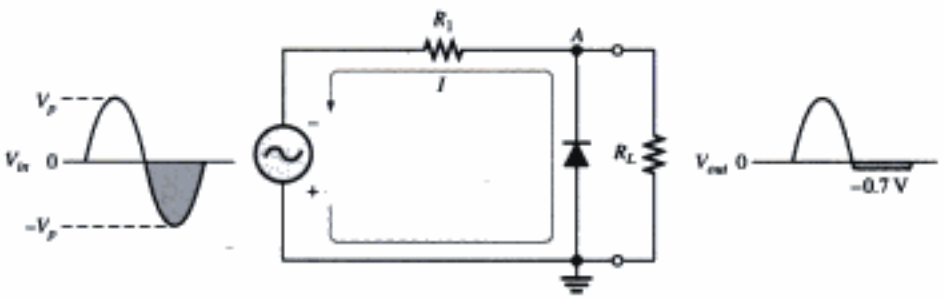
$$V_{out} = \left(\frac{R_L}{R_1 + R_L}\right)V_{in}$$

If R_1 is small compared to R_L, then $V_{out} = V_{in}$.

If the diode is turned around, as in Figure 2–41(b), the negative part of the input voltage is clipped off. When the diode is forward-biased during the negative part of the input voltage, point *A* is held at −0.7 V by the diode drop. When the input voltage goes above −0.7 V, the diode is no longer forward-biased; and a voltage appears across R_L proportional to the input voltage.



(a) Limiting of the positive alternation. The diode is forward-biased during the positive alternation (above 0.7 V) and reverse-biased during the negative alternation.



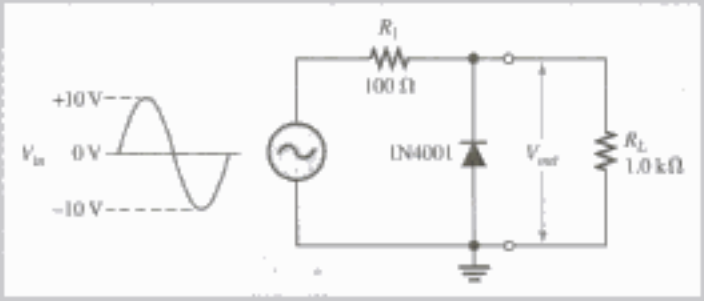
(b) Limiting of the negative alternation. The diode is forward-biased during the negative alternation (below −0.7 V) and reverse-biased during the positive alternation.

◀ **FIGURE 2–41**
Examples of diode limiters (clippers).

EXAMPLE 2–10

What would you expect to see displayed on an oscilloscope connected across R_L in the limiter shown in Figure 2–42?

▶ FIGURE 2–42



Solution The diode is forward-biased and conducts when the input voltage goes below −0.7 V. So, for the negative limiter, determine the peak output voltage across R_L by the following equation:

$$V_{p(out)} = \left(\frac{R_L}{R_1 + R_L}\right)V_{p(in)} = \left(\frac{1.0\text{ k}\Omega}{1.1\text{ k}\Omega}\right)10\text{ V} = 9.09\text{ V}$$

The scope will display an output waveform as shown in Figure 2–43.

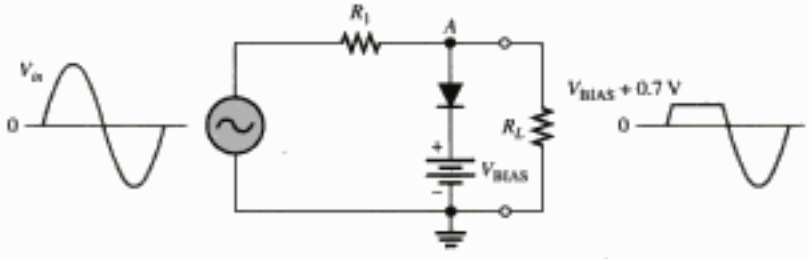
▶ FIGURE 2–43

Output voltage waveform for Figure 2–42.

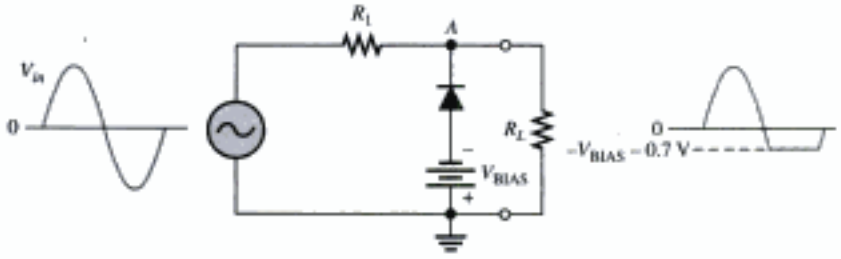
Biased Limiters The level to which an ac voltage is limited can be adjusted by adding a bias voltage, V_{BIAS}, in series with the diode, as shown in Figure 2–44. The voltage at point A must equal V_{BIAS} + 0.7 V before the diode will become forward-biased and conduct. Once the diode begins to conduct, the voltage at point A is limited to V_{BIAS} + 0.7 V so that all input voltage above this level is clipped off.

▶ FIGURE 2–44

A positive limiter.



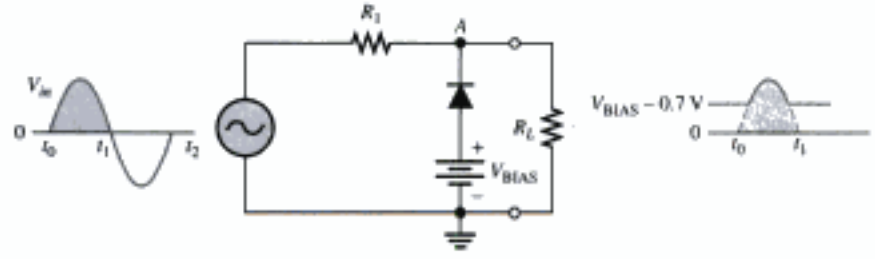
To limit a voltage to a specified negative level, the diode and bias voltage must be connected as in Figure 2–45. In this case, the voltage at point A must go below $-V_{BIAS} - 0.7$ V to forward-bias the diode and initiate limiting action as shown.



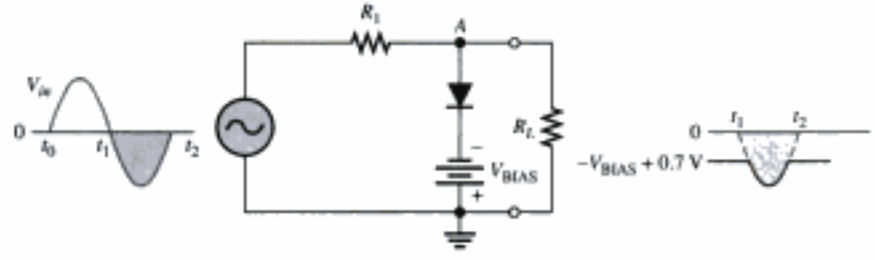
◀ **FIGURE 2–45**
A negative limiter.

By turning the diode around, the positive limiter can be modified to limit the output voltage to the portion of the input voltage waveform above $V_{BIAS} - 0.7$ V, as shown by the output waveform in Figure 2–46(a). Similarly, the negative limiter can be modified to limit the output voltage to the portion of the input voltage waveform below $-V_{BIAS} + 0.7$ V, as shown by the output waveform in part (b).

◀ **FIGURE 2–46**



(a)

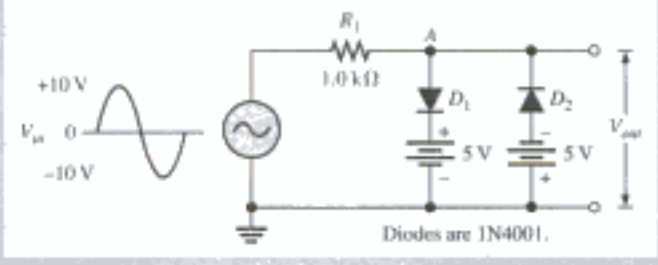


(b)

EXAMPLE 2–11

Figure 2–47 shows a circuit combining a positive limiter with a negative limiter. Determine the output voltage waveform.

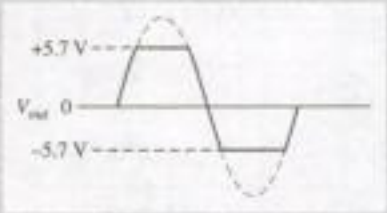
▶ **FIGURE 2–47**



Solution When the voltage at point *A* reaches +5.7 V, diode D_1 conducts and limits the waveform to +5.7 V. Diode D_2 does not conduct until the voltage reaches −5.7 V. Therefore, positive voltages above +5.7 V and negative voltages below −5.7 V are clipped off. The resulting output voltage waveform is shown in Figure 2–48.

► FIGURE 2–48

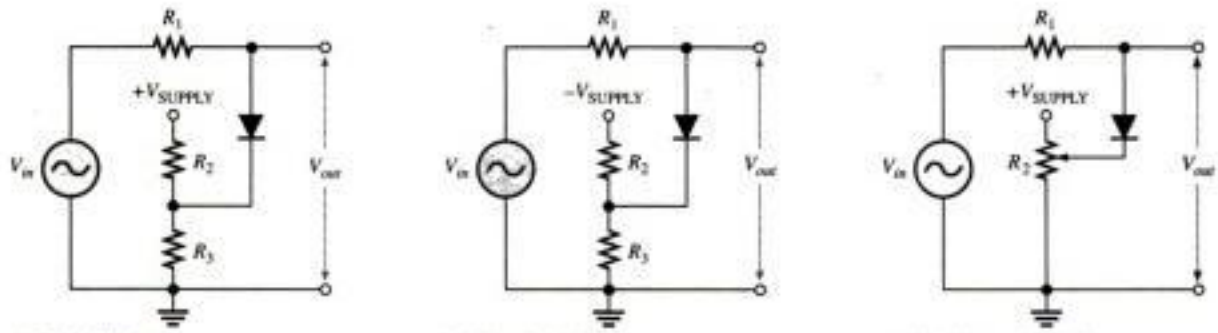
Output voltage waveform for Figure 2–47.



Voltage-Divider Bias The bias voltage sources that have been used to illustrate the basic operation of diode limiters can be replaced by a resistive voltage divider that derives the desired bias voltage from the dc supply voltage, as shown in Figure 2–49. The bias voltage is set by the resistor values according to the voltage-divider formula.

$$V_{BIAS} = \left(\frac{R_3}{R_2 + R_3}\right) V_{SUPPLY}$$

A positively biased limiter is shown in Figure 2–49(a), a negatively biased limiter is shown in part (b), and a variable positive bias circuit using a potentiometer voltage divider is shown in part (c). The bias resistors must be small compared to R_1 so that the forward current through the diode will not affect the bias voltage.



(a) Positive limiter (b) Negative limiter (c) Variable positive limiter

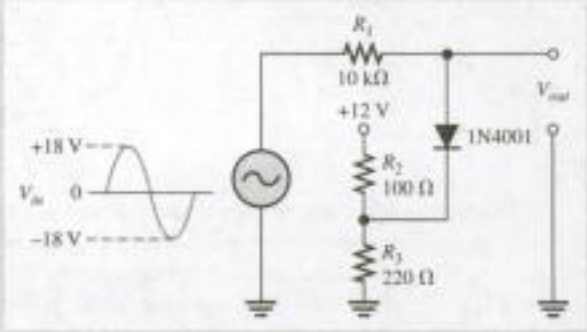
▲ FIGURE 2–49

Diode limiters implemented with voltage–divider bias.

EXAMPLE 2–12

Describe the output voltage waveform for the diode limiter in Figure 2–50.

► FIGURE 2–50



Solution The circuit is a positive limiter. Use the voltage-divider formula to determine the bias voltage.

$$V_{BIAS} = \left(\frac{R_3}{R_2 + R_3}\right)V_{SUPPLY} = \left(\frac{220\ \Omega}{100\ \Omega + 220\ \Omega}\right)12\ \text{V} = 8.25\ \text{V}$$

The output voltage waveform is shown in Figure 2–51. The positive part of the output voltage waveform is limited to $V_{BIAS} + 0.7$ V.

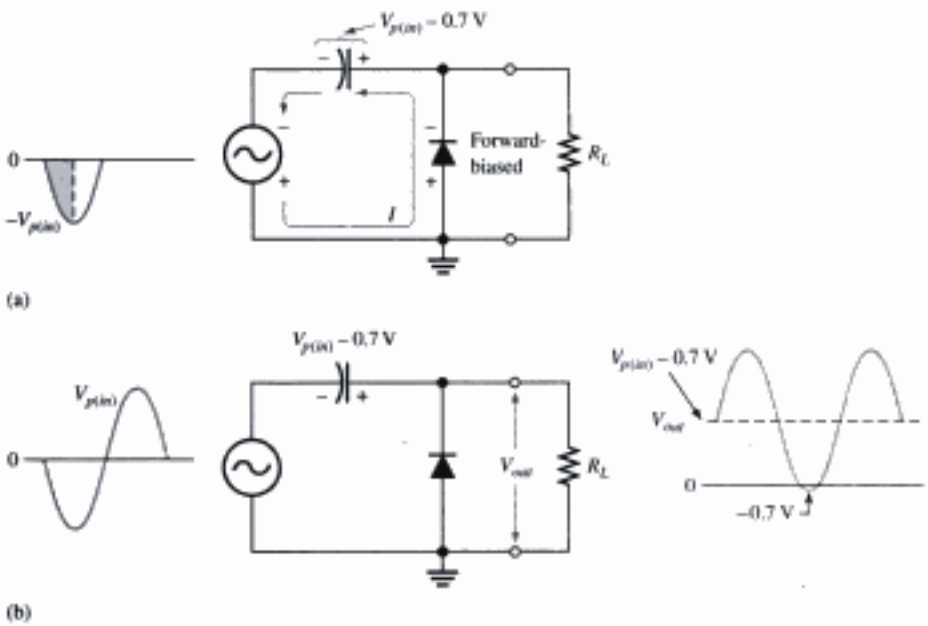
► **FIGURE 2–51**

Diode Clampers

A clamper adds a dc level to an ac voltage. **Clampers** are sometimes known as *dc restorers*. Figure 2–52 shows a diode clamper that inserts a positive dc level in the output waveform. The operation of this circuit can be seen by considering the first negative half-cycle of the input voltage. When the input voltage initially goes negative, the diode is forward-biased, allowing the capacitor to charge to near the peak of the input ($V_{p(in)} - 0.7$ V), as shown in Figure 2–52(a). Just after the negative peak, the diode is reverse-biased. This is because the cathode is held near $V_{p(in)} - 0.7$ V by the charge on the capacitor. The capacitor can only discharge through the high resistance of R_L. So, from the peak of one negative half-cycle to the next, the capacitor discharges very little. The amount that is discharged, of course, depends on the value of R_L. For good clamping action, the RC time constant should be at least ten times the period of the input frequency.

The net effect of the clamping action is that the capacitor retains a charge approximately equal to the peak value of the input less the diode drop. The capacitor voltage acts essentially as a battery in series with the input voltage. The dc voltage of the capacitor adds to the input voltage by superposition, as in Figure 2–52(b).

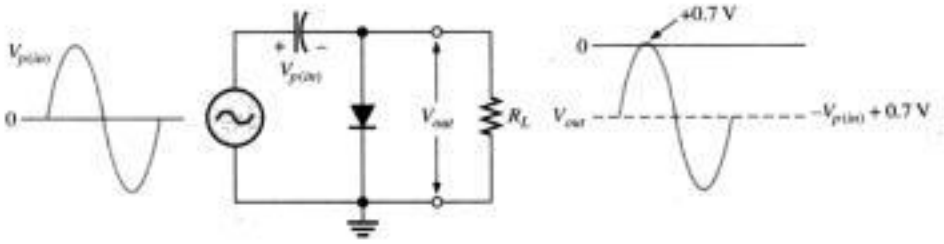
If the diode is turned around, a negative dc voltage is added to the input voltage to produce the output voltage as shown in Figure 2–53.



◄ **FIGURE 2–52**
Positive clamper operation.

► FIGURE 2–53

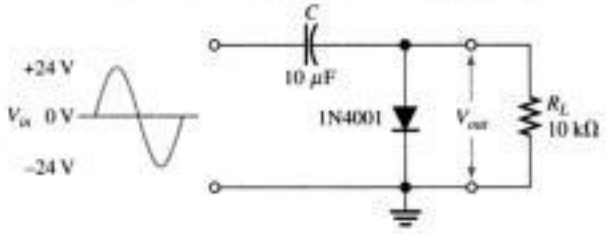
Negative clamper.



EXAMPLE 2–13

What is the output voltage that you would expect to observe across R_L in the clamping circuit of Figure 2–54? Assume that RC is large enough to prevent significant capacitor discharge.

► FIGURE 2–54



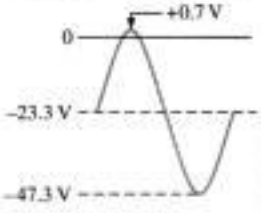
Solution Ideally, a negative dc value equal to the input peak less the diode drop is inserted by the clamping circuit.

$$V_{DC} \equiv -(V_{p(in)} - 0.7\text{ V}) = -(24\text{ V} - 0.7\text{ V}) = \mathbf{-23.3\text{ V}}$$

Actually, the capacitor will discharge slightly between peaks, and, as a result, the output voltage will have an average value of slightly less than that calculated above. The output waveform goes to approximately +0.7 V, as shown in Figure 2–55.

► FIGURE 2–55

Output waveform across R_L for Figure 2–54.



SECTION 2–5 REVIEW

1. Discuss how diode limiters and diode clampers differ in terms of their function.
2. What is the difference between a positive limiter and a negative limiter?
3. What is the maximum voltage across an unbiased positive silicon diode limiter during the positive alternation of the input voltage?
4. To limit the output voltage of a positive limiter to 5 V when a 10 V peak input is applied, what value must the bias voltage be?
5. What component in a clamping circuit effectively acts as a battery?

2–6 VOLTAGE MULTIPLIERS

Voltage multipliers use clamping action to increase peak rectified voltages without the necessity of increasing the transformer's voltage rating. Multiplication factors of two, three, and four are common. Voltage multipliers are used in high-voltage, low-current applications such as TV receivers.

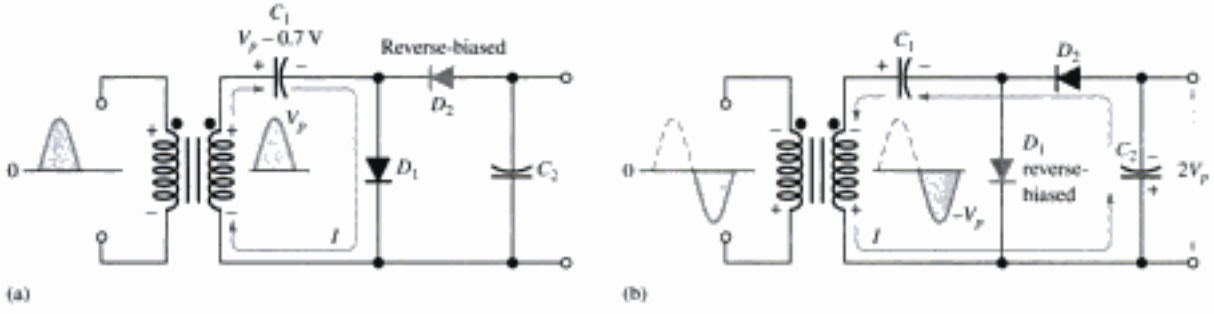
Voltage Doubler

Half-Wave Voltage Doubler A voltage doubler is a **voltage multiplier** with a multiplication factor of two. A half-wave voltage doubler is shown in Figure 2–56. During the positive half-cycle of the secondary voltage, diode D_1 is forward-biased and D_2 is reverse-biased. Capacitor C_1 is charged to the peak of the secondary voltage (V_p) less the diode drop with the polarity shown in part (a). During the negative half-cycle, diode D_2 is forward-biased and D_1 is reverse-biased, as shown in part (b). Since C_1 can't discharge, the peak voltage on C_1 adds to the secondary voltage to charge C_2 to approximately $2V_p$. Applying Kirchhoff's law around the loop as shown in part (b), the voltage across C_2 is

$$V_{C1} - V_{C2} + V_p = 0$$
$$V_{C2} = V_p + V_{C1}$$

Neglecting the diode drop of D_2, $V_{C1} = V_p$. Therefore,

$$V_{C2} = V_p + V_p = 2V_p$$



▲ FIGURE 2–56

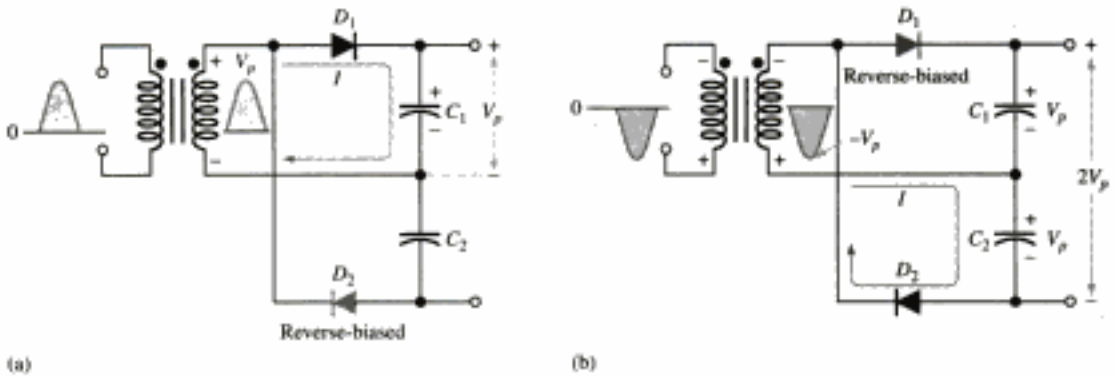
Half-wave voltage doubler operation. V_p is the peak secondary voltage.

Under a no-load condition, C_2 remains charged to approximately $2V_p$. If a load resistance is connected across the output, C_2 discharges slightly through the load on the next positive half-cycle and is again recharged to $2V_p$ on the following negative half-cycle. The resulting output is a half-wave, capacitor-filtered voltage. The peak inverse voltage across each diode is $2V_p$.

Full-Wave Voltage Doubler A full-wave doubler is shown in Figure 2–57. When the secondary voltage is positive, D_1 is forward-biased and C_1 charges to approximately V_p, as shown in part (a). During the negative half-cycle, D_2 is forward-biased and C_2 charges to approximately V_p, as shown in part (b). The output voltage, $2V_p$, is taken across the two capacitors in series.

Voltage Tripler

The addition of another diode-capacitor section to the half-wave voltage doubler creates a voltage tripler, as shown in Figure 2–58. The operation is as follows: On the positive half-cycle of the secondary voltage, C_1 charges to V_p through D_1. During the negative half-cycle, C_2 charges

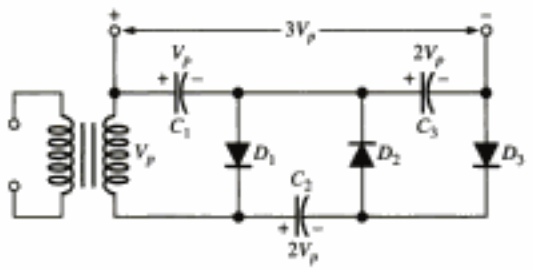


▲ FIGURE 2–57

Full-wave voltage doubler operation.

▶ FIGURE 2–58

Voltage tripler.



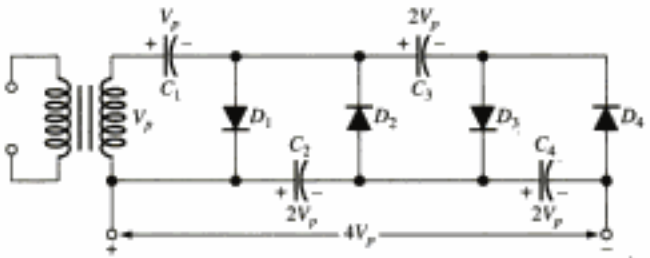
to $2V_p$ through D_2, as described for the doubler. During the next positive half-cycle, C_3 charges to $2V_p$ through D_3. The tripler output is taken across C_1 and C_3, as shown in the figure.

Voltage Quadrupler

The addition of still another diode-capacitor section, as shown in Figure 2–59, produces an output four times the peak secondary voltage. C_4 charges to $2V_p$ through D_4 on a negative half-cycle. The $4V_p$ output is taken across C_2 and C_4, as shown. In both the tripler and quadrupler circuits, the PIV of each diode is $2V_p$.

▶ FIGURE 2–59

Voltage quadrupler.

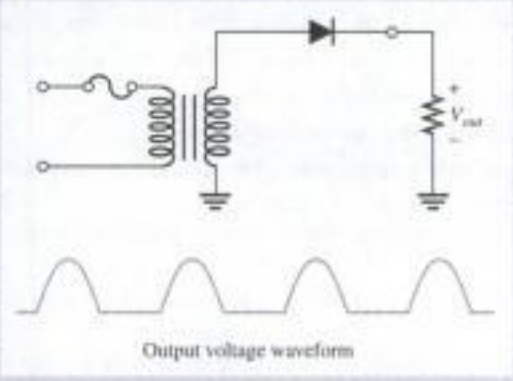


SECTION 2–6 REVIEW

1. What must be the peak voltage rating of the transformer secondary for a voltage doubler that produces an output of 200 V?
2. The output voltage of a quadrupler is 620 V. What minimum PIV rating must each diode have?

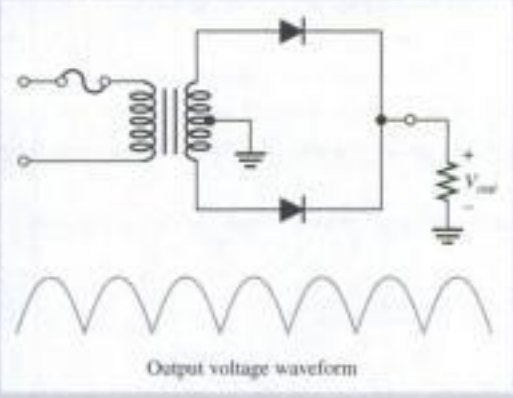
SUMMARY OF POWER SUPPLY RECTIFIERS

HALF-WAVE RECTIFIER



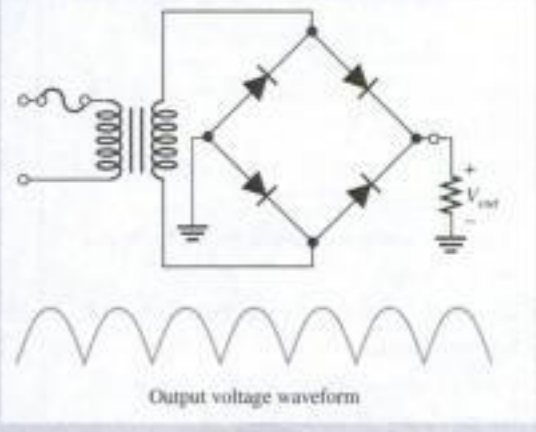
- Peak value of output:
  $V_{p(out)} = V_{p(sec)} - 0.7\text{ V}$
- Average value of output:
  $$V_{AVG} = \frac{V_{p(out)}}{\pi}$$
- Diode peak inverse voltage:
  $\text{PIV} = V_{p(sec)}$

CENTER-TAPPED FULL-WAVE RECTIFIER



- Peak value of output:
  $$V_{p(out)} = \frac{V_{p(sec)}}{2} - 0.7\text{ V}$$
- Average value of output:
  $$V_{AVG} = \frac{2V_{p(out)}}{\pi}$$
- Diode peak inverse voltage:
  $\text{PIV} = 2V_{p(out)} + 0.7\text{ V}$

BRIDGE FULL-WAVE RECTIFIER



- Peak value of output:
  $V_{p(out)} = V_{p(sec)} - 1.4\text{ V}$
- Average value of output:
  $$V_{AVG} = \frac{2V_{p(out)}}{\pi}$$
- Diode peak inverse voltage:
  $\text{PIV} = V_{p(out)} + 0.7\text{ V}$

CHAPTER SUMMARY

- The single diode in a half-wave rectifier is forward-biased and conducts for 180° of the input cycle.
- The output frequency of a half-wave rectifier equals the input frequency.
- PIV (peak inverse voltage) is the maximum voltage appearing across the diode in reverse bias.
- Each diode in a full-wave rectifier is forward-biased and conducts for 180° of the input cycle.
- The output frequency of a full-wave rectifier is twice the input frequency.
- The two basic types of full-wave rectifier are center-tapped and bridge.
- The peak output voltage of a center-tapped full-wave rectifier is approximately one-half of the total peak secondary voltage less one diode drop.
- The PIV for each diode in a center-tapped full-wave rectifier is twice the peak output voltage plus one diode drop.
- The peak output voltage of a bridge rectifier equals the total peak secondary voltage less two diode drops.
- The PIV for each diode in a bridge rectifier is approximately half that required for an equivalent center-tapped configuration and is equal to the peak output voltage plus one diode drop.
- A capacitor-input filter provides a dc output approximately equal to the peak of its rectified input voltage.
- Ripple voltage is caused by the charging and discharging of the filter capacitor.
- The smaller the ripple voltage, the better the filter.
- Regulation of output voltage over a range of input voltages is called *input* or *line regulation*.
- Regulation of output voltage over a range of load currents is called *load regulation*.
- Diode limiters cut off voltage above or below specified levels. Limiters are also called *clippers*.
- Diode clampers add a dc level to an ac voltage.
- A dc power supply typically consists of an input transformer, a diode rectifier, a filter, and a regulator.

OBJECTIVE TYPE QUESTIONS

Answers are at the end of the chapter.

1. If the input voltage in Figure 2–10 is increased, the peak inverse voltage across the diode will
   (a) increase **(b)** decrease **(c)** not change
2. If the turns ratio of the transformer in Figure 2–10 is decreased, the forward current through the diode will
   (a) increase **(b)** decrease **(c)** not change
3. If the frequency of the input voltage in Figure 2–18 is increased, the output voltage will
   (a) increase **(b)** decrease **(c)** not change
4. If the PIV rating of the diodes in Figure 2–18 is increased, the current through R_L will
   (a) increase **(b)** decrease **(c)** not change
5. If one of the diodes in Figure 2–23 opens, the average voltage to the load will
   (a) increase **(b)** decrease **(c)** not change
6. If the value of R_L in Figure 2–23 is decreased, the current through each diode will
   (a) increase **(b)** decrease **(c)** not change
7. If the capacitor value in Figure 2–30 is decreased, the output ripple voltage will
   (a) increase **(b)** decrease **(c)** not change
8. If the line voltage in Figure 2–33 is increased, ideally the +5 V output will
   (a) increase **(b)** decrease **(c)** not change
9. If the bias voltage in Figure 2–37 is decreased, the positive portion of the output voltage will
   (a) increase **(b)** decrease **(c)** not change

10. If the bias voltage in Figure 2–37 is increased, the negative portion of the output voltage will
(a) increase **(b)** decrease **(c)** not change

11. If the value of R_3 in Figure 2–50 is decreased, the positive output voltage will
(a) increase **(b)** decrease **(c)** not change

12. If the input voltage in Figure 2–54 is increased, the peak negative value of the output voltage will
(a) increase **(b)** decrease **(c)** not change

13. The average value of a half-wave rectified voltage with a peak value of 200 V is
(a) 63.7 V **(b)** 127.3 V **(c)** 141 V **(d)** 0 V

14. When a 60 Hz sinusoidal voltage is applied to the input of a half-wave rectifier, the output frequency is
(a) 120 Hz **(b)** 30 Hz **(c)** 60 Hz **(d)** 0 Hz

15. The peak value of the input to a half-wave rectifier is 10 V. The approximate peak value of the output is
(a) 10 V **(b)** 3.18 V **(c)** 10.7 V **(d)** 9.3 V

16. For the circuit in Question 3, the diode must be able to withstand a reverse voltage of
(a) 10 V **(b)** 5 V **(c)** 20 V **(d)** 3.18 V

17. The average value of a full-wave rectified voltage with a peak value of 75 V is
(a) 53 V **(b)** 47.8 V **(c)** 37.5 V **(d)** 23.9 V

18. When a 60 Hz sinusoidal voltage is applied to the input of a full-wave rectifier, the output frequency is
(a) 120 Hz **(b)** 60 Hz **(c)** 240 Hz **(d)** 0 Hz

19. The total secondary voltage in a center-tapped full-wave rectifier is 125 V rms. Neglecting the diode drop, the rms output voltage is
(a) 125 V **(b)** 177 V **(c)** 100 V **(d)** 62.5 V

20. When the peak output voltage is 100 V, the PIV for each diode in a center-tapped full-wave rectifier is (neglecting the diode drop)
(a) 100 V **(b)** 200 V **(c)** 141 V **(d)** 50 V

21. When the rms output voltage of a bridge full-wave rectifier is 20 V, the peak inverse voltage across the diodes is (neglecting the diode drop)
(a) 20 V **(b)** 40 V **(c)** 28.3 V **(d)** 56.6 V

22. The ideal dc output voltage of a capacitor-input filter is equal to
(a) the peak value of the rectified voltage
(b) the average value of the rectified voltage
(c) the rms value of the rectified voltage

23. A certain power-supply filter produces an output with a ripple of 100 mV peak-to-peak and a dc value of 20 V. The ripple factor is
(a) 0.05 **(b)** 0.005 **(c)** 0.00005 **(d)** 0.02

24. A 60 V peak full-wave rectified voltage is applied to a capacitor-input filter. If $f = 120$ Hz, $R_L = 10\ \text{k}\Omega$, and $C = 10\ \mu\text{F}$, the ripple voltage is
(a) 0.6 V **(b)** 6 mV **(c)** 5.0 V **(d)** 2.88 V

25. If the load resistance of a capacitor-filtered full-wave rectifier is reduced, the ripple voltage
(a) increases **(b)** decreases **(c)** is not affected **(d)** has a different frequency

26. Line regulation is determined by
(a) load current
(b) zener current and load current
(c) changes in load resistance and output voltage
(d) changes in output voltage and input voltage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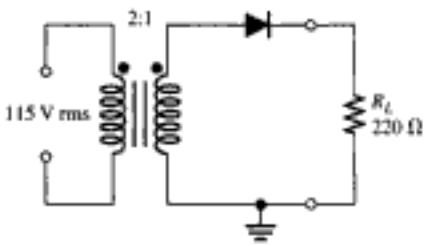
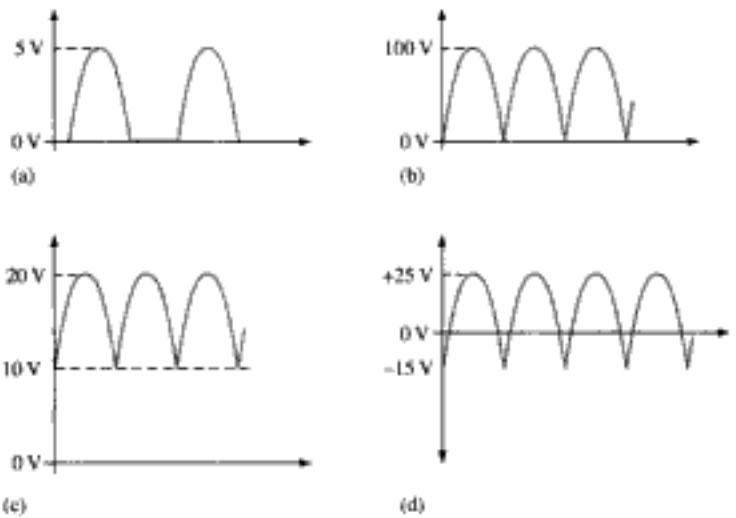
4. Determine the peak and average power delivered to R_L in Figure 2–61.



◀ FIGURE 2–61

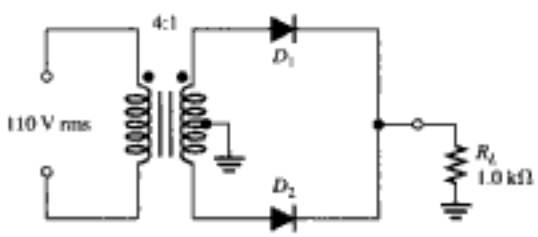
SECTION 2–2 Full-Wave Rectifiers

5. Find the average value of each voltage in Figure 2–62.



▲ FIGURE 2–62

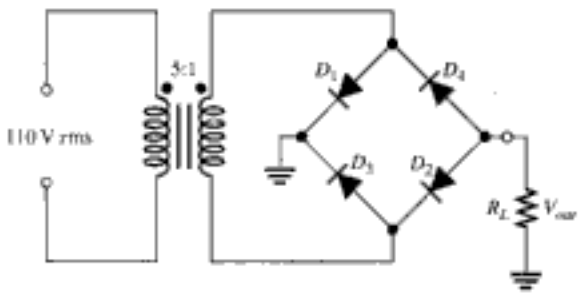
6. Consider the circuit in Figure 2–63.
   - **(a)** What type of circuit is this?
   - **(b)** What is the total peak secondary voltage?
   - **(c)** Find the peak voltage across each half of the secondary.
   - **(d)** Sketch the voltage waveform across R_L.
   - **(e)** What is the peak current through each diode?
   - **(f)** What is the PIV for each diode?



◀ FIGURE 2–63

7. Calculate the peak voltage across each half of a center-tapped transformer used in a full-wave rectifier that has an average output voltage of 110 V.

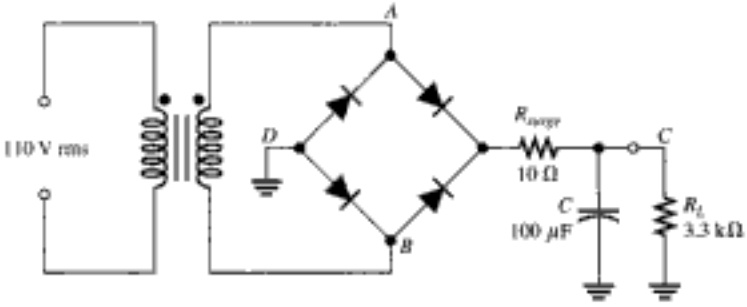
8. Show how to connect the diodes in a center-tapped rectifier in order to produce a negative-going full-wave voltage across the load resistor.
9. What PIV rating is required for the diodes in a bridge rectifier that produces an average output voltage of 50 V?
10. The rms output voltage of a bridge rectifier is 20 V. What is the peak inverse voltage across the diodes?
11. Draw the output voltage of the bridge rectifier in Figure 2–64. Notice that all the diodes are reversed from previous circuits.



▲ FIGURE 2–64

SECTION 2–3 Power Supply Filters and Capacitor Filter

12. A certain rectifier filter produces a dc output voltage of 75 V with a peak-to-peak ripple voltage of 0.5 V. Calculate the ripple factor.
13. A certain full-wave rectifier has a peak output voltage of 30 V. A 50 μF capacitor-input filter is connected to the rectifier. Calculate the peak-to-peak ripple and the dc output voltage developed across a 600 Ω load resistance.
14. What is the percentage of ripple for the rectifier filter in Problem 13?
15. What value of filter capacitor is required to produce a 1% ripple factor for a full-wave rectifier having a load resistance of 1.5 kΩ? Assume the rectifier produces a peak output of 18 V.
16. A full-wave rectifier produces an 80 V peak rectified voltage from a 60 Hz ac source. If a 10 μF filter capacitor is used, determine the ripple factor for a load resistance of 10 kΩ.
17. Determine the peak-to-peak ripple and dc output voltages in Figure 2–65. The transformer has a 36 V rms secondary voltage rating, and the line voltage has a frequency of 60 Hz.



▲ FIGURE 2–65

18. Refer to Figure 2–65 and draw the following voltage waveforms in relationship to the input waveforms: V_{AB}, V_{AD}, and V_{CD}. A double letter subscript indicates a voltage from one point to another.
19. If the no-load output voltage of a regulator is 15.5 V and the full-load output is 14.9 V, what is the percent load regulation?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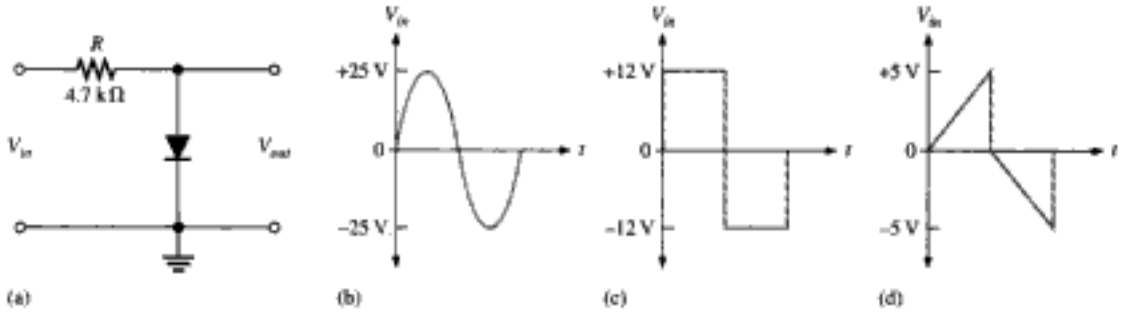
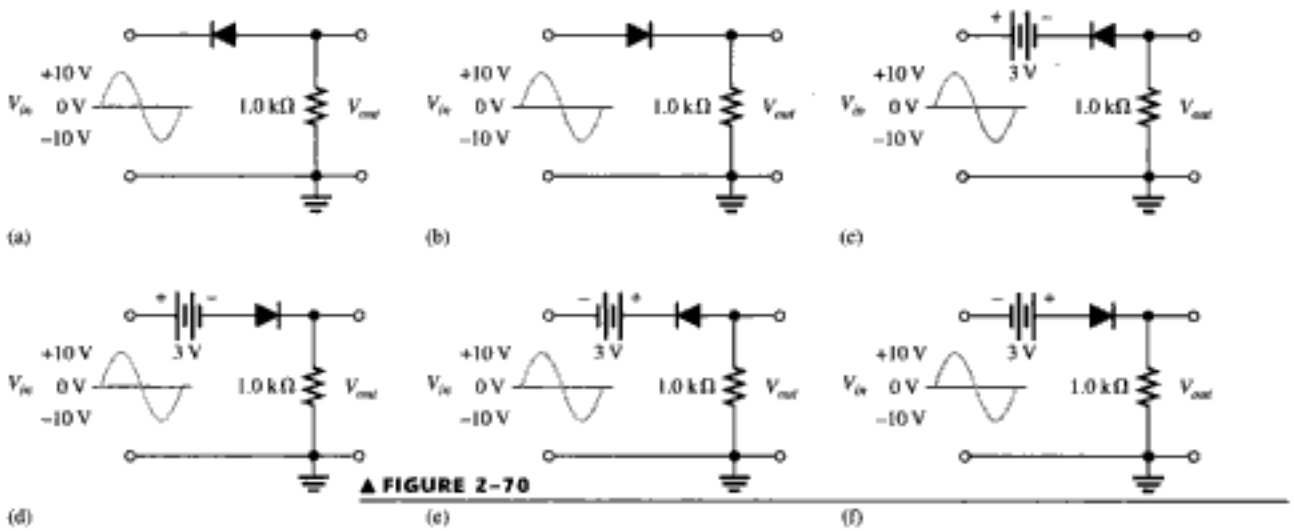
27. Determine the output voltage for the circuit in Figure 2–69(a) for each input voltage in (b), (c), and (d).



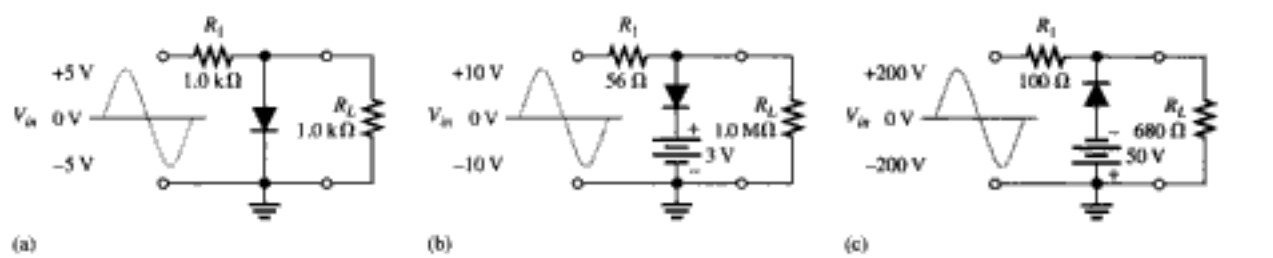
▲ **FIGURE 2–69**

28. Determine the output voltage waveform for each circuit in Figure 2–70.



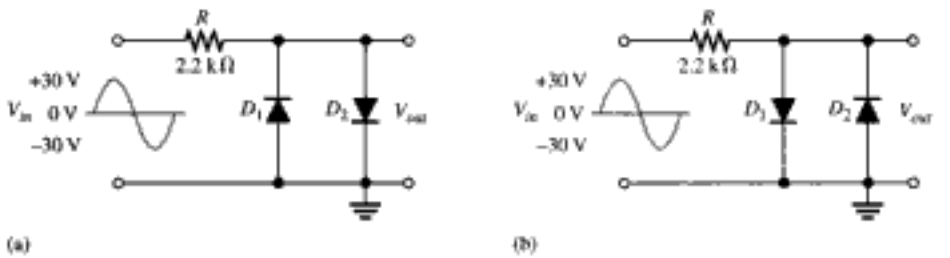
▲ **FIGURE 2–70**

29. Determine the R_L voltage waveform for each circuit in Figure 2–71.



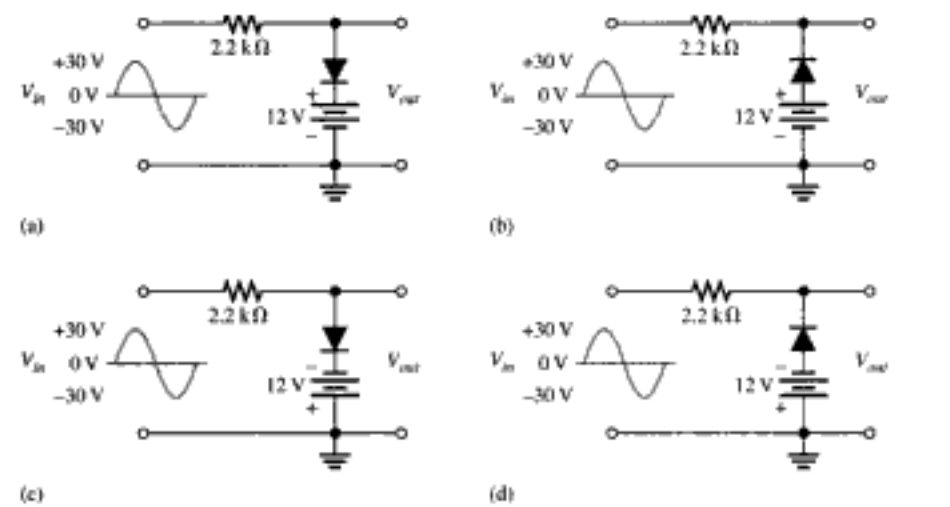
▲ **FIGURE 2–71**

30. Draw the output voltage waveform for each circuit in Figure 2–72.



◀ **FIGURE 2–72**

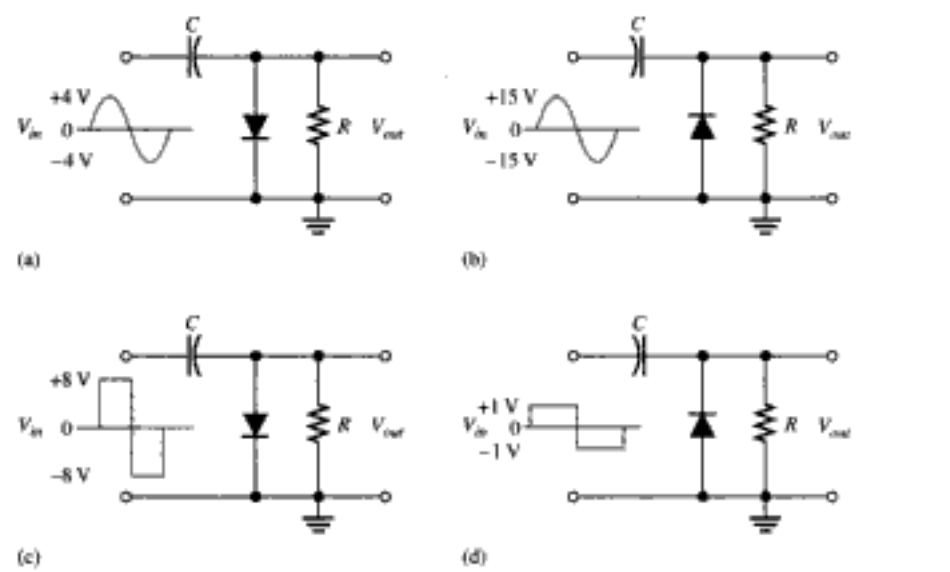
31. Determine the output voltage waveform for each circuit in Figure 2–73.



◀ **FIGURE 2–73**

32. Describe the output waveform of each circuit in Figure 2–74. Assume the *RC* time constant is much greater than the period of the input.

33. Repeat Problem 32 with the diodes turned around.



◀ **FIGURE 2–74**

SECTION 2–6 Voltage Multipliers

34. A certain voltage doubler has 20 V rms on its input. What is the output voltage? Draw the circuit, indicating the output terminals and PIV rating for the diode.

35. Repeat Problem 34 for a voltage tripler and quadrupler.

ADVANCED PROBLEMS

36. A full-wave rectifier with a capacitor-input filter provides a dc output voltage of 35 V to a 3.3 kΩ load. Determine the minimum value of filter capacitor if the maximum peak-to-peak ripple voltage is to be 0.5 V.

37. A certain unfiltered full-wave rectifier with 115 V, 60 Hz input produces an output with a peak of 15 V. When a capacitor-input filter and a 1.0 kΩ load are connected, the dc output voltage is 14 V. What is the peak-to-peak ripple voltage?

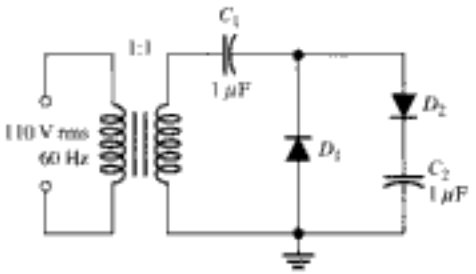
38. For a certain full-wave rectifier, the measured surge current in the capacitor filter is 50 A. The transformer is rated for a secondary voltage of 24 V with a 110 V, 60 Hz input. Determine the value of the surge resistor in this circuit.

39. Design a filtered power supply that can produce dc output voltages of +9 V ± 10% and −9 V ±10% with a maximum load current of 100 mA. The voltages are to be switch selectable across one set of output terminals. The ripple voltage must not exceed 0.25 V rms.

40. Design a circuit to limit a 20 V rms sinusoidal voltage to a maximum positive amplitude of 18 V and a maximum negative amplitude of 10 V using a single 24 V dc voltage source.

41. Determine the voltage across each capacitor in the circuit of Figure 2–75.

► **FIGURE 2–75**



ANSWERS

SECTION REVIEWS

SECTION 2–1 Half-Wave Rectifiers

1. PIV across the diode occurs at the peak of the input when the diode is reversed biased.
2. There is current through the load for approximately half (50%) of the input cycle.
3. The average value is $10\ V/\pi = 3.18\ V$.
4. The peak output voltage is $25\ V - 0.7\ V = 24.3\ V$.
5. The PIV must be at least 50 V.

SECTION 2–2 Full-Wave Rectifiers

1. A full-wave voltage occurs on each half of the input cycle and has a frequency of twice the input frequency. A half-wave voltage occurs once each input cycle and has a frequency equal to the input frequency.
2. The average value of $2(60\ V)/\pi = 38.12\ V$
3. The bridge rectifier has the greater output voltage.
4. The 50 V diodes must be used in the bridge rectifier.
5. In the center-tapped rectifier, diodes with a PIV rating of at least 90 V would be required.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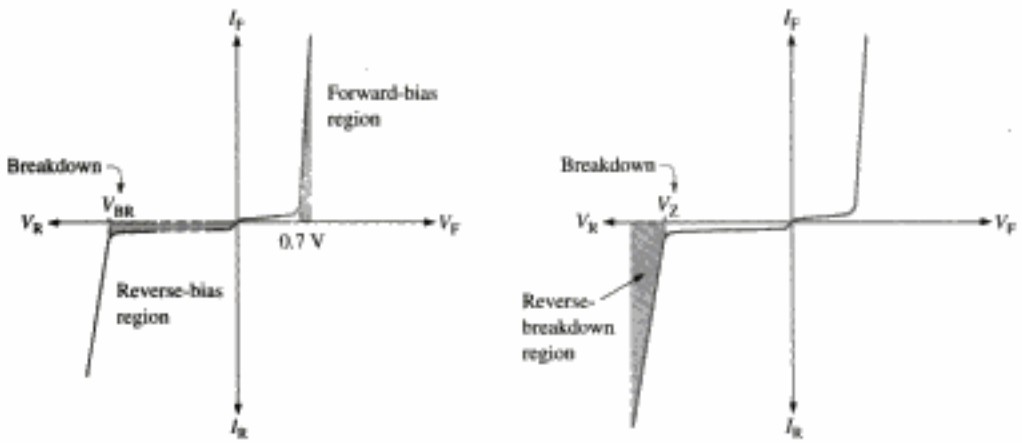
3–1 ZENER DIODES

A major application for zener diodes is as a type of voltage regulator for providing stable reference voltages for use in power supplies, voltmeters, and other instruments. In this section, you will see how the zener diode maintains a nearly constant dc voltage under the proper operating conditions. You will learn the conditions and limitations for properly using the zener diode and the factors that affect its performance.

▲ **FIGURE 3–1**

Zener diode symbol.

The symbol for a zener diode is shown in Figure 3–1. A **zener diode** is a silicon *pn* junction device that is designed for operation in the reverse-breakdown region. The breakdown voltage of a zener diode is set by carefully controlling the doping level during manufacture. Recall, that when a diode reaches reverse breakdown, its voltage remains almost constant even though the current changes drastically. This volt-ampere characteristic is shown again in Figure 3–2 with normal operating regions for rectifier diodes and for zener diodes shown as shaded areas. If a zener diode is forward-biased, it operates the same as a rectifier diode.



(a) The normal operating regions for a rectifier diode are shown as shaded areas.

(b) The normal operating region for a zener diode is shaded.

▲ **FIGURE 3–2**

General diode *V-I* characteristic.

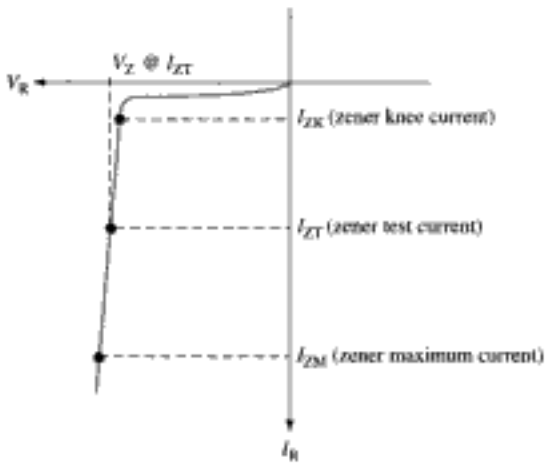
Zener Breakdown

Zener diodes are designed to operate in reverse breakdown. There are two types of reverse breakdown in a zener diode: *avalanche* and *zener*. The avalanche breakdown occurs in both rectifier and zener diodes at a sufficiently high reverse voltage. **Zener breakdown** occurs in a zener diode at low reverse voltages. A zener diode is heavily doped to reduce the breakdown voltage. This causes a very thin depletion region. As a result, an intense electric field exists within the depletion region. Near the zener breakdown voltage (V_Z), the field is intense enough to pull electrons from their valence bands and create current.

Zener diodes with breakdown voltages of less than approximately 5 V operate predominately in zener breakdown. Those with breakdown voltages greater than approximately 5 V operate predominantly in **avalanche breakdown**. Both types, however, are called *zener diodes*. Zeners are commercially available with breakdown voltages of 1.8 V to 200 V with specified tolerances from 1% to 20%.

Breakdown Characteristics

Figure 3–3 shows the reverse portion of a zener diode's characteristic curve. As the reverse voltage (V_R) is increased, the reverse current (I_R) remains extremely small up to the "knee" of the curve. The reverse current is also called the zener current, I_Z. At this point, the breakdown effect begins; the internal zener resistance, also called zener impedance (Z_Z), begins to decrease as the reverse current increases rapidly. From the bottom of the knee, the zener breakdown voltage (V_Z) remains essentially constant although it increases slightly as the zener current, I_Z, increases.



◀ FIGURE 3–3

Reverse characteristic of a zener diode. V_Z is usually specified at the zener test current, I_{ZT}, and is designated V_{ZT}.

Zener Regulation The ability to keep the reverse voltage across its terminals essentially constant is the key feature of the zener diode. A zener diode operating in breakdown acts as a voltage regulator because it maintains a nearly constant voltage across its terminals over a specified range of reverse-current values.

A minimum value of reverse current, I_{ZK}, must be maintained in order to keep the diode in breakdown for voltage regulation. You can see on the curve in Figure 3–3 that when the reverse current is reduced below the knee of the curve, the voltage decreases drastically and regulation is lost. Also, there is a maximum current, I_{ZM}, above which the diode may be damaged due to excessive power dissipation. So, basically, the zener diode maintains a nearly constant voltage across its terminals for values of reverse current ranging from I_{ZK} to I_{ZM}. A nominal zener voltage, V_{ZT}, is usually specified on a data sheet at a value of reverse current called the *zener test current*, I_{ZT}.

Zener Equivalent Circuit

Figure 3–4(a) shows the ideal model of a zener diode in reverse breakdown. It has a constant voltage drop equal to the nominal zener voltage. This constant voltage drop is represented by a dc voltage source even though the zener diode does not actually produce an emf voltage. The dc source simply indicates that the effect of reverse breakdown is a constant voltage across the zener terminals.

Figure 3–4(b) represents the practical model of a zener diode, where the zener impedance (Z_Z) is included. Since the actual voltage curve is not ideally vertical, a change in zener current (ΔI_Z) produces a small change in zener voltage (ΔV_Z), as illustrated in Figure 3–4(c). By Ohm's law, the ratio of ΔV_Z to ΔI_Z is the impedance, as expressed in the following equation:

$$Z_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

Equation 3–1

Normally, Z_Z is specified at I_{ZT}, the zener test current, and is designated Z_{ZT}. In most cases, you can assume that Z_Z is constant over the full linear range of zener current values and is purely resistive.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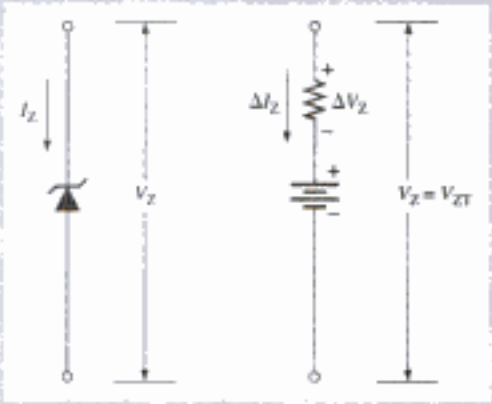
EXAMPLE 3–2

A 1N4736 zener diode has a Z_{ZT} of 3.5 Ω. The data sheet gives $V_{ZT} = 6.8$ V at $I_{ZT} = 37$ mA and $I_{ZK} = 1$ mA. What is the voltage across the zener terminals when the current is 50 mA? When the current is 25 mA? Figure 3–6 represents the zener diode.

▶ **FIGURE 3–6**



Solution For $I_Z = 50$ mA: The 50 mA current is a 13 mA increase above $I_{ZT} = 37$ mA.

$$\Delta I_Z = I_Z - I_{ZT} = +13 \text{ mA}$$
$$\Delta V_Z = \Delta I_Z Z_{ZT} = (13 \text{ mA})(3.5\ \Omega) = +45.5 \text{ mV}$$

The change in voltage due to the increase in current above the I_{ZT} value causes the zener terminal voltage to increase. The zener voltage for $I_Z = 50$ mA is

$$V_Z = 6.8 \text{ V} + \Delta V_Z = 6.8 \text{ V} + 45.5 \text{ mV} = \mathbf{6.85\ V}$$

For $I_Z = 25$ mA: The 25 mA current is a 12 mA decrease below $I_{ZT} = 37$ mA.

$$\Delta I_Z = -12 \text{ mA}$$
$$\Delta V_Z = \Delta I_Z Z_{ZT} = (-12 \text{ mA})(3.5\ \Omega) = -42 \text{ mV}$$

The change in voltage due to the decrease in current below I_{ZT} causes the zener terminal voltage to decrease. The zener voltage for $I_Z = 25$ mA is

$$V_Z = 6.8 \text{ V} - \Delta V_Z = 6.8 \text{ V} - 42 \text{ mV} = \mathbf{6.76\ V}$$

Temperature Coefficient

The temperature coefficient specifies the percent change in zener voltage for each degree centigrade change in temperature. For example, a 12 V zener diode with a positive temperature coefficient of 0.01%/°C will exhibit a 1.2 mV increase in V_Z when the junction temperature increases one degree centigrade. The formula for calculating the change in zener voltage for a given junction temperature change, for a specified temperature coefficient, is

$$\Delta V_Z = V_Z \times TC \times \Delta T \qquad \text{Equation 3–2}$$

where V_Z is the nominal zener voltage at 25°C, TC is the temperature coefficient, and ΔT is the change in temperature. A positive TC means that the zener voltage increases with an increase in temperature or decreases with a decrease in temperature. A negative TC means that the zener voltage decreases with an increase in temperature or increases with a decrease in temperature.

In some cases, the temperature coefficient is expressed in mV/°C rather than as %/°C. For these cases, ΔV_Z is calculated as

$$\Delta V_Z = TC \times \Delta T \qquad \text{Equation 3–3}$$

EXAMPLE 3–3

An 8.2 V zener diode (8.2 V at 25°C) has a positive temperature coefficient of 0.05%/°C. What is the zener voltage at 60°C?

Solution The change in zener voltage is

$$\Delta V_Z = V_Z \times TC \times \Delta T = (8.2\text{ V})(0.05\%/^\circ\text{C})(60^\circ\text{C} - 25^\circ\text{C})$$
$$= (8.2\text{ V})(0.0005/^\circ\text{C})(35^\circ\text{C}) = 144\text{ mV}$$

Notice that 0.05%/°C was converted to 0.0005/°C. The zener voltage at 60°C is

$$V_Z + \Delta V_Z = 8.2\text{ V} + 144\text{ mV} = \mathbf{8.34\text{ V}}$$

Zener Power Dissipation and Derating

Zener diodes are specified to operate at a maximum power called the maximum dc power dissipation, $P_{D(max)}$. For example, the 1N746 zener is rated at a $P_{D(max)}$ of 500 mW and the 1N3305A is rated at a $P_{D(max)}$ of 50 W. The dc power dissipation is determined by the formula,

$$P_D = V_Z I_Z$$

Power Derating The maximum power dissipation of a zener diode is typically specified for temperatures at or below a certain value (50°C, for example). Above the specified temperature, the maximum power dissipation is reduced according to a derating factor. The derating factor is expressed in mW/°C. The maximum derated power can be determined with the following formula:

Equation 3–4

$$P_{D(derated)} = P_{D(max)} - (\text{mW}/^\circ\text{C})\Delta T$$

EXAMPLE 3–4

A certain zener diode has a maximum power rating of 400 mW at 50°C and a derating factor of 3.2 mW/°C. Determine the maximum power the zener can dissipate at a temperature of 90°C.

Solution

$$P_{D(derated)} = P_{D(max)} - (\text{mW}/^\circ\text{C})\Delta T$$
$$= 400\text{ mW} - (3.2\text{ mW}/^\circ\text{C})(90^\circ\text{C} - 50^\circ\text{C})$$
$$= 400\text{ mW} - 128\text{ mW} = \mathbf{272\text{ mW}}$$

SECTION 3–1 REVIEW

Answers are at the end of the chapter.

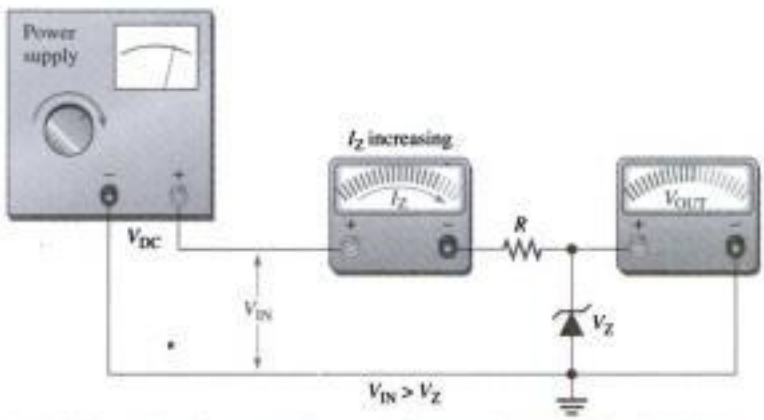
1. In what region of their characteristic curve are zener diodes operated?
2. At what value of zener current is the zener voltage normally specified?
3. How does the zener impedance affect the voltage across the terminals of the device?
4. For a certain zener diode, $V_Z = 10$ V at $I_{ZT} = 30$ mA. If $Z_Z = 8\ \Omega$, what is the terminal voltage at $I_Z = 50$ mA?
5. What does a positive temperature coefficient of 0.05%/°C mean?
6. Explain power derating.

3–2 ZENER DIODE APPLICATIONS

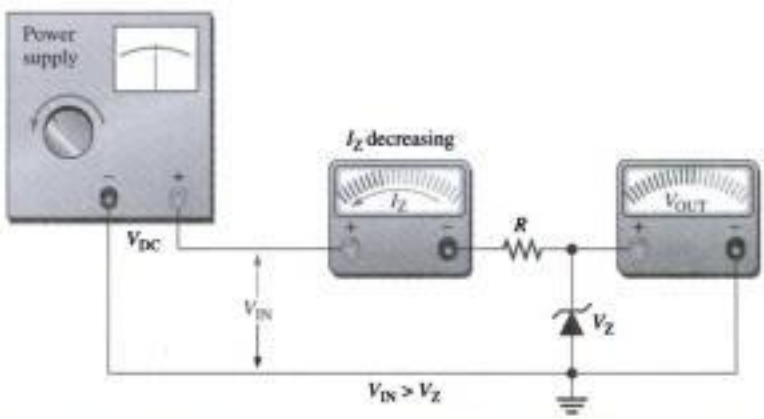
The zener diode can be used as a type of voltage regulator for providing stable reference voltages. In this section, you will see how zeners can be used as regulators and as simple limiters or clippers.

Zener Regulation with a Varying Input Voltage

Figure 3–7 illustrates how a zener diode can be used to regulate a varying dc voltage. As the input voltage varies (within limits), the zener diode maintains a nearly constant output voltage across its terminals. However, as V_{IN} changes, I_Z will change proportionally so that the limitations on the input voltage variation are set by the minimum and maximum current



(a) As the input voltage increases, the output voltage remains constant ($I_{ZK} < I_Z < I_{ZM}$).



(b) As the input voltage decreases, the output voltage remains constant ($I_{ZK} < I_Z < I_{ZM}$).

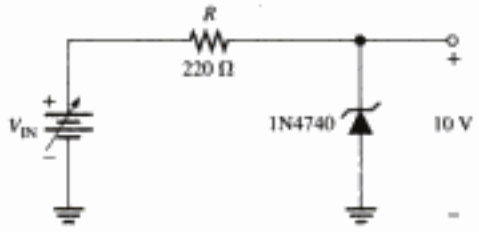
◀ **FIGURE 3–7**
Zener regulation of a varying input voltage.

values (I_{ZK} and I_{ZM}) with which the zener can operate. Resistor R is the series current-limiting resistor. The meters indicate the relative values and trends.

To illustrate regulation, suppose that the 1N4740 10 V zener diode in Figure 3–8 can maintain regulation over a range of zener current values from I_{ZK} = 0.25 mA to I_{ZM} = 100 mA. Let $P_{D(max)}$ = 1 W and V_Z = 10 V. (Figure 3–7)

$$I_{ZM} = \frac{P_{D(max)}}{V_Z} = \frac{1\text{ W}}{10\text{ V}} = 100\text{ mA}$$

► FIGURE 3–8



For the minimum zener current, the voltage across the 220 Ω resistor is

$$V_R = I_{ZK}R = (0.25\text{ mA})(220\ \Omega) = 55\text{ mV}$$

Since $V_R = V_{IN} - V_Z$,

$$V_{IN(min)} \cong V_R + V_Z = 55\text{ mV} + 10\text{ V} = 10.055\text{ V}$$

For the maximum zener current, the voltage across the 220 Ω resistor is

$$V_R = I_{ZM}R = (100\text{ mA})(220\ \Omega) = 22\text{ V}$$

Therefore,

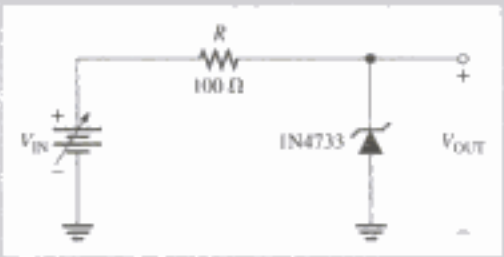
$$V_{IN(max)} \cong 22\text{ V} + 10\text{ V} = 32\text{ V}$$

This shows that this zener diode can regulate an input voltage from 10.055 V to 32 V and maintain an approximate 10 V output. The output will vary slightly because of the zener impedance, which has been neglected in these calculations.

EXAMPLE 3–5

Determine the minimum and the maximum input voltages that can be regulated by the zener diode in Figure 3–9.

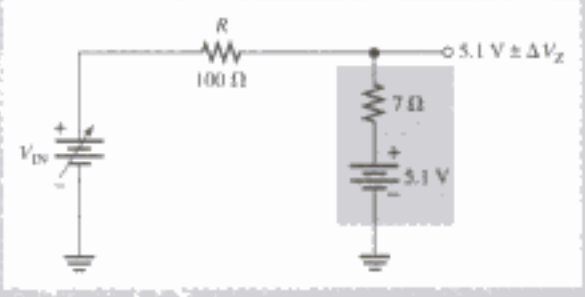
► FIGURE 3–9



Solution Let $V_Z = 5.1$ V at $I_{ZT} = 49$ mA, $I_{ZK} = 1$ mA, and $Z_Z = 7\ \Omega$ at I_{ZT}. For simplicity, assume this value of Z_Z over the range of current values. The equivalent circuit is shown in Figure 3–10.

► FIGURE 3–10

Equivalent of circuit in Figure 3–9.



At $I_{ZK} = 1$ mA, the output voltage is

$$V_{OUT} \cong 5.1\text{ V} - \Delta V_Z = 5.1\text{ V} - (I_{ZT} - I_{ZK})Z_Z$$
$$= 5.1\text{ V} - (48\text{ mA})(7\ \Omega) = 5.1\text{ V} - 0.336\text{ V} = 4.76\text{ V}$$

Therefore,

$$V_{IN(min)} = I_{ZK}R + V_{OUT} = (1\text{ mA})(100\ \Omega) + 4.76\text{ V} = \mathbf{4.86\text{ V}}$$

To find the maximum input voltage, first calculate the maximum zener current. Assume the temperature is 50°C or below the power dissipation is 1 W.

$$I_{ZM} = \frac{P_{D(max)}}{V_Z} = \frac{1\text{ W}}{5.1\text{ V}} = 196\text{ mA}$$

At I_{ZM}, the output voltage is

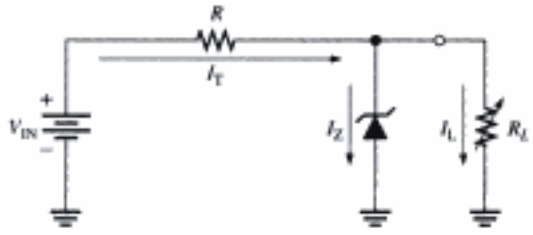
$$V_{OUT} \cong 5.1\text{ V} + \Delta V_Z = 5.1\text{ V} + (I_{ZM} - I_{ZT})Z_Z$$
$$= 5.1\text{ V} + (147\text{ mA})(7\ \Omega) = 5.1\text{ V} + 1.03\text{ V} = 6.13\text{ V}$$

Therefore,

$$V_{IN(max)} = I_{ZM}R + V_{OUT} = (196\text{ mA})(100\ \Omega) + 6.13\text{ V} = \mathbf{25.7\text{ V}}$$

Zener Regulation with a Variable Load

Figure 3–11 shows a zener voltage regulator with a variable load resistor across the terminals. The zener diode maintains a nearly constant voltage across R_L as long as the zener current is greater than I_{ZK} and less than I_{ZM}.



◀ FIGURE 3–11

Zener regulation with a variable load.

From No Load to Full Load

When the output terminals of the zener regulator are open ($R_L = \infty$), the load current is zero and *all* of the current is through the zener; this is a no-load condition. When a load resistor (R_L) is connected, part of the total current is through the zener and part through R_L. The total current through R remains essentially constant as long as the zener is regulating. As R_L is decreased, the load current, I_L, increases and I_Z decreases. The zener diode continues to regulate the voltage until I_Z reaches its minimum value, I_{ZK}. At this point the load current is maximum, and a full-load condition exists. The following example will illustrate this.

EXAMPLE 3–6

Determine the minimum and the maximum load currents for which the zener diode in Figure 3–12 will maintain regulation. What is the minimum value of R_L that can be used? $V_Z = 12$ V, $I_{ZK} = 1$ mA, and $I_{ZM} = 50$ mA. Assume $Z_Z = 0\ \Omega$ and V_Z remains a constant 12 V over the range of current values, for simplicity.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Solution First, review Example 3–6. The 1N4744 zener used in the regulator circuit of Figure 3–13 is a 15 V diode. Let $V_Z = 15\text{ V}$ @ I_{ZT}, $I_{ZK} = 0.25\text{ mA}$, $I_{ZT} = 17\text{ mA}$, and $Z_{ZT} = 14\ \Omega$.

(a) For I_{ZK}:

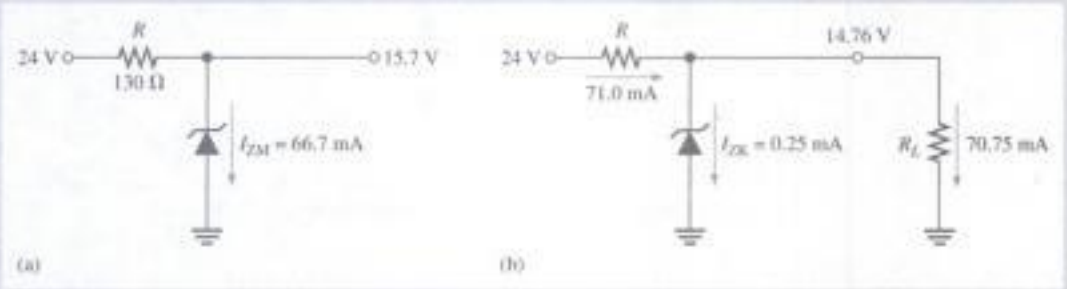
$$V_{OUT} = V_Z = 15\text{ V} - \Delta I_Z Z_{ZT} = 15\text{ V} - (I_{ZT} - I_{ZK})Z_{ZT}$$
$$= 15\text{ V} - (16.75\text{ mA})(14\ \Omega) = 15\text{ V} - 0.235\text{ V} = \mathbf{14.76\text{ V}}$$

Calculate the zener maximum current. The power dissipation is 1 W.

$$I_{ZM} = \frac{P_{D(max)}}{V_Z} = \frac{1\text{ W}}{15\text{ V}} = 66.7\text{ mA}$$

For I_{ZM}:

$$V_{OUT} = V_Z = 15\text{ V} + \Delta I_Z Z_{ZT}$$
$$= 15\text{ V} + (I_{ZM} - I_{ZT})Z_{ZT} = 15\text{ V} + (49.7\text{ mA})(14\ \Omega) = \mathbf{15.7\text{ V}}$$



▲ **FIGURE 3–14**

(b) Calculate the value of R for the maximum zener current that occurs when there is no load as shown in Figure 3–14(a).

$$R = \frac{V_{IN} - V_Z}{I_{ZM}} = \frac{24\text{ V} - 15.7\text{ V}}{66.7\text{ mA}} = 124\ \Omega$$

$R = \mathbf{130\ \Omega}$ (nearest larger standard value).

(c) For the minimum load resistance (maximum load current), the zener current is minimum ($I_{ZK} = 0.25\text{ mA}$) as shown in Figure 3–14(b).

$$I_T = \frac{V_{IN} - V_{OUT}}{R} = \frac{24\text{ V} - 14.76\text{ V}}{130\ \Omega} = 71.0\text{ mA}$$
$$I_L = I_T - I_{ZK} = 71.0\text{ mA} - 0.25\text{ mA} = 70.75\text{ mA}$$
$$R_{L(min)} = \frac{V_{OUT}}{I_L} = \frac{14.76\text{ V}}{70.75\text{ mA}} = \mathbf{209\ \Omega}$$

Zener Limiting

In addition to voltage regulation applications, zener diodes can be used in ac applications to limit voltage swings to desired levels. Figure 3–15 shows three basic ways the limiting action of a zener diode can be used. Part (a) shows a zener used to limit the positive peak of a signal voltage to the selected zener voltage. During the negative alternation, the zener acts as a forward-biased diode and limits the negative voltage to −0.7 V. When the zener is turned around, as in part (b), the negative peak is limited by zener action and the positive voltage is limited to +0.7 V. Two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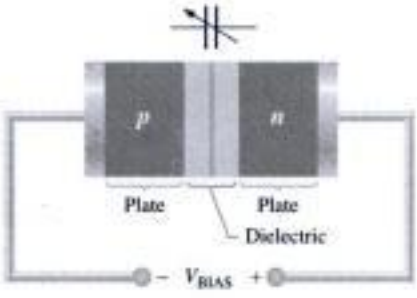
SECTION 3–2 REVIEW

1. In a zener diode regulator, what value of load resistance results in the maximum zener current?
2. Explain the terms *no-load* and *full-load*.
3. How much voltage appears across a zener diode when it is forward-biased?

3–3 VARACTOR DIODES

Varactor diodes are also known as variable-capacitance diodes because the junction capacitance varies with the amount of reverse-bias voltage. Varactor diodes are specifically designed to take advantage of this variable-capacitance characteristic. These devices are commonly used in electronic tuning circuits used in communications systems.

A **varactor** is a diode that always operates in reverse-bias and is doped to maximize the inherent capacitance of the depletion region. The depletion region, widened by the reverse bias, acts as a capacitor dielectric because of its nonconductive characteristic. The *p* and *n* regions are conductive and act as the capacitor plates, as illustrated in Figure 3–18.

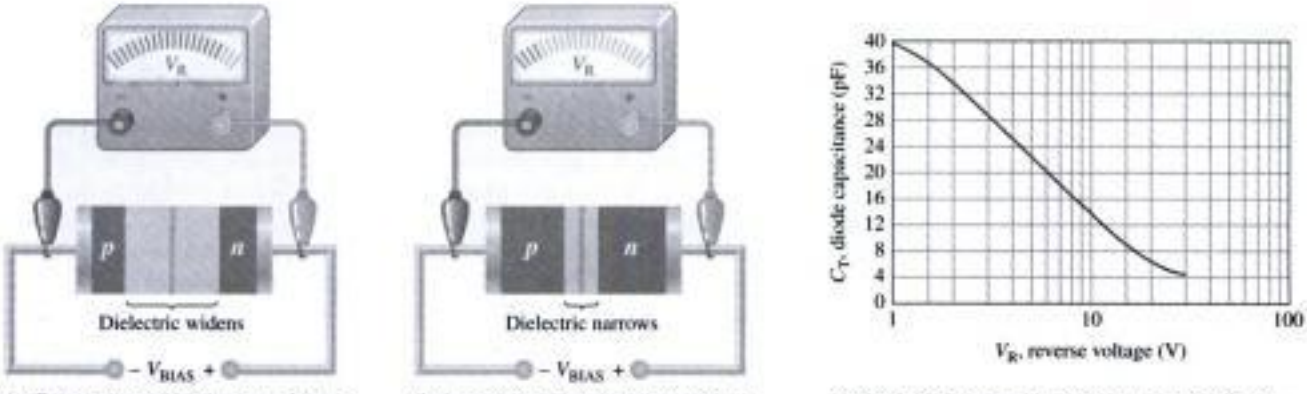


◄ FIGURE 3–18

The reverse-biased varactor diode acts as a variable capacitor.

Basic Operation

As the reverse-bias voltage increases, the depletion region widens, effectively increasing the plate separation and the dielectric thickness and thus decreasing the capacitance. When the reverse-bias voltage decreases, the depletion region narrows, thus increasing the capacitance. This action is shown in Figure 3–19(a) and (b). A graph of diode



(a) Greater reverse bias, less capacitance (b) Less reverse bias, greater capacitance (c) Graph of diode capacitance versus reverse voltage

▲ FIGURE 3–19

Varactor diode capacitance varies with reverse voltage.

▲ FIGURE 3–20
Varactor diode symbol.

capacitance (C_T) versus reverse voltage for a certain varactor is shown in Figure 3–19(c). For this particular device, C_T varies from 40 pF to slightly greater than 4 pF as V_R varies from 1 V to 40 V.

Recall that capacitance is determined by the parameters of plate area (A), dielectric constant (ϵ), and dielectric thickness (d), as expressed in the following formula:

$$C = \frac{A\epsilon}{d}$$

In a varactor diode, these capacitance parameters are controlled by the method of doping near the *pn* junction and the size and geometry of the diode's construction. Nominal varactor capacitances are typically available from a few picofarads to several hundred picofarads. Figure 3–20 shows a common symbol for a varactor.

SECTION 3–3 REVIEW

1. What is the key feature of a varactor diode?
2. Under what bias condition is a varactor operated?
3. What part of the varactor produces the capacitance?
4. Based on the graph in Figure 3–22(b), what happens to the diode capacitance when the reverse voltage is increased?
5. Define *tuning ratio*.

3–4 OPTICAL DIODES

In this section, two types of optoelectronic devices—the light-emitting diode (LED) and the photodiode—are introduced. As the name implies, the LED is a light emitter. The photodiode, on the other hand, is a light detector. We will examine the characteristics of both devices, and you will see an example of their use in a system application at the end of the chapter.

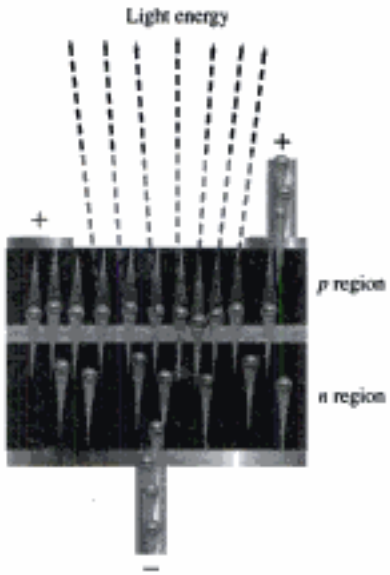
▲ FIGURE 3–21
Symbol for an LED. When forward-biased, it emits light.

The Light-Emitting Diode (LED)

The symbol for an LED is shown in Figure 3–21.

The basic operation of the **light-emitting diode (LED)** is as follows. When the device is forward-biased, electrons cross the *pn* junction from the *n*-type material and recombine with holes in the *p*-type material. These free electrons are in the conduction band and at a higher energy than the holes in the valence band. When recombination takes place, the recombining electrons release energy in the form of heat and light. A large exposed surface area on one layer of the semiconductive material permits the **photons** to be emitted as visible light. This process, called **electroluminescence**, is illustrated in Figure 3–22. Various impurities are added during the doping process to establish the wavelength of the emitted light. The wavelength determines the color of the light and if it is visible or **infrared** (IR).

LED Semiconductor Materials The semiconductor gallium arsenide (GaAs) was used in early LEDs. The first visible red LEDs were produced using gallium arsenide phosphide (GaAsP) on a GaAs substrate. The efficiency was increased using a gallium phosphide (GaP) substrate, resulting in brighter red LEDs and also allowing orange LEDs. GaAs LEDs emit infrared (IR) radiation, which is invisible.

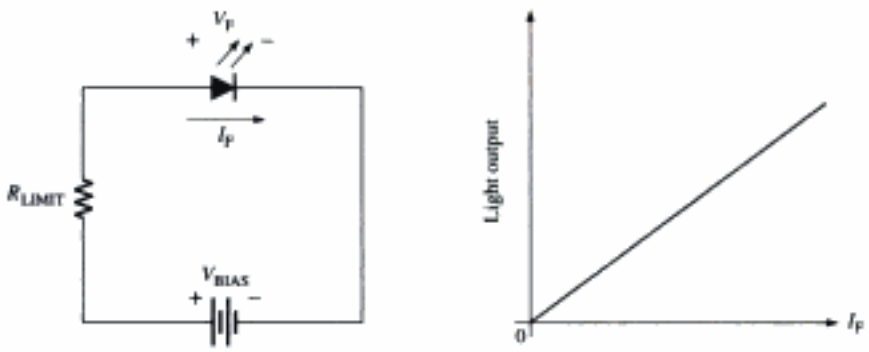


◀ **FIGURE 3–22**
Electroluminescence in a forward-biased LED.

Later, GaP was used as the light-emitter to achieve pale green light. By using a red and a green chip, LEDs were able to produce yellow light. The first super-bright red, yellow, and green LEDs were produced using gallium aluminum arsenide phosphide (GaAlAsP). By the early 1990s ultrabright LEDs using indium gallium aluminum phosphide (InGaAlP) were available in red, orange, yellow, and green.

Blue LEDs using silicon carbide (SiC) and ultrabright blue LEDs made of gallium nitride (GaN) became available. High intensity LEDs that produce green and blue are also made using indium gallium nitride (InGaN). High-intensity white LEDs are formed using ultrabright blue GaN coated with fluorescent phosphors that absorb the blue light and re-emit it as white light.

LED Biasing The forward voltage across an LED is considerably greater than for a silicon diode. Typically the maximum V_F for LEDs is between 1.2 V and 3.2 V, depending on the device. Reverse breakdown for an LED is much less than for a silicon rectifier diode (3 V to 10 V is typical).



(a) Forward-biased operation

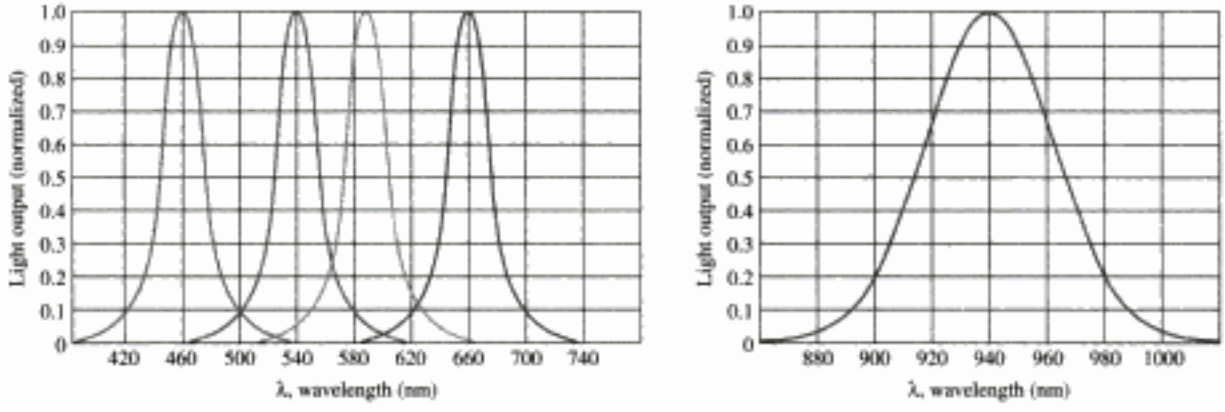
(b) General light output versus forward current

◀ **FIGURE 3–23**
Basic operation of an LED.

The LED emits light in response to a sufficient forward current, as shown in Figure 3–23(a). The amount of power output translated into light is directly proportional to the forward current, as indicated in Figure 3–23(b). An increase in I_F corresponds proportionally to an increase in light output.

Light Emission The **wavelength** of light determines whether it is visible or infrared. An LED emits light over a specified range of wavelengths as indicated by the **spectral** output

curves in Figure 3–24. The curves in part (a) represent the light output versus wavelength for typical visible LEDs, and the curve in part (b) is for a typical infrared LED. The wavelength (λ) is expressed in nanometers (nm). The normalized output of the visible red LED peaks at 660 nm, the yellow at 590 nm, green at 540 nm, and blue at 460 nm. The output for the infrared LED peaks at 940 nm.



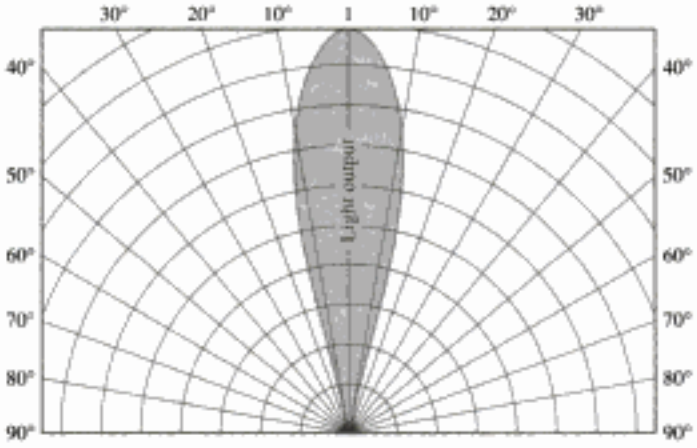
(a) Visible light (b) Infrared (IR)

▲ FIGURE 3–24

Examples of typical spectral output curves for LEDs.

▶ FIGURE 3–25

General radiation pattern of a typical LED.



The graph in Figure 3–25 is the **radiation** pattern for a typical LED. It shows how directional the emitted light is. The radiation pattern depends on the type of lens structure of the LED. The narrower the radiation pattern, the more the light is concentrated in a particular direction. Also, colored lenses are used to enhance the color.

Typical LEDs are shown in Figure 3–26. Photodiodes, to be studied next, generally have a similar appearance.

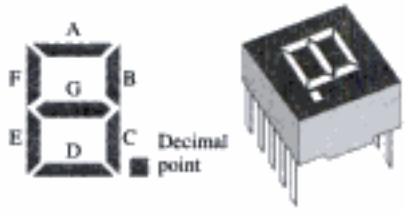
▶ FIGURE 3–26

Typical LEDs.

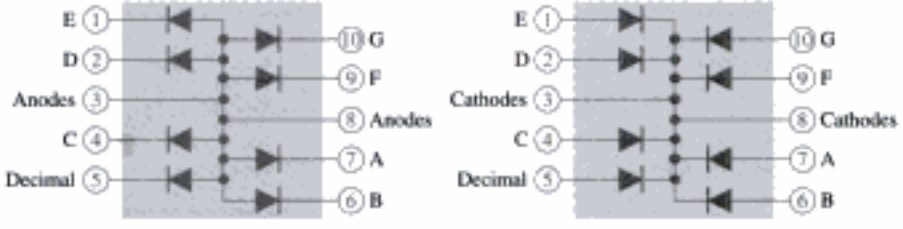
Cathode (lead on right looking from front) Anode (longer lead) Anode (lead near tab)

Applications Standard LEDs are used for indicator lamps and readout displays on a wide variety of instruments, ranging from consumer appliances to scientific apparatus. A common type of display device using LEDs is the seven-segment display. Combinations of the segments form the ten decimal digits as illustrated in Figure 3–27. Each segment in the display is an LED. By forward-biasing selected combinations of segments, any decimal digit and a decimal point can be formed. Two types of LED circuit arrangements are the common anode and common cathode as shown.

◀ **FIGURE 3–27**
The 7-segment LED display.



(a) LED segment arrangement and typical device



(b) Common anode (c) Common cathode

IR light-emitting diodes are used in optical coupling applications, often in conjunction with fiber optics. Areas of application include industrial processing and control, position encoders, bar graph readers, and optical switching.

High-Intensity LEDs

LEDs come in a variety of colors, and they are available in different light intensities. High-intensity LEDs produce many times more light than do the standard LEDs and are found in a variety of applications. The large video screens that are seen everywhere from sports stadiums to banks and other commercial buildings are mostly constructed with high-intensity LEDs. The automotive industry plans to replace all incandescent bulbs, even headlights, with LEDs. Also, LEDs will play a significant role in home and office lighting in the future.

The Photodiode

The **photodiode** is a device that operates in reverse bias, as shown in Figure 3–28(a), where I_λ is the reverse current. The photodiode has a small transparent window that allows light to strike the *pn* junction. Some typical photodiodes are shown in Figure 3–28(b). An alternate photodiode symbol is shown in Figure 3–28(c).

When reverse-biased, a rectifier diode has a very small reverse leakage current. The same is true for a photodiode. The reverse-biased current is produced by thermally generated

◀ **FIGURE 3–28**
Photodiode.

(a) Reverse-bias operation (b) Typical devices (c) Alternate symbol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These calculations show that the photodiode can be used as a variable-resistance device controlled by light intensity.

Figure 3–30 illustrates that the photodiode allows essentially no reverse current (except for a very small dark current) when there is no incident light. When a light beam strikes the photodiode, it conducts an amount of reverse current that is proportional to the light intensity (irradiance).

SECTION 3–4 REVIEW

1. Name two types of LEDs in terms of their light-emission spectrum.
2. Which has the greater wavelength, visible light or infrared?
3. In what bias condition is an LED normally operated?
4. What happens to the light emission of an LED as the forward current increases?
5. The forward voltage drop of an LED is 0.7 V. (true or false)
6. In what bias condition is a photodiode normally operated?
7. When the intensity of the incident light (irradiance) on a photodiode increases, what happens to its internal reverse resistance?
8. What is *dark current*?

3–5 OTHER TYPES OF DIODES

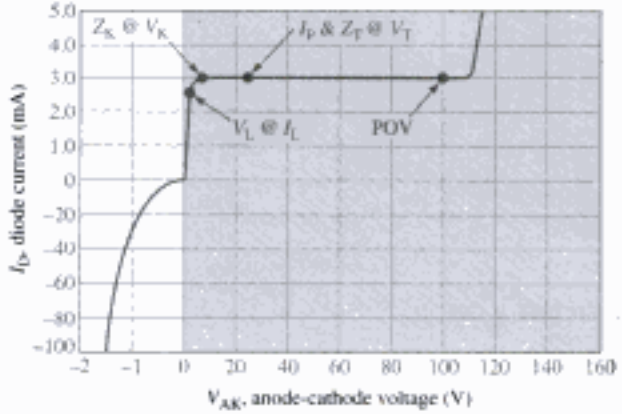
In this section, several types of diodes that you are less likely to encounter but are nevertheless important are introduced. Among these are the current regulator diode, the Schottky diode, the *pin* diode, the step-recovery diode, the tunnel diode, and the laser diode.

Current Regulator Diode

The current regulator diode is often referred to as a constant-current diode. Rather than maintaining a constant voltage, as the zener diode does, this diode maintains a constant current. The symbol is shown in Figure 3–31.

◀ FIGURE 3–31
Symbol for a current regulator diode.

Figure 3–32 shows a typical characteristic curve. The current regulator diode operates in forward bias (shaded region), and the forward current becomes a specified constant value at forward voltages ranging from about 1.5 V to about 6 V, depending on the diode type. The constant forward current is called the *regulator current* and is designated I_P. For



◀ FIGURE 3–32
Typical characteristic curve for a current regulator diode.

example, the 1N5283–1N5314 series of diodes have nominal regulator currents ranging from 220 μA to 4.7 mA. These diodes may be used in parallel to obtain higher currents. This diode does not have a sharply defined reverse breakdown, so the reverse current begins to increase for V_{AK} values of less than 0 V (unshaded region of the figure). This device should never be operated in reverse bias.

In forward bias, the diode regulation begins at the limiting voltage, V_L, and extends up to the POV (peak operating voltage). Between V_K and POV, the current is essentially constant. V_T is the test voltage at which I_P and the diode impedance, Z_T, are specified on a data sheet. The impedance Z_T has very high values ranging from 235 kΩ to 25 MΩ for the diode series mentioned before.

The Schottky Diode

▲ **FIGURE 3–33**

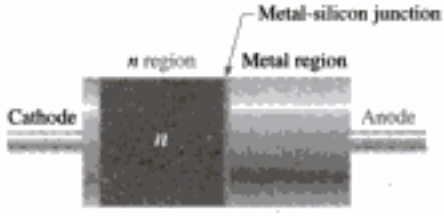
Schottky diode symbol.

Schottky diodes are used primarily in high-frequency and fast-switching applications. They are also known as *hot-carrier diodes*. A Schottky diode symbol is shown in Figure 3–33. A Schottky diode is formed by joining a doped semiconductor region (usually *n*-type) with a metal such as gold, silver, or platinum. Rather than a *pn* junction, there is a metal-to-semiconductor junction, as shown in Figure 3–34. The forward voltage drop is typically around 0.3 V.

The Schottky diode operates only with majority carriers. There are no minority carriers and thus no reverse leakage current as in other types of diodes. The metal region is heavily occupied with conduction-band electrons, and the *n*-type semiconductor region is lightly doped. When forward-biased, the higher energy electrons in the *n* region are injected into the metal region where they give up their excess energy very rapidly. Since there are no minority carriers, as in a conventional rectifier diode, there is a very rapid response to a change in bias. The Schottky is a fast-switching diode, and most of its applications make use of this property. It can be used in high-frequency applications and in many digital circuits to decrease switching times.

▶ **FIGURE 3–34**

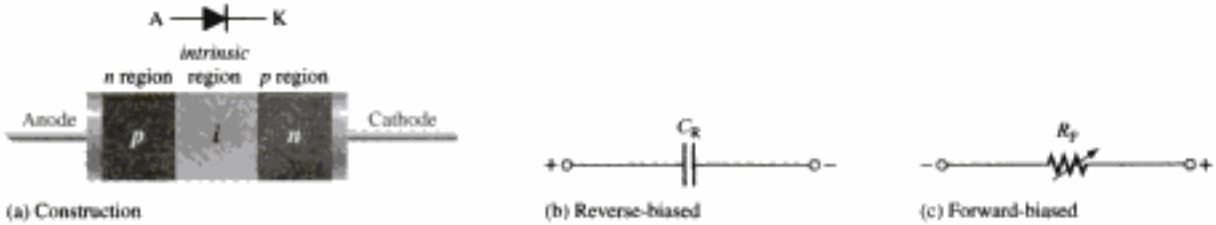
Basic internal construction of a Schottky diode.



The *PIN* Diode

The *pin* diode consists of heavily doped *p* and *n* regions separated by an intrinsic (*i*) region, as shown in Figure 3–35(a). When reverse-biased, the *pin* diode acts like a nearly constant capacitance. When forward-biased, it acts like a current-controlled variable resistance. This is shown in Figure 3–35(b) and (c). The low forward resistance of the intrinsic region decreases with increasing current.

The forward series resistance characteristic and the reverse capacitance characteristic are shown graphically in Figure 3–36 for a typical *pin* diode.



(a) Construction (b) Reverse-biased (c) Forward-biased

▲ **FIGURE 3–35**

PIN diode.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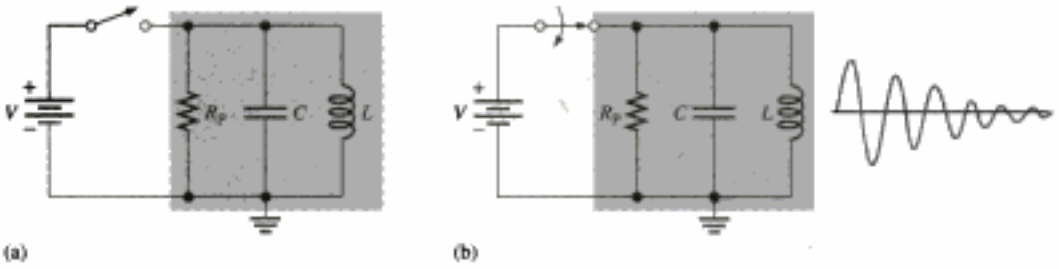
Also, the extremely narrow depletion region permits electrons to "tunnel" through the *pn* junction at very low forward-bias voltages, and the diode acts as a conductor. This is shown in Figure 3–38 between points *A* and *B*. At point *B*, the forward voltage begins to develop a barrier, and the current begins to decrease as the forward voltage continues to increase. This is the *negative-resistance region*.

$$R_F = \frac{\Delta V_F}{\Delta I_F}$$

This effect is opposite to that described in Ohm's law, where an increase in voltage results in an increase in current. At point *C*, the diode begins to act as a conventional forward-biased diode.

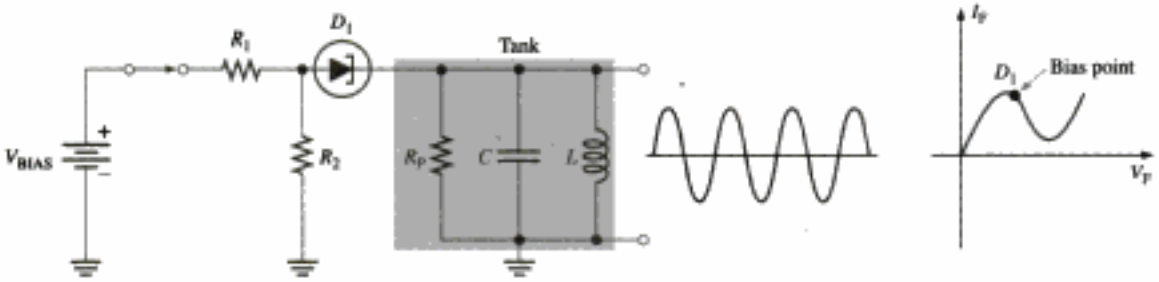
An Application A parallel resonant circuit can be represented by a capacitance, inductance, and resistance in parallel, as in Figure 3–39(a). R_P is the parallel equivalent of the series winding resistance of the coil. When the tank circuit is subjected to oscillation by an application of voltage as in Figure 3–39(b), a damped sinusoidal output results. The damping is due to the resistance of the tank, which prevents a sustained oscillation because energy is lost when there is current through the resistance.



▲ FIGURE 3–39

Parallel resonant circuit.

If a tunnel diode is placed in series with the tank circuit and biased at the centre of the negative-resistance portion of its characteristic curve, as shown in Figure 3–40, a sustained oscillation (constant sinusoidal voltage) will result on the output. This is because the negative-resistance characteristic of the tunnel diode counteracts the positive-resistance characteristic of the tank resistance.



▲ FIGURE 3–40

Basic tunnel diode oscillator.

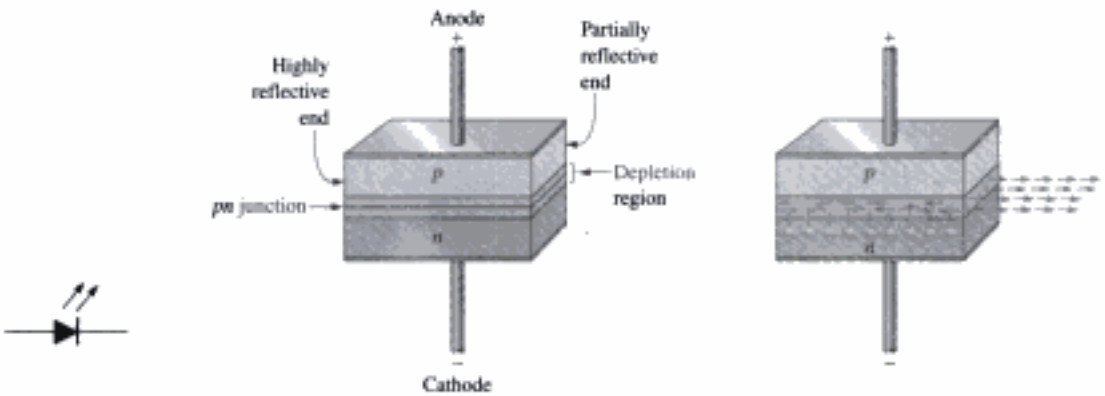
The Laser Diode

The term **laser** stands for *l*ight *a*mplification by *s*timulated *e*mission of *r*adiation. Laser light is **monochromatic**, which means that it consists of a single color and not a mixture of

colors. Laser light is also called **coherent light**, a single wavelength, as compared to incoherent light, which consists of a wide band of wavelengths. The laser diode normally emits coherent light, whereas the LED emits incoherent light. The symbols are the same as shown in Figure 3–41(a).

The basic construction of a laser diode is shown in Figure 3–41(b). A *pn* junction is formed by two layers of doped gallium arsenide. The length of the *pn* junction bears a precise relationship with the wavelength of the light to be emitted. There is a highly reflective surface at one end of the *pn* junction and a partially reflective surface at the other end produced by "polishing" the ends. External leads provide the anode and cathode connections.

The basic operation is as follows. The laser diode is forward-biased by an external voltage source. As electrons move through the junction, recombination occurs just as in an ordinary diode. As electrons fall into holes to recombine, photons are released. A released photon can strike an atom, causing another photon to be released. As the forward current is increased, more electrons enter the depletion region and cause more photons to be emitted. Eventually some of the photons that are randomly drifting within the depletion region strike the reflected surfaces perpendicularly. These reflected photons move along the depletion region, striking atoms and releasing additional photons due to the avalanche effect. This



▲ FIGURE 3–41

Basic laser diode construction and operation.

back-and-forth movement of photons increases as the generation of photons "snowballs" until a very intense beam of laser light is formed by the photons that pass through the partially reflective end of the *pn* junction.

Each photon produced in this process is identical to the other photons in energy level, phase relationship, and frequency. So a single wavelength of intense light emerges from the laser diode, as indicated in Figure 3–41(c). Laser diodes have a threshold level of current above which the laser action occurs and below which the diode behaves essentially as an LED, emitting incoherent light.

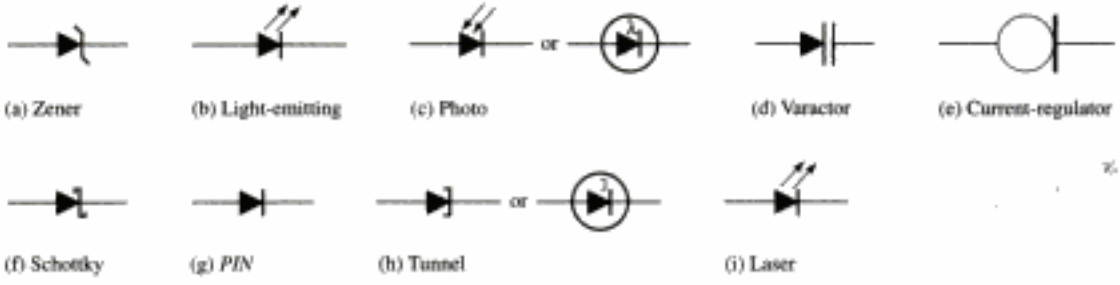
An Application Laser diodes and photodiodes are used in the pick-up system of compact disk (CD) players. Audio information (sound) is digitally recorded in stereo on the surface of a compact disk in the form of microscopic "pits" and "flats." A lens arrangement focuses the laser beam from the diode onto the CD surface. As the CD rotates, the lens and beam follow the track under control of a servomotor. The laser light, which is altered by the pits and flats along the recorded track, is reflected back from the track through a lens and optical system to infrared photodiodes. The signal from the photodiodes is then used to reproduce the digitally recorded sound.

SECTION 3–5 REVIEW

1. Between what two voltages does a current regulator diode operate?
2. What are the primary application areas for Schottky diodes?
3. What is a hot-carrier diode?
4. What is the key characteristic of a tunnel diode?
5. What is one application for a tunnel diode?
6. Name the three regions of a *pin* diode.
7. What does *laser* mean?
8. What is the difference between incoherent and coherent light and which is produced by a laser diode?

CHAPTER SUMMARY

- The zener diode operates in reverse breakdown.
- There are two breakdown mechanisms in a zener diode: avalanche breakdown and zener breakdown.
- When $V_Z < 5$ V, zener breakdown is predominant.
- When $V_Z > 5$ V, avalanche breakdown is predominant.
- A zener diode maintains a nearly constant voltage across its terminals over a specified range of zener currents.
- Zener diodes are used as voltage regulators and limiters.
- Zener diodes are available in many voltage ratings ranging from 1.8 V to 200 V.
- A varactor diode acts as a variable capacitor under reverse-bias conditions.
- The capacitance of a varactor varies inversely with reverse-bias voltage.
- The current regulator diode keeps its forward current at a constant specified value.
- The Schottky diode has a metal-to-semiconductor junction. It is used in fast-switching applications.
- The tunnel diode is used in oscillator circuits.
- An LED emits light when forward-biased.
- LEDs are available for either infrared or visible light.
- The photodiode exhibits an increase in reverse current with light intensity.
- The *pin* diode has a *p* region, an *n* region, and an intrinsic (*i*) region and displays a variable resistance characteristic when forward-biased and a constant capacitance when reverse-biased.
- A laser diode is similar to an LED except that it emits coherent (single wavelength) light when the forward current exceeds a threshold value.
- A summary of special-purpose diode symbols is given in Figure 3–42.



(a) Zener (b) Light-emitting (c) Photo (d) Varactor (e) Current-regulator

(f) Schottky (g) *PIN* (h) Tunnel (i) Laser

▲ FIGURE 3–42

Diode symbols.

OBJECTIVE TYPE QUESTIONS

Answers are at the end of the chapter.

1. If the input voltage in Figure 3–9 is increased from 5 V to 10 V, ideally the output voltage will

(a) increase **(b)** decrease **(c)** not change

2. If the input voltage in Figure 3–12 is reduced by 2 V, the zener current will

(a) increase **(b)** decrease **(c)** not change

3. If R_L in Figure 3–12 is removed, the current through the zener diode will

(a) increase **(b)** decrease **(c)** not change

4. If the zener opens in Figure 3–12, the output voltage will

(a) increase **(b)** decrease **(c)** not change

5. If R in Figure 3–12 is increased, the current to the load resistor will

(a) increase **(b)** decrease **(c)** not change

6. If the input voltage amplitude in Figure 3–15(a) is increased, the positive output voltage will

(a) increase **(b)** decrease **(c)** not change

7. If the input voltage amplitude in Figure 3–16(a) is reduced, the amplitude of the output voltage will

(a) increase **(b)** decrease **(c)** not change

8. If the bias voltage in Figure 3–23 is increased, the light output of the LED will

(a) increase **(b)** decrease **(c)** not change

9. If the bias voltage in Figure 3–23 is reversed, the light output of the LED will

(a) increase **(b)** decrease **(c)** not change

10. The cathode of a zener diode in a voltage regulator is normally

(a) more positive than the anode **(b)** more negative than the anode
(c) at +0.7 V **(d)** grounded

11. If a certain zener diode has a zener voltage of 3.6 V, it operates in

(a) regulated breakdown **(b)** zener breakdown
(c) forward conduction **(d)** avalanche breakdown

12. For a certain 12 V zener diode, a 10 mA change in zener current produces a 0.1 V change in zener voltage. The zener impedance for this current range is

(a) 1 Ω **(b)** 100 Ω **(c)** 10 Ω **(d)** 0.1 Ω

13. The data sheet for a particular zener gives $V_Z = 10$ V at $I_{ZT} = 500$ mA. Z_Z for these conditions is

(a) 50 Ω **(b)** 20 Ω **(c)** 10 Ω **(d)** unknown

14. A no-load condition means that

(a) the load has infinite resistance **(b)** the load has zero resistance
(c) the output terminals are open **(d)** answers (a) and (c)

15. A varactor diode exhibits

(a) a variable capacitance that depends on reverse voltage
(b) a variable resistance that depends on reverse voltage
(c) a variable capacitance that depends on forward current
(d) a constant capacitance over a range of reverse voltages

16. An LED

(a) emits light when reverse-biased
(b) senses light when reverse-biased
(c) emits light when forward-biased
(d) acts as a variable resistance

17. Compared to a visible red LED, an infrared LED
    (a) produces light with shorter wavelengths
    (b) produces light of all wavelengths
    (c) produces only one color of light
    (d) produces light with longer wavelengths
18. The internal resistance of a photodiode
    (a) increases with light intensity when reverse-biased
    (b) decreases with light intensity when reverse-biased
    (c) increases with light intensity when forward-biased
    (d) decreases with light intensity when forward-biased
19. A diode that has a negative resistance characteristic is the
    (a) Schottky diode (b) tunnel diode
    (c) laser diode (d) hot-carrier diode
20. An infrared LED is optically coupled to a photodiode. When the LED is turned off, the reading on an ammeter in series with the reverse-biased photodiode will
    (a) not change (b) decrease (c) increase (d) fluctuate
21. In order for a system to function properly, the various types of circuits that make up the system must be
    (a) properly biased (b) properly connected
    (c) properly interfaced (d) all of the above
    (e) answers (a) and (b)

PROBLEMS

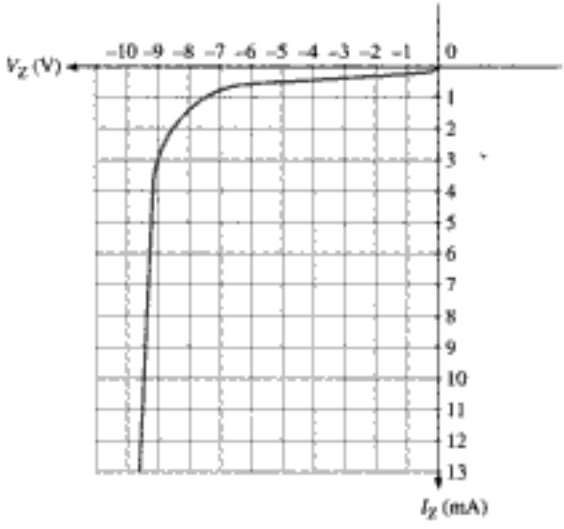
Answers to all selected problems at the end of the book.

BASIC PROBLEMS

SECTION 3–1 Zener Diodes

1. A certain zener diode has a $V_Z = 7.5$ V and an $Z_Z = 5\ \Omega$ at a certain current. Draw the equivalent circuit.
2. From the characteristic curve in Figure 3–43, what is the approximate minimum zener current (I_{ZK}) and the approximate zener voltage at I_{ZK}?

► FIGURE 3–43

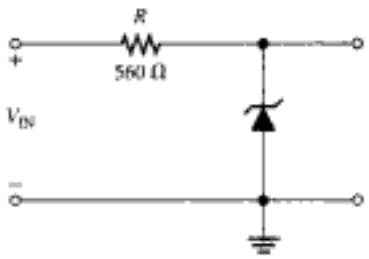


3. When the reverse current in a particular zener diode increases from 20 mA to 30 mA, the zener voltage changes from 5.6 V to 5.65 V. What is the impedance of this device?
4. A zener has an impedance of 15 Ω. What is its terminal voltage at 50 mA if $V_{ZT} = 4.7$ V at $I_{ZT} = 25$ mA?
5. A certain zener diode has the following specifications: $V_Z = 6.8$ V at 25°C and $TC = +0.04\%/°C$. Determine the zener voltage at 70°C.

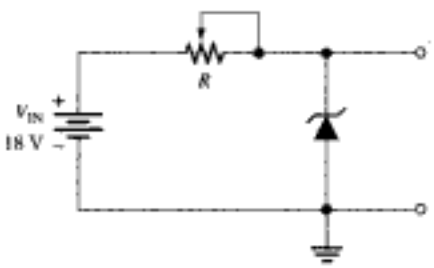
SECTION 3–2 Zener Diode Applications

6. Determine the minimum input voltage required for regulation to be established in Figure 3–44. Assume an ideal zener diode with $I_{ZK} = 1.5$ mA and $V_Z = 14$ V.

▶ FIGURE 3–44

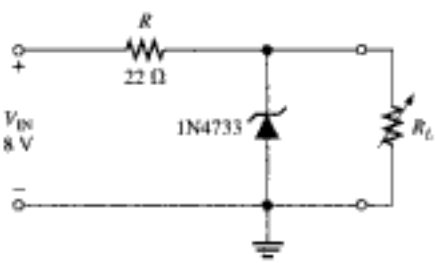


7. Repeat Problem 6 with $Z_Z = 20\ \Omega$ and $V_{ZT} = 14$ V at 30 mA.
8. To what value must R be adjusted in Figure 3–45 to make $I_Z = 40$ mA? Assume $V_Z = 12$ V at 30 mA and $Z_Z = 30\ \Omega$.
9. A 20 V peak sinusoidal voltage is applied to the circuit in Figure 3–45 in place of the dc source. Draw the output waveform. Use the parameter values established in Problem 8.



◀ FIGURE 3–45

10. A loaded zener regulator is shown in Figure 3–46. $V_Z = 5.1$ V at $I_{ZT} = 49$ mA, $I_{ZK} = 1$ mA, $Z_Z = 7\ \Omega$, and $I_{ZM} = 70$ mA. Determine the minimum and maximum permissible load currents.
11. Find the load regulation expressed as a percentage in Problem 10. Refer to Chapter 2, Equation 2–16.
12. Analyze the circuit in Figure 3–46 for percent line regulation using an input voltage from 6 V to 12 V with no load. Refer to Chapter 2, Equation 2–15.



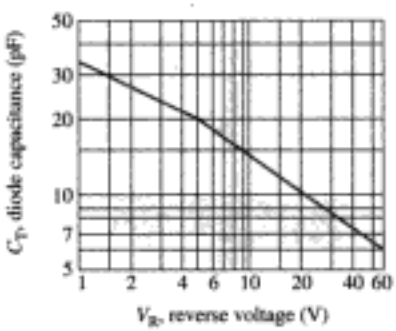
◀ FIGURE 3–46

13. The no-load output voltage of a certain zener regulator is 8.23 V, and the full-load output is 7.98 V. Calculate the load regulation expressed as a percentage. Refer to Chapter 2, Equation 2–16.
14. In a certain zener regulator, the output voltage changes 0.2 V when the input voltage goes from 5 V to 10 V. What is the input regulation expressed as a percentage? Refer to Chapter 2, Equation 2–15.
15. The output voltage of a zener regulator is 3.6 V at no load and 3.4 V at full load. Determine the load regulation expressed as a percentage. Refer to Chapter 2, Equation 2–16.

SECTION 3–3 Varactor Diodes

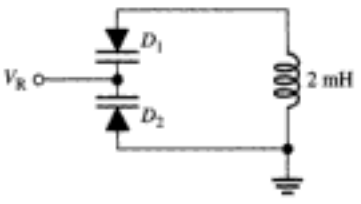
16. Figure 3–47 is a curve of reverse voltage versus capacitance for a certain varactor. Determine the change in capacitance if V_R varies from 5 V to 20 V.
17. Refer to Figure 3–47 and determine the value of V_R that produces 25 pF.

► FIGURE 3–47



18. What capacitance value is required for each of the varactors in Figure 3–48 to produce a resonant frequency of 1 MHz?
19. At what value must the voltage V_R be set in Problem 18 if the varactors have the characteristic curve in Figure 3–47?

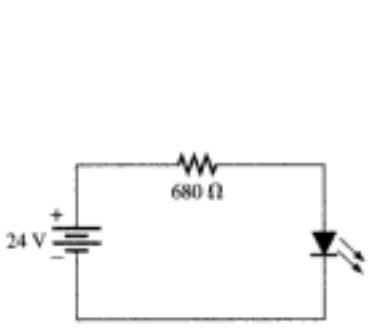
► FIGURE 3–48



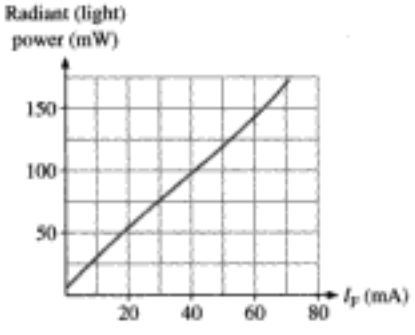
SECTION 3–4 Optical Diodes

20. The LED in Figure 3–49(a) has a light-producing characteristic as shown in part (b). Neglecting the forward voltage drop of the LED, determine the amount of radiant (light) power produced in mW.

► FIGURE 3–49



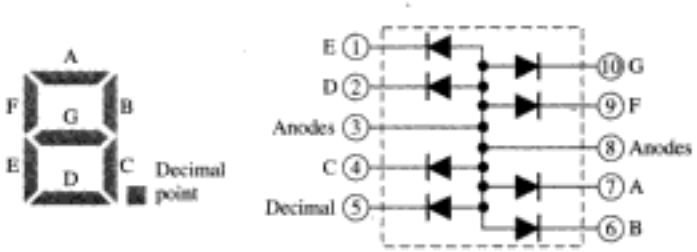
(a)



(b)

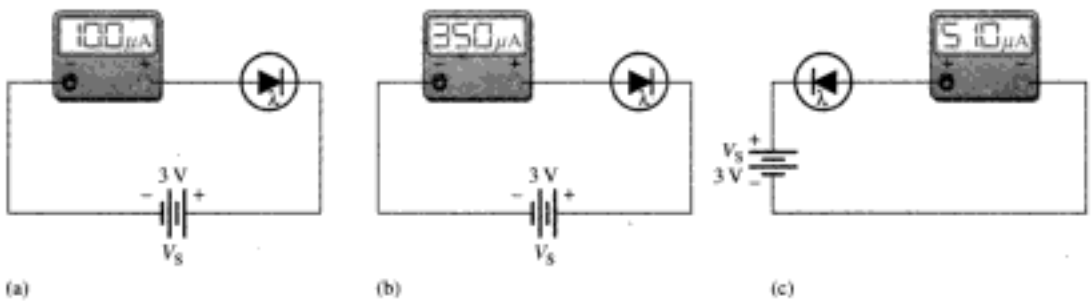
21. Determine how to connect the seven-segment display in Figure 3–50 to display "5." The maximum continuous forward current for each LED is 30 mA and a +5 V dc source is to be used.

▶ **FIGURE 3–50**



22. For a certain photodiode at a given irradiance, the reverse resistance is 200 kΩ and the reverse voltage is 10 V. What is the current through the device?

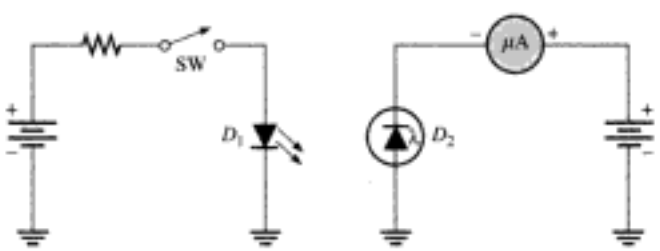
23. What is the resistance of each photodiode in Figure 3–51?



▲ **FIGURE 3–51**

24. When the switch in Figure 3–52 is closed, will the microammeter reading increase or decrease? Assume D_1 and D_2 are optically coupled.

▶ **FIGURE 3–52**



SECTION 3–5 Other Types of Diodes

25. The *V-I* characteristic of a certain tunnel diode shows that the current changes from 0.25 mA to 0.15 mA when the voltage changes from 125 mV to 200 mV. What is the resistance?

26. In what type of circuit are tunnel diodes commonly used?

27. What purpose do the reflective surfaces in the laser diode serve? Why is one end only partially reflective?

ANSWERS

SECTION REVIEWS

SECTION 3–1 Zener Diodes

1. Zener diodes are operated in the reverse-breakdown region.
2. The test current, I_{ZT}
3. The zener impedance causes the voltage to vary slightly with current.
4. $V_Z = 10\text{ V} + (20\text{ mA})(8\ \Omega) = 10.16\text{ V}$
5. The zener voltage increases (or decreases) 0.05% for each degree centigrade increase (or decrease).
6. Power derating is the reduction in the power rating of a device as a result of an increase in temperature.

SECTION 3–2 Zener Diode Applications

1. An infinite resistance (open)
2. With no load, there is no current to a load. With full load, there is maximum current to the load.
3. Approximately 0.7 V, just like a rectifier diode

SECTION 3–3 Varactor Diodes

1. A varactor exhibits variable capacitance.
2. A varactor is operated in reverse bias.
3. The depletion region
4. Capacitance decreases with more reverse bias.
5. The tuning ratio is the ratio of a varactor's capacitance at a specified minimum voltage to the capacitance at a specified maximum voltage.

SECTION 3–4 Optical Diodes

1. Infrared and visible light
2. Infrared has the greater wavelength.
3. An LED operates in forward bias.
4. Light emission increases with forward current.
5. False, V_F of an LED is usually greater than 1.2 V.
6. A photodiode operates in reverse bias.
7. The internal resistance decreases.
8. Dark current is the reverse photodiode current when there is no light.

SECTION 3–5 Other Types of Diodes

1. A current regulator operates between V_L (limiting voltage) and POV (peak operating voltage).
2. High-frequency and fast-switching circuits
3. *Hot carrier* is another name for Schottky diodes.
4. Tunnel diodes have negative resistance.
5. Oscillators
6. *p* region, *n* region, and intrinsic (*i*) region
7. *l*ight *a*mplification by *s*timulated *e*mission of *r*adiation
8. Coherent light has only a single wavelength, but incoherent light has a wide band of wavelengths. A laser diode produces coherent light.

OBJECTIVE TYPE QUESTIONS

1. (c)	**2.** (b)	**3.** (a)	**4.** (a)	**5.** (b)	**6.** (c)	**7.** (c)	**8.** (a)	**9.** (b)
10. (a)	**11.** (b)	**12.** (c)	**13.** (b)	**14.** (d)	**15.** (a)	**16.** (c)	**17.** (d)	**18.** (b)
19. (b)	**20.** (b)	**21.** (d)						

4

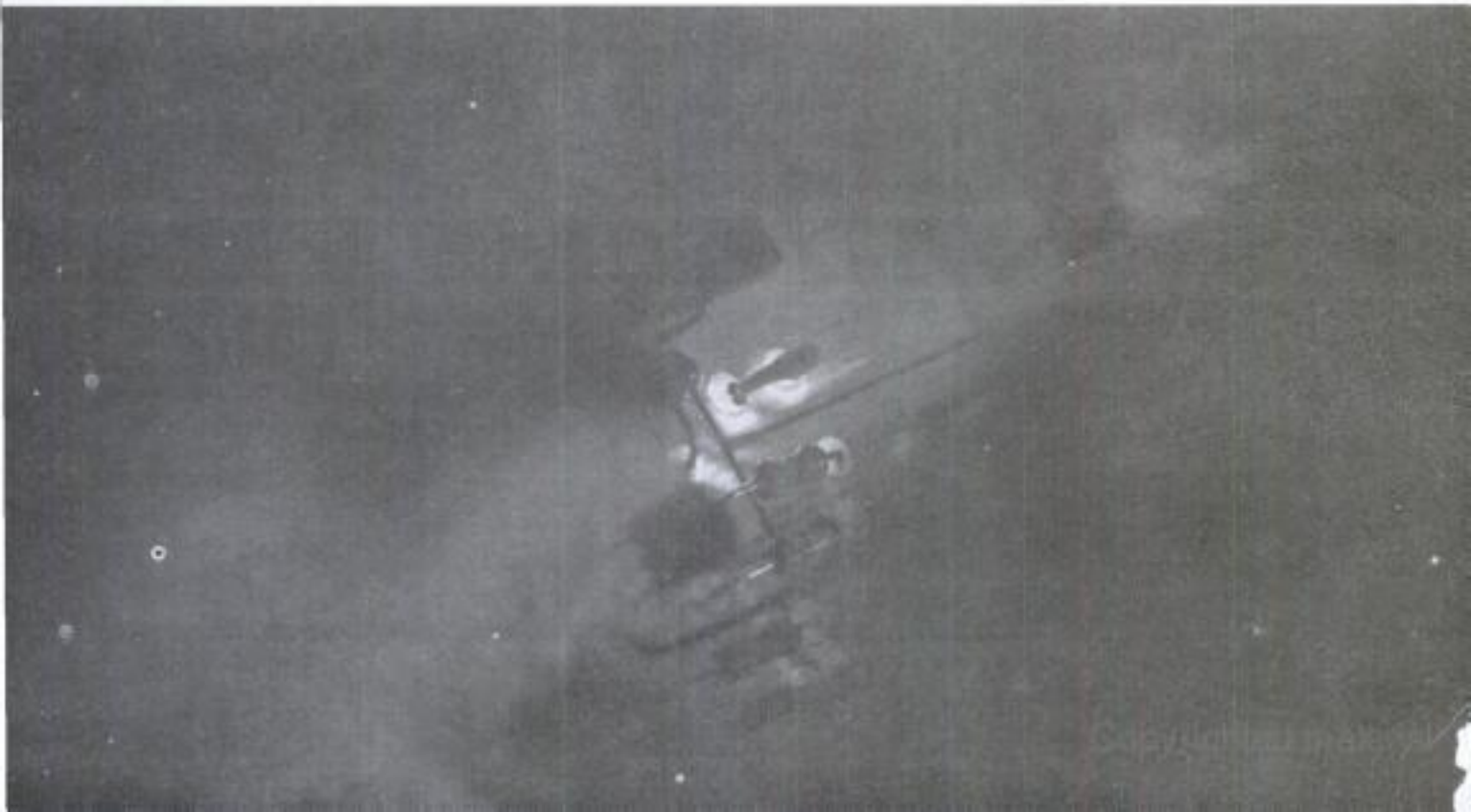
BIPOLAR JUNCTION TRANSISTORS (BJTs)

CHAPTER OUTLINE

INTRODUCTION

The transistor was invented by a team of three men at Bell Laboratories in 1947. Although this first transistor was not a bipolar junction device, it was the beginning of a technological revolution that is still continuing. All of the complex electronic devices and systems today are an outgrowth of early developments in semiconductor transistors.

Two basic types of transistors are the bipolar junction transistor (BJT), which we will begin to study in this chapter, and the field-effect transistor (FET), which we will cover in later chapters. The BJT is used in two broad areas—as a linear amplifier to boost or amplify an electrical signal and as an electronic switch. Both of these applications are introduced in this chapter.

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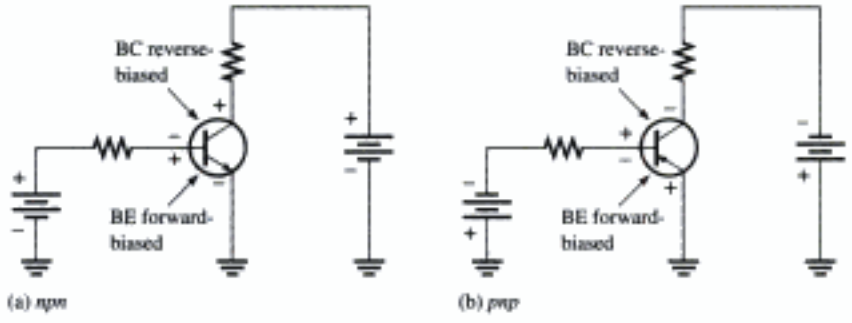
4–2 BASIC TRANSISTOR OPERATION

In order for the transistor to operate properly as an amplifier, the two *pn* junctions must be correctly biased with external dc voltages. In this section, we use the *npn* transistor for illustration. The operation of the *pnp* is the same as for the *npn* except that the roles of the electrons and holes, the bias voltage polarities, and the current directions are all reversed.



◀ **FIGURE 4–3**
Forward-reverse bias of junctions of a BJT.

Figure 4–3 shows the proper **bias** arrangement for both *npn* and *pnp* **transistors** for active operation as an **amplifier**. Notice that in both cases the base-emitter (BE) junction is forward-biased and the base-collector (BC) junction is reverse-biased.

To illustrate transistor action, let's examine what happens inside the *npn* transistor. The forward bias from base to emitter narrows the BE depletion region, and the reverse bias from base to collector widens the BC depletion region, as depicted in Figure 4–4. The heavily doped *n*-type emitter region is teeming with conduction-band (free) electrons that easily diffuse through the forward-biased BE junction into the *p*-type base region where they become minority carriers, just as in a forward-biased diode. The base region is lightly doped and very thin so that it has a limited number of holes. Thus, only a small percentage of all the electrons flowing through the BE junction can combine with the available holes in the base. These relatively few recombined electrons flow out of the base lead as valence electrons, forming the small base electron current, as shown in Figure 4–4.

Most of the electrons flowing from the emitter into the thin, lightly doped base region do not recombine but diffuse into the BC depletion region. Once in this region they are pulled through the reverse-biased BC junction by the electric field set up by the force of attraction between the positive and negative ions. Actually, you can think of the electrons as being pulled across the reverse-biased BC junction by the attraction of the collector supply voltage. The electrons now move through the collector region, out through the collector lead, and into the positive terminal of the collector voltage source. This forms the collector electron current, as shown in Figure 4–4. The collector current is much larger than the base current. This is the reason transistors exhibit current gain.

Transistor Currents

The directions of the currents in an *npn* transistor and its schematic symbol are as shown in Figure 4–5(a); those for a *pnp* transistor are shown in Figure 4–5(b). Notice that the arrow on the emitter of the transistor symbols points in the direction of conventional current. These diagrams show that the emitter current (I_E) is the sum of the collector current (I_C) and the base current (I_B), expressed as follows:

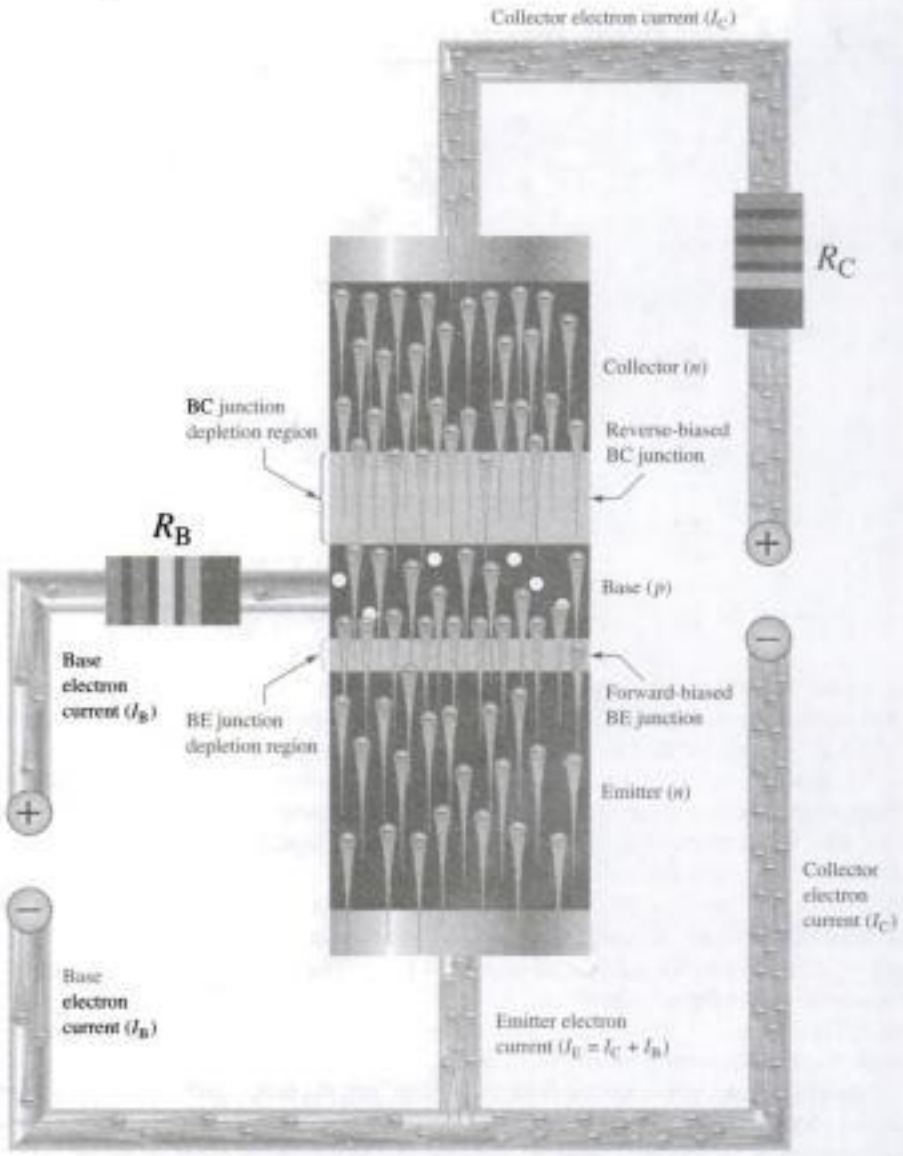
$$I_E = I_C + I_B$$

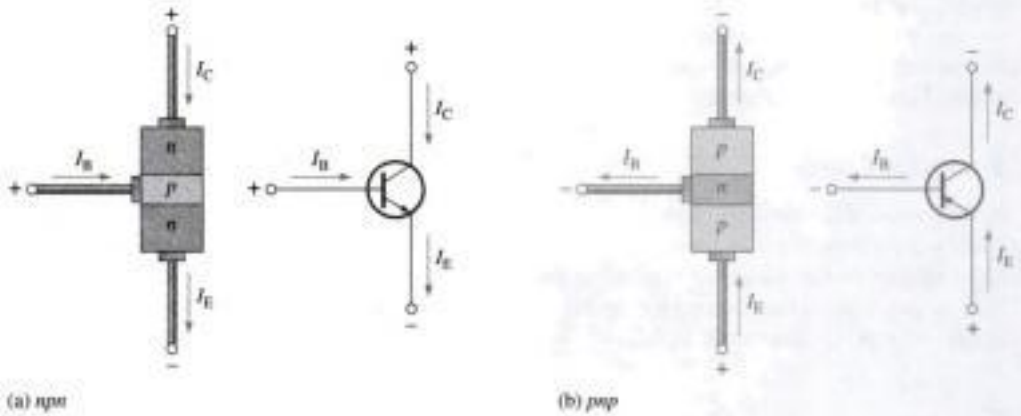
Equation 4–1

As mentioned before, I_B is very small compared to I_E or I_C. The capital-letter subscripts indicate dc values.

► **FIGURE 4–4**

Illustration of BJT action.





▲ **FIGURE 4–5**

Transistor currents.

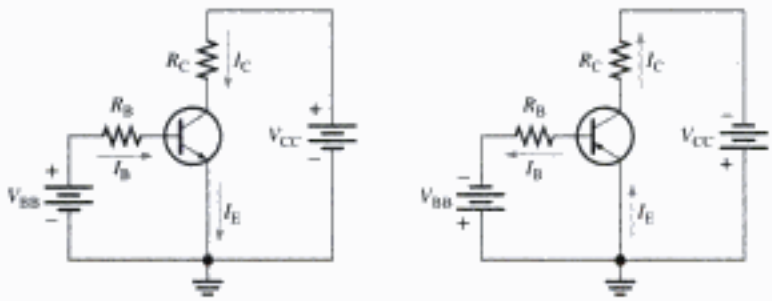
SECTION 4–2 REVIEW

1. What are the bias conditions of the base-emitter and base-collector junctions for a transistor to operate as an amplifier?
2. Which is the largest of the three transistor currents?
3. Is the base current smaller or larger than the emitter current?
4. Is the base region much thinner or much wider than the collector and emitter regions?
5. If the collector current is 1 mA and the base current is 10 μA, what is the emitter current?

4–3 TRANSISTOR CHARACTERISTICS AND PARAMETERS

Two important parameters, β_{DC} and α_{DC} are introduced and used to analyze a transistor circuit. Also, transistor characteristic curves are covered, and you will learn how a transistor's operation can be determined from these curves. Finally, maximum ratings of a transistor are discussed.

As discussed in the last section, when a transistor is connected to dc bias voltages, as shown in Figure 4–6 for both *npn* and *pnp* types, V_{BB} forward-biases the base-emitter junction, and V_{CC} reverse-biases the base-collector junction. Although in this chapter we are using battery symbols to represent the bias voltages, in practice the voltages are often derived from a dc power supply. For example, V_{CC} is normally taken directly from the power supply output and V_{BB} can be produced with a voltage divider. V_{BB} is very small when compared to V_{CC}.



◀ **FIGURE 4–6**
Transistor dc bias circuits.

DC Beta (β_{DC}) and DC Alpha (α_{DC})

The ratio of the dc collector current (I_C) to the dc base current (I_B) is the dc **beta** (β_{DC}), which is the dc current **gain** of a transistor.

$$\beta_{DC} = \frac{I_C}{I_B}$$

Equation 4–2

Typical values of β_{DC} range from less than 20 to 200 or higher. β_{DC} is usually designated as an equivalent hybrid (h) parameter, h_{FE}, on transistor data sheets. h-parameters are covered in later chapters. All you need to know now is that

$$h_{FE} = \beta_{DC}$$

The ratio of the dc collector current (I_C) to the dc emitter current (I_E) is the dc **alpha** (α_{DC}). The alpha is a less-used parameter than beta in transistor circuits.

$$\alpha_{DC} = \frac{I_C}{I_E}$$

Typically, values of α_{DC} range from 0.95 to 0.99 or greater, but α_{DC} is always less than 1. The reason is that I_C is always slightly less than I_E by the amount of I_B. For example, if I_E = 100 mA and I_B = 1 mA, then I_C = 99 mA and α_{DC} = 0.99.

EXAMPLE 4–1

Determine β_{DC} and I_E for a transistor where I_B = 50 μA and I_C = 3.65 mA.

Solution

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{3.65\text{ mA}}{50\ \mu\text{A}} = 73$$

$$I_E = I_C + I_B = 3.65\text{ mA} + 50\ \mu\text{A} = \mathbf{3.70\ mA}$$

Current and Voltage Analysis

Consider the basic transistor bias circuit configuration in Figure 4–7. Three transistor dc currents and three dc voltages can be identified.

I_B: dc base current

I_E: dc emitter current

I_C: dc collector current

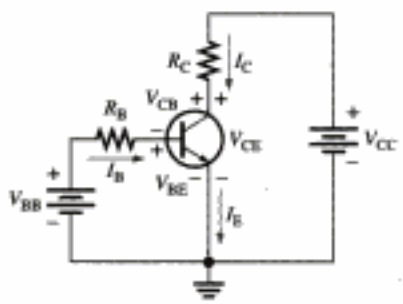
V_{BE}: dc voltage at base with respect to emitter

V_{CB}: dc voltage at collector with respect to base

V_{CE}: dc voltage at collector with respect to emitter

▶ **FIGURE 4–7**

Transistor currents and voltages.



V_{BB} forward-biases the base-emitter junction, and V_{CC} reverse-biases the base-collector junction. When the base-emitter junction is forward-biased, it is like a forward-biased diode and has a nominal forward voltage drop of

Equation 4–3

$$V_{BE} \cong 0.7\text{ V}$$

Although in an actual transistor V_{BE} can be as high as 0.9 V and is dependent on current, we will use 0.7 V throughout this text in order to simplify the analysis of the basic concepts.

Since the emitter is at ground (0 V), by Kirchhoff's voltage law, the voltage across R_B is

$$V_{R_B} = V_{BB} - V_{BE}$$

Also, by Ohm's law,

$$V_{R_B} = I_B R_B$$

Substituting for V_{R_B} yields

$$I_B R_B = V_{BB} - V_{BE}$$

Solving for I_B,

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$ **Equation 4–4**

The voltage at the collector with respect to the grounded emitter is

$$V_{CE} = V_{CC} - V_{R_C}$$

Since the drop across R_C is

$$V_{R_C} = I_C R_C$$

the voltage at the collector can be written as

$$V_{CE} = V_{CC} - I_C R_C$$ **Equation 4–5**

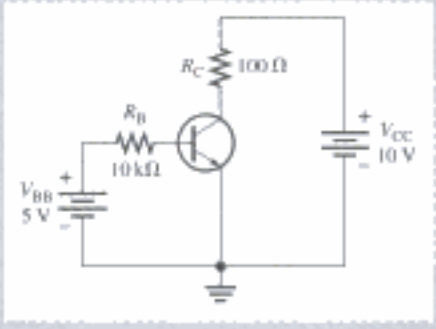
where $I_C = \beta_{DC} I_B$.

The voltage across the reverse-biased collector-base junction is

$$V_{CB} = V_{CE} - V_{BE}$$ **Equation 4–6**

EXAMPLE 4–2

Determine I_B, I_C, I_E, V_{BE}, V_{CE}, and V_{CB} in the circuit of Figure 4–8. The transistor has a $\beta_{DC} = 150$.



◀ FIGURE 4–8

Solution From Equation 4–3, $V_{BE} \cong$ **0.7 V**. Calculate the base, collector, and emitter currents as follows:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = \mathbf{430\ \mu A}$$

$$I_C = \beta_{DC} I_B = (150)(430\ \mu\text{A}) = \mathbf{64.5\ mA}$$

$$I_E = I_C + I_B = 64.5\text{ mA} + 430\ \mu\text{A} = \mathbf{64.9\ mA}$$

Solve for V_{CE} and V_{CB}.

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (64.5\text{ mA})(100\ \Omega) = 10\text{ V} - 6.45\text{ V} = \mathbf{3.55\ V}$$

$$V_{CB} = V_{CE} - V_{BE} = 3.55\text{ V} - 0.7\text{ V} = \mathbf{2.85\ V}$$

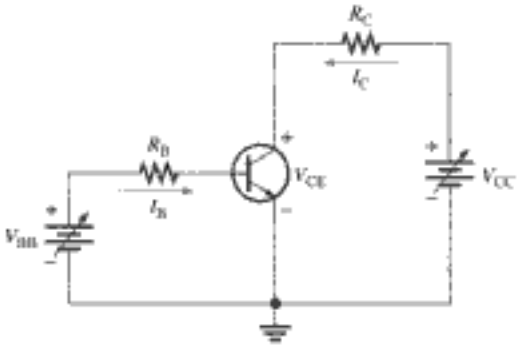
Since the collector is at a higher voltage than the base, the collector-base junction is reverse-biased.

Collector Characteristic Curves (Output Characteristics in CE)

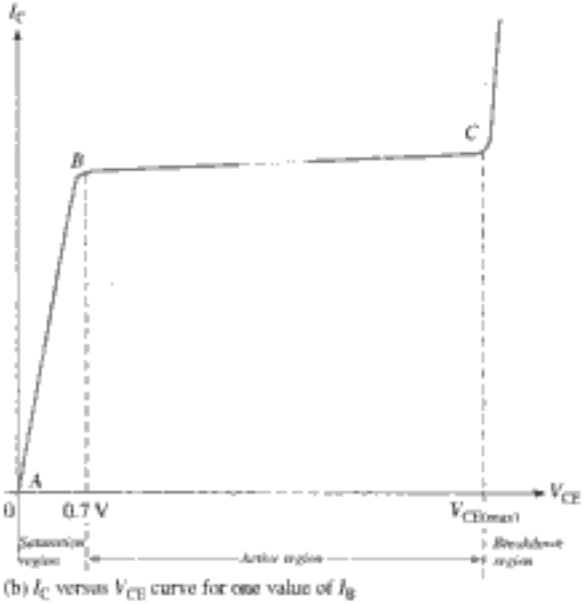
Using a circuit like that shown in Figure 4–9(a), you can generate a set of *collector characteristic curves* that show how the collector current, I_C, varies with the collector-to-emitter voltage, V_{CE}, for specified values of base current, I_B. Notice in the circuit diagram that both V_{BB} and V_{CC} are variable sources of voltage.

Assume that V_{BB} is set to produce a certain value of I_B and V_{CC} is zero. For this condition, both the base-emitter junction and the base-collector junction are forward-biased because the base is at approximately 0.7 V while the emitter and the collector are at 0 V. The base current is through the base-emitter junction because of the low impedance path to ground and, therefore, I_C is zero. When both junctions are forward-biased, the transistor is in the **saturation** region of its operation.

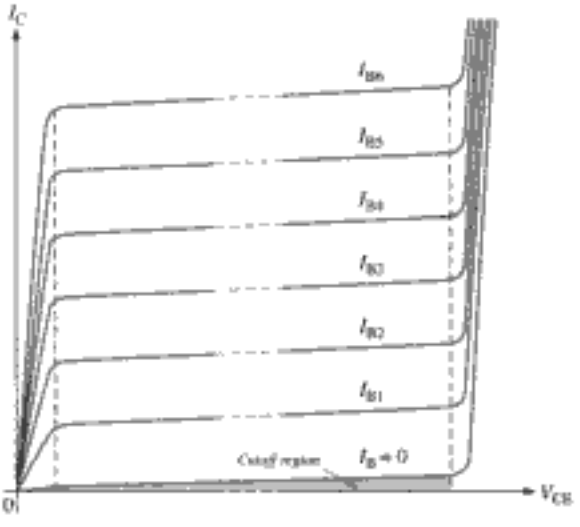
As V_{CC} is increased, V_{CE} increases gradually as the collector current increases. This is indicated by the portion of the characteristic curve between points *A* and *B* in Figure 4–9(b). I_C increases as V_{CC} is increased because V_{CE} remains less than 0.7 V due to the forward-biased base-collector junction.



(a) Circuit



(b) I_C versus V_{CE} curve for one value of I_B



(c) Family of I_C versus V_{CE} curves for several values of I_B ($I_{B1} < I_{B2} < I_{B3}$, etc.)

▲ FIGURE 4–9

Collector characteristic curves.

Ideally, when V_{CE} exceeds 0.7 V, the base-collector junction becomes reverse-biased and the transistor goes into the *active* or **linear** region of its operation. Once the base-collector junction is reverse-biased, I_C levels off and remains essentially constant for a given value of I_B as V_{CE} continues to increase. Actually, I_C increases very slightly as V_{CE} increases due to widening of the base-collector depletion region. This results in fewer holes for recombination in the base region which effectively causes a slight increase in β_{DC}. This is shown by the portion of the characteristic curve between points *B* and *C* in Figure 4–9(b). For this portion of the characteristic curve, the value of I_C is determined only by the relationship expressed as $I_C = \beta_{DC} I_B$.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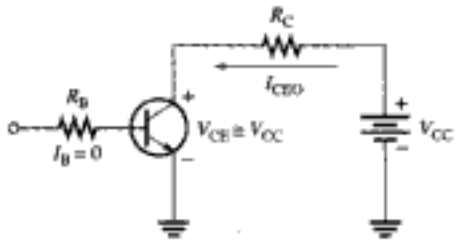
Cutoff

As previously mentioned, when $I_B = 0$, the transistor is in the cutoff region of its operation. This is shown in Figure 4–12 with the base lead open, resulting in a base current of zero. Under this condition, there is a very small amount of collector leakage current, I_{CEO}, due mainly to thermally produced carriers. Because I_{CEO} is extremely small, it will usually be neglected in circuit analysis so that $V_{CE} = V_{CC}$. In cutoff, both the base-emitter and the base-collector junctions are reverse-biased.

► FIGURE 4–12

Cutoff: Collector leakage current (I_{CEO}) is extremely small and is usually neglected. Base-emitter and base-collector junctions are reverse-biased.

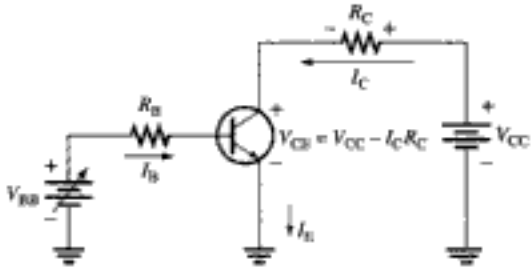


Saturation

When the base-emitter junction becomes forward-biased and the base current is increased, the collector current also increases ($I_C = \beta_{DC} I_B$) and V_{CE} decreases as a result of more drop across the collector resistor ($V_{CE} = V_{CC} - I_C R_C$). This is illustrated in Figure 4–13. When V_{CE} reaches its saturation value, $V_{CE(sat)}$, the base-collector junction becomes forward-biased and I_C can increase no further even with a continued increase in I_B. At the point of saturation, the relation $I_C = \beta_{DC} I_B$ is no longer valid. $V_{CE(sat)}$ for a transistor occurs somewhere below the knee of the collector curves, and it is usually only a few tenths of a volt for silicon transistors.

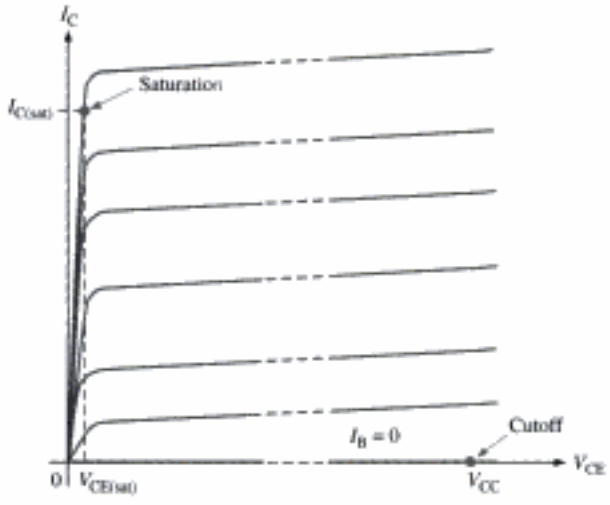
► FIGURE 4–13

Saturation: As I_B increases due to increasing V_{BB}, I_C also increases and V_{CE} decreases due to the increased voltage drop across R_C. When the transistor reaches saturation, I_C can increase no further regardless of further increase in I_B. Base-emitter and base-collector junctions are forward-biased.



DC Load Line

Cutoff and saturation can be illustrated in relation to the collector characteristic curves by the use of a load line. Figure 4–14 shows a dc load line drawn on a family of curves connecting the cutoff point and the saturation point. The bottom of the load line is at ideal cutoff where $I_C = 0$ and $V_{CE} = V_{CC}$. The top of the load line is at saturation where $I_C = I_{C(sat)}$ and $V_{CE} = V_{CE(sat)}$. In between cutoff and saturation along the load line is the *active region* of the transistor's operation.

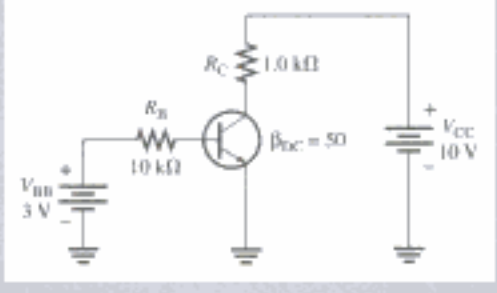


◀ FIGURE 4–14

DC load line on a family of collector characteristic curves illustrating the cutoff and saturation conditions.

EXAMPLE 4–4

Determine whether or not the transistor in Figure 4–15 is in saturation. Assume $V_{CE(sat)} = 0.2$ V.



◀ FIGURE 4–15

Solution First, determine $I_{C(sat)}$.

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{10\text{ V} - 0.2\text{ V}}{1.0\text{ k}\Omega} = \frac{9.8\text{ V}}{1.0\text{ k}\Omega} = 9.8\text{ mA}$$

Now, see if I_B is large enough to produce $I_{C(sat)}$.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{3\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = \frac{2.3\text{ V}}{10\text{ k}\Omega} = 0.23\text{ mA}$$

$$I_C = \beta_{DC} I_B = (50)(0.23\text{ mA}) = 11.5\text{ mA}$$

This shows that with the specified β_{DC}, this base current is capable of producing an I_C greater than $I_{C(sat)}$. Therefore, the **transistor is saturated**, and the collector current value of 11.5 mA is never reached. If you further increase I_B, the collector current remains at its saturation value.

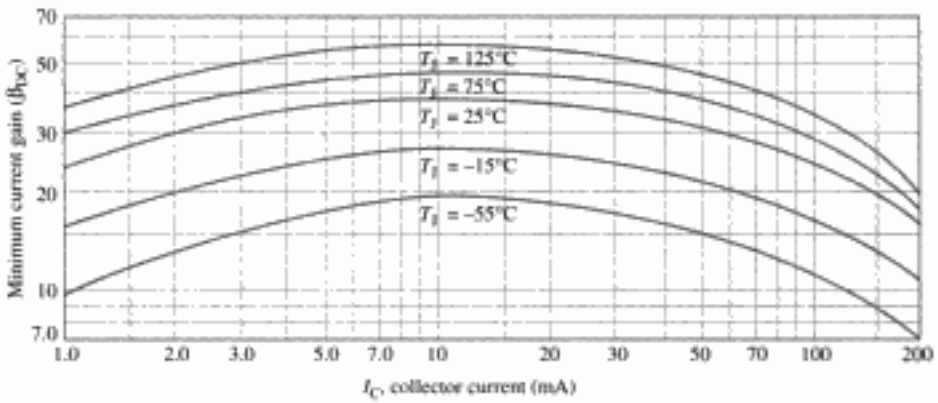
More About β_{DC}

The β_{DC} or h_{FE} is an important bipolar junction transistor parameter that we need to examine further. β_{DC} is not truly constant but varies with both collector current and with temperature. Keeping the junction temperature constant and increasing I_C causes β_{DC} to increase to a maximum. A further increase in I_C beyond this maximum point causes β_{DC}

to decrease. If I_C is held constant and the temperature is varied, β_{DC} changes directly with the temperature. If the temperature goes up, β_{DC} goes up and vice versa. Figure 4–16 shows the variation of β_{DC} with I_C and junction temperature (T_J) for a typical transistor.

▶ FIGURE 4–16

Variation of β_{DC} with I_C for several temperatures.



Maximum Transistor Ratings

A transistor, like any other electronic device, has limitations on its operation. These limitations are stated in the form of maximum ratings and are normally specified on the manufacturer's data sheet. Typically, maximum ratings are given for collector-to-base voltage, collector-to-emitter voltage, emitter-to-base voltage, collector current, and power dissipation.

The product of V_{CE} and I_C must not exceed the maximum power dissipation. Both V_{CE} and I_C cannot be maximum at the same time. If V_{CE} is maximum, I_C can be calculated as

Equation 4–7

$$I_C = \frac{P_{D(max)}}{V_{CE}}$$

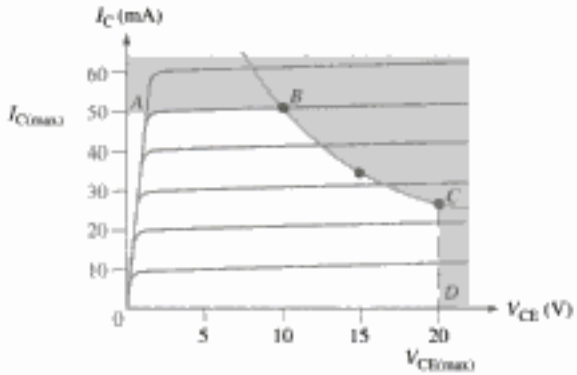
If I_C is maximum, V_{CE} can be calculated by rearranging Equation 4–7 as follows:

$$V_{CE} = \frac{P_{D(max)}}{I_C}$$

For any given transistor, a maximum power dissipation curve can be plotted on the collector characteristic curves, as shown in Figure 4–17(a). These values are tabulated in Figure 4–17(b). Assume $P_{D(max)}$ is 500 mW, $V_{CE(max)}$ is 20 V, and $I_{C(max)}$ is 50 mA. The curve shows that this particular transistor cannot be operated in the shaded portion of the graph. $I_{C(max)}$ is the limiting rating between points A and B, $P_{D(max)}$ is the limiting rating between points B and C, and $V_{CE(max)}$ is the limiting rating between points C and D.

▶ FIGURE 4–17

Maximum power dissipation curve and tabulated values.



(a)

$P_{D(max)}$	V_{CE}	I_C
500 mW	5 V	100 mA
500 mW	10 V	50 mA
500 mW	15 V	33 mA
500 mW	20 V	25 mA

(b)

EXAMPLE 4–5

A certain transistor is to be operated with $V_{CE} = 6$ V. If its maximum power rating is 250 mW, what is the most collector current that it can handle?

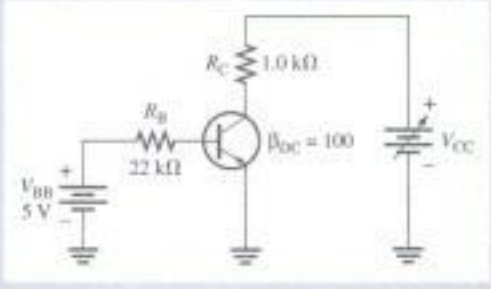
Solution

$$I_C = \frac{P_{D(max)}}{V_{CE}} = \frac{250 \text{ mW}}{6 \text{ V}} = \mathbf{41.7 \text{ mA}}$$

Remember that this is not necessarily the maximum I_C. The transistor can handle more collector current if V_{CE} is reduced, as long as $P_{D(max)}$ is not exceeded.

EXAMPLE 4–6

The transistor in Figure 4–18 has the following maximum ratings: $P_{D(max)} = 800$ mW, $V_{CE(max)} = 15$ V, and $I_{C(max)} = 100$ mA. Determine the maximum value to which V_{CC} can be adjusted without exceeding a rating. Which rating would be exceeded first?



◀ FIGURE 4–18

Solution First, find I_B so that you can determine I_C.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5 \text{ V} - 0.7 \text{ V}}{22 \text{ k}\Omega} = 195 \ \mu\text{A}$$

$$I_C = \beta_{DC} I_B = (100)(195 \ \mu\text{A}) = 19.5 \text{ mA}$$

I_C is much less than $I_{C(max)}$ and will not change with V_{CC}. It is determined only by I_B and β_{DC}.

The voltage drop across R_C is

$$V_{R_C} = I_C R_C = (19.5 \text{ mA})(1.0 \text{ k}\Omega) = 19.5 \text{ V}$$

Now you can determine the value of V_{CC} when $V_{CE} = V_{CE(max)} = 15$ V.

$$V_{R_C} = V_{CC} - V_{CE}$$

So,

$$V_{CC(max)} = V_{CE(max)} + V_{R_C} = 15 \text{ V} + 19.5 \text{ V} = \mathbf{34.5 \text{ V}}$$

V_{CC} can be increased to 34.5 V, under the existing conditions, before $V_{CE(max)}$ is exceeded. However, at this point it is not known whether or not $P_{D(max)}$ has been exceeded.

$$P_D = V_{CE(max)} I_C = (15 \text{ V})(19.5 \text{ mA}) = 293 \text{ mW}$$

Since $P_{D(max)}$ is 800 mW, it is *not* exceeded when $V_{CC} = 34.5$ V. So, $V_{CE(max)} = 15$ V is the limiting rating in this case. If the base current is removed causing the transistor to turn off, **$V_{CE(max)}$ will be exceeded first** because the entire supply voltage, V_{CC}, will be dropped across the transistor.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AC and all time-varying quantities always carry a lowercase italic subscript. For example, I_b, I_c, and I_e are the ac transistor currents. V_{be}, V_{cb}, and V_{ce} are the ac voltages from one transistor terminal to another. Single subscripted voltages such as V_b, V_c, and V_e are ac voltages from the transistor terminals to ground.

The rule is different for *internal* transistor resistances. As you will see later, transistors have internal ac resistances that are designated by lowercase r' with an appropriate subscript. For example, the internal ac emitter resistance is designated as r'_e.

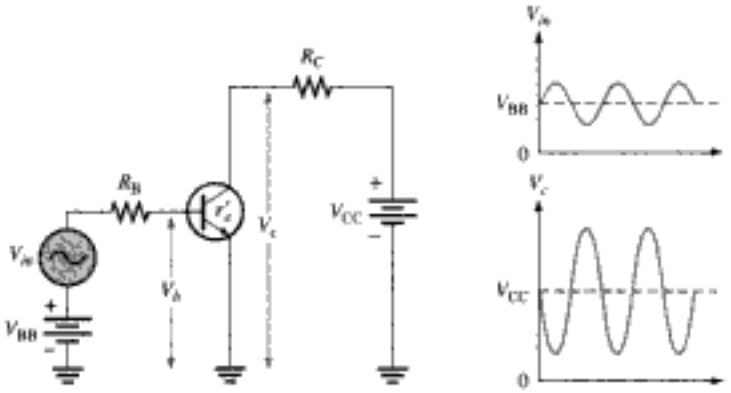
Circuit resistances external to the transistor itself use the standard italic capital R with a subscript that identifies the resistance as dc or ac (when applicable), just as for current and voltage. For example R_E is an external dc emitter resistance and R_e is an external ac emitter resistance.

Transistor Amplification

As you have learned, a transistor amplifies current because the collector current is equal to the base current multiplied by the current gain, β. The base current in a transistor is very small compared to the collector and emitter currents. Because of this, the collector current is approximately equal to the emitter current.

With this in mind, let's look at the circuit in Figure 4–19(a). An ac voltage, V_{in}, is superimposed on the dc bias voltage V_{BB} by connecting them in series with the base resistor, R_B, as shown. The dc bias voltage V_{CC} is connected to the collector through the collector resistor, R_C.

The ac input voltage produces an ac base current, which results in a much larger ac collector current. The ac collector current produces an ac voltage across R_C, thus producing an amplified, but inverted, reproduction of the ac input voltage in the active region of operation, as illustrated in Figure 4–19(b).



(a) Circuit with ac input voltage V_{in} and dc bias voltage superimposed

(b) Waveforms

◀ **FIGURE 4–19**

Basic transistor amplifier circuit.

The forward-biased base-emitter junction presents a very low resistance to the ac signal. This internal ac emitter resistance is designated r'_e. In Figure 4–19(a), the ac emitter current is

$$I_e \cong I_c = \frac{V_b}{r'_e}$$

The ac collector voltage, V_c, equals the ac voltage drop across R_C.

$$V_c = I_c R_C$$

Since $I_c \cong I_e$, the ac collector voltage is

$$V_c \cong I_e R_C$$

V_b can be considered the transistor ac input voltage where $V_b = V_{in} - I_b R_B$. V_c can be considered the transistor ac output voltage. The ratio of V_c to V_b is the ac voltage gain, A_v, of the transistor circuit.

$$A_v = \frac{V_c}{V_b}$$

Substituting $I_e R_C$ for V_c and $I_e r'_e$ for V_b yields

$$A_v = \frac{V_c}{V_b} \cong \frac{I_e R_C}{I_e r'_e}$$

The I_e terms cancel; therefore,

Equation 4–8

$$A_v \cong \frac{R_C}{r'_e}$$

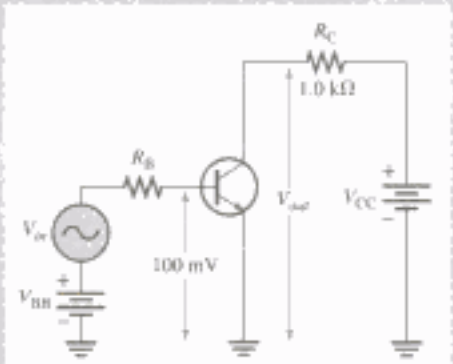
Equation 4–8 shows that the transistor in Figure 4–19 provides amplification in the form of voltage gain, which is dependent on the values of R_C and r'_e.

Since R_C is always considerably larger in value than r'_e, the output voltage is always greater than the input voltage.

EXAMPLE 4–8

Determine the voltage gain and the ac output voltage in Figure 4–20 if $r'_e = 50\ \Omega$.

▶ **FIGURE 4–20**



Solution The voltage gain is

$$A_v \cong \frac{R_C}{r'_e} = \frac{1.0\ \text{k}\Omega}{50\ \Omega} = \mathbf{20}$$

Therefore, the ac output voltage is

$$V_{out} = A_v V_b = (20)(100\ \text{mV}) = \mathbf{2\ V\ rms}$$

SECTION 4–4 REVIEW

1. What is amplification?
2. How is voltage gain defined?
3. Name two factors that determine the voltage gain of an amplifier.
4. What is the voltage gain of a transistor amplifier that has an output of 5 V rms and an input of 250 mV rms?
5. A transistor connected as in Figure 4–21 has an $r'_e = 20\ \Omega$. If R_C is 1200 Ω, what is the voltage gain?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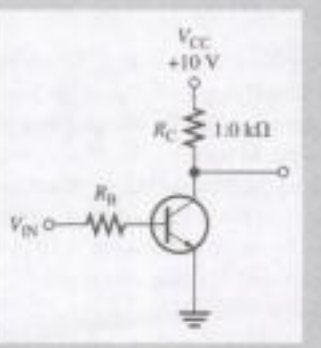
EXAMPLE 4–9

(a) For the transistor circuit in Figure 4–22, what is V_{CE} when $V_{IN} = 0$ V?

(b) What minimum value of I_B is required to saturate this transistor if β_{DC} is 200? Neglect $V_{CE(sat)}$.

(c) Calculate the maximum value of R_B when $V_{IN} = 5$ V.

► FIGURE 4–22



Solution (a) When $V_{IN} = 0$ V, the transistor is in cutoff (acts like an open switch) and

$$V_{CE} = V_{CC} = \mathbf{10\ V}$$

(b) Since $V_{CE(sat)}$ is neglected (assumed to be 0 V),

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{10\text{ V}}{1.0\text{ k}\Omega} = 10\text{ mA}$$

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}} = \frac{10\text{ mA}}{200} = \mathbf{50\ \mu A}$$

This is the value of I_B necessary to drive the transistor to the point of saturation. Any further increase in I_B will drive the transistor deeper into saturation but will not increase I_C.

(c) When the transistor is on, $V_{BE} \cong 0.7$ V. The voltage across R_B is

$$V_{R_B} = V_{IN} - V_{BE} = 5\text{ V} - 0.7\text{ V} = 4.3\text{ V}$$

Calculate the maximum value of R_B needed to allow a minimum I_B of 50 μA by Ohm's law as follows:

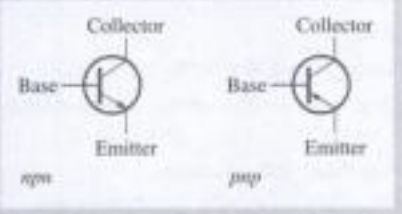
$$R_{B(max)} = \frac{V_{R_B}}{I_{B(min)}} = \frac{4.3\text{ V}}{50\ \mu\text{A}} = \mathbf{86\ k\Omega}$$

SECTION 4–5 REVIEW

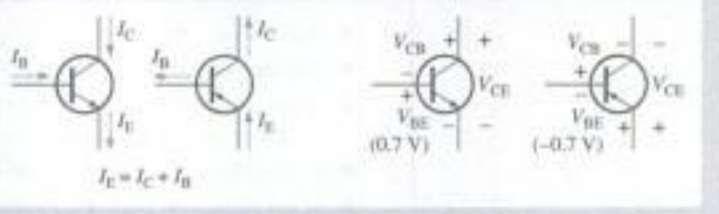
1. When a transistor is used as a switch, in what two states is it operated?
2. When is the collector current maximum?
3. When is the collector current approximately zero?
4. Under what condition is $V_{CE} = V_{CC}$?
5. When is V_{CE} minimum?

SUMMARY OF BIPOLAR JUNCTION TRANSISTORS

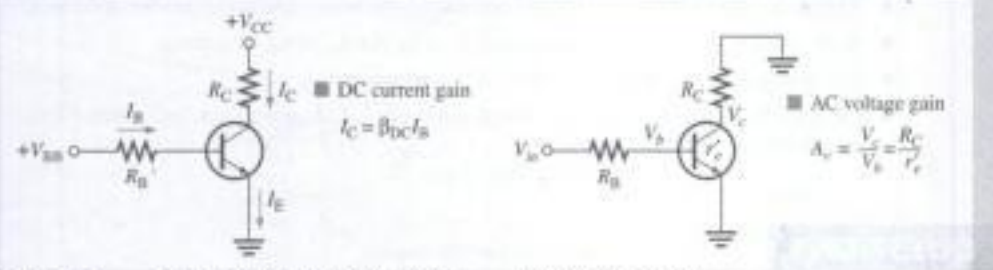
SYMBOLS



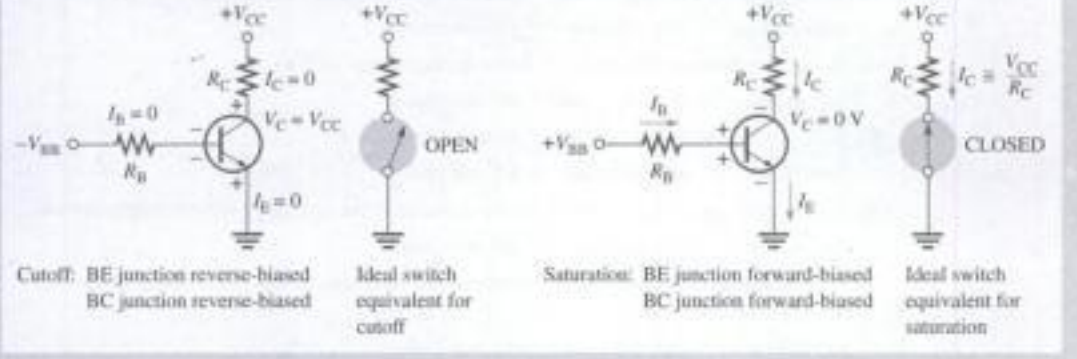
CURRENTS AND VOLTAGES



AMPLIFICATION



CUTOFF AND SATURATION



CHAPTER SUMMARY

- The BJT (bipolar junction transistor) is constructed with three regions: base, collector, and emitter.
- The BJT has two *pn* junctions, the base-emitter junction and the base-collector junction.
- Current in a BJT consists of both free electrons and holes, thus the term *bipolar*.
- The base region is very thin and lightly doped compared to the collector and emitter regions.
- The two types of bipolar junction transistor are the *npn* and the *pnp*.
- To operate as an amplifier, the base-emitter junction must be forward-biased and the base-collector junction must be reverse-biased. This is called *forward-reverse bias*.

- The three currents in the transistor are the base current (I_B), emitter current (I_E), and collector current (I_C).
- I_B is very small compared to I_C and I_E.
- The dc current gain of a transistor is the ratio of I_C to I_B and is designated β_{DC}. Values typically range from less than 20 to several hundred.
- β_{DC} is usually referred to as h_{FE} on transistor data sheets.
- The ratio of I_C to I_E is called α_{DC}. Values typically range from 0.95 to 0.99.
- When a transistor is forward-reverse biased, the voltage gain depends on the internal emitter resistance and the external collector resistance.
- A transistor can be operated as an electronic switch in cutoff and saturation.
- In cutoff, both *pn* junctions are reverse-biased and there is essentially no collector current. The transistor ideally behaves like an open switch between collector and emitter.
- In saturation, both *pn* junctions are forward-biased and the collector current is maximum. The transistor ideally behaves like a closed switch between collector and emitter.
- There is a variation in β_{DC} over temperature and also from one transistor to another of the same type.
- There are many types of transistor packages using plastic, metal, or ceramic.
- It is best to check a transistor in-circuit before removing it.
- Common faults are open junctions, low β_{DC}, excessive leakage currents, and external opens and shorts on the circuit board.

OBJECTIVE TYPE QUESTIONS

Answers are at the end of the chapter.

1. If a transistor with a higher β_{DC} is used in Figure 4–8, the collector current will
(a) increase **(b)** decrease **(c)** not change

2. If a transistor with a higher β_{DC} is used in Figure 4–8, the emitter current will
(a) increase **(b)** decrease **(c)** not change

3. If a transistor with a higher β_{DC} is used in Figure 4–8, the base current will
(a) increase **(b)** decrease **(c)** not change

4. If V_{BB} is reduced in Figure 4–15, the collector current will
(a) increase **(b)** decrease **(c)** not change

5. If V_{CC} in Figure 4–15 is increased, the base current will
(a) increase **(b)** decrease **(c)** not change

6. If the amplitude of V_{in} in Figure 4–20 is decreased, the ac output voltage amplitude will
(a) increase **(b)** decrease **(c)** not change

7. If the transistor in Figure 4–22 is saturated and the base current is increased, the collector current will
(a) increase **(b)** decrease **(c)** not change

8. If R_C in Figure 4–22 is reduced in value, the value of $I_{C(sat)}$ will
(a) increase **(b)** decrease **(c)** not change

9. The three terminals of a bipolar junction transistor are called
(a) *p*, *n*, *p* **(b)** *n*, *p*, *n* **(c)** input, output, ground **(d)** base, emitter, collector

10. In a *pnp* transistor, the *p* regions are
(a) base and emitter **(b)** base and collector **(c)** emitter and collector

11. For operation as an amplifier, the base of an *npn* transistor must be
(a) positive with respect to the emitter **(b)** negative with respect to the emitter
(c) positive with respect to the collector **(d)** 0 V

12. The emitter current is always
(a) greater than the base current **(b)** less than the collector current
(c) greater than the collector current **(d)** answers (a) and (c)

13. The β_{DC} of a transistor is its
    (a) current gain (b) voltage gain (c) power gain (d) internal resistance
14. If I_C is 50 times larger than I_B, then β_{DC} is
    (a) 0.02 (b) 100 (c) 50 (d) 500
15. The approximate voltage across the forward-biased base-emitter junction of a silicon BJT is
    (a) 0 V (b) 0.7 V (c) 0.3 V (d) V_{BR}
16. The bias condition for a transistor to be used as a linear amplifier is called
    (a) forward-reverse (b) forward-forward (c) reverse-reverse (d) collector bias
17. If the output of a transistor amplifier is 5 V rms and the input is 100 mV rms, the voltage gain is
    (a) 5 (b) 500 (c) 50 (d) 100
18. When operated in cutoff and saturation, the transistor acts like a
    (a) linear amplifier (b) switch (c) variable capacitor (d) variable resistor
19. In cutoff, V_{CE} is
    (a) 0 V (b) minimum (c) maximum
    (d) equal to V_{CC} (e) answers (a) and (b) (f) answers (c) and (d)
20. In saturation, V_{CE} is
    (a) 0.7 V (b) equal to V_{CC} (c) minimum (d) maximum
21. To saturate a BJT,
    (a) $I_B = I_{C(sat)}$ (b) $I_B > I_{C(sat)}/\beta_{DC}$
    (c) V_{CC} must be at least 10 V (d) the emitter must be grounded
22. Once in saturation, a further increase in base current will
    (a) cause the collector current to increase
    (b) not affect the collector current
    (c) cause the collector current to decrease
    (d) turn the transistor off
23. If the base-emitter junction is open, the collector voltage is
    (a) V_{CC} (b) 0 V (c) floating (d) 0.2 V

PROBLEMS

Answers to all selected problems at the end of the book.

BASIC PROBLEMS

SECTION 4–1 Transistor Structure

1. What are the majority carriers in the base region of an *npn* transistor called?
2. Explain the purpose of a thin, lightly doped base region.

SECTION 4–2 Basic Transistor Operation

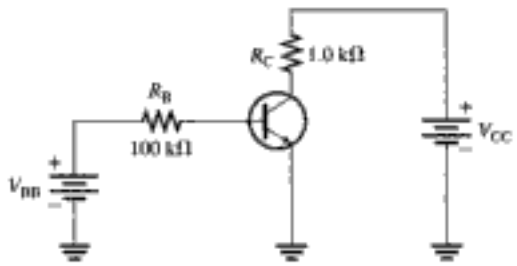
3. Why is the base current in a transistor so much less than the collector current?
4. In a certain transistor circuit, the base current is 2 percent of the 30 mA emitter current. Determine the collector current.
5. For normal operation of a *pnp* transistor, the base must be (+ or −) with respect to the emitter, and (+ or −) with respect to the collector.
6. What is the value of I_C for $I_E = 5.34$ mA and $I_B = 475\ \mu$A?

SECTION 4–3 Transistor Characteristics and Parameters

7. What is the α_{DC} when $I_C = 8.23$ mA and $I_E = 8.69$ mA?
8. A certain transistor has an $I_C = 25$ mA and an $I_B = 200\ \mu$A. Determine the β_{DC}.
9. What is the β_{DC} of a transistor if $I_C = 20.5$ mA and $I_E = 20.3$ mA?
10. What is the α_{DC} if $I_C = 5.35$ mA and $I_B = 50\ \mu$A?
11. A certain transistor exhibits an α_{DC} of 0.96. Determine I_C when $I_E = 9.35$ mA.

12. A base current of 50 μA is applied to the transistor in Figure 4–23, and a voltage of 5 V is dropped across R_C. Determine the β_{DC} of the transistor.

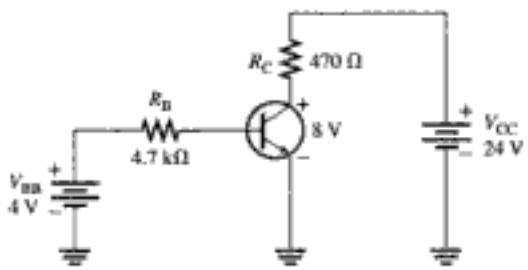
▶ **FIGURE 4–23**



13. Calculate α_{DC} for the transistor in Problem 12.

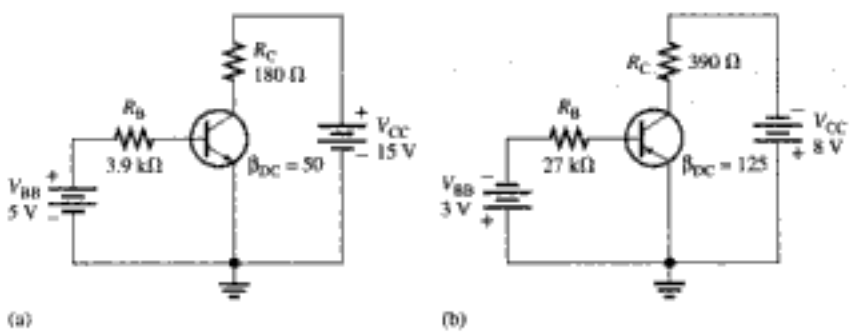
14. Determine each current in Figure 4–24. What is the β_{DC}?

▶ **FIGURE 4–24**



15. Find V_{CE}, V_{BE}, and V_{CB} in both circuits of Figure 4–25.

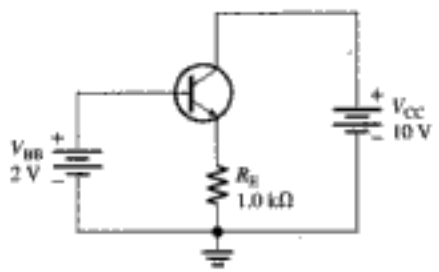
▶ **FIGURE 4–25**



16. Determine whether or not the transistors in Figure 4–25 are saturated.

17. Find I_B, I_E, and I_C in Figure 4–26. $\alpha_{DC} = 0.98$.

▶ **FIGURE 4–26**

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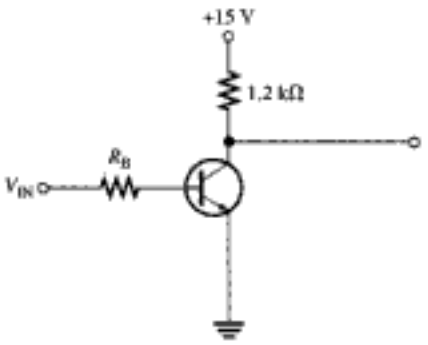
26. The transistor in Figure 4–29 has a β_{DC} of 50. Determine the value of R_B required to ensure saturation when V_{IN} is 5 V. What must V_{IN} be to cut off the transistor? Assume $V_{CE(sat)} = 0$ V.

▶ FIGURE 4–29



ANSWERS

SECTION REVIEWS

SECTION 4–1 Transistor Structure

1. The two types of BJTs are *npn* and *pnp*.
2. The terminals of a BJT are base, collector, and emitter.
3. The three regions of a BJT are separated by two *pn* junctions.

SECTION 4–2 Basic Transistor Operation

1. To operate as an amplifier, the base-emitter is forward-biased and the base-collector is reverse-biased.
2. The emitter current is the largest.
3. The base current is much smaller than the emitter current.
4. The base region is very narrow compared to the other two regions.
5. $I_E = 1\text{ mA} + 10\ \mu\text{A} = 1.01\text{ mA}$

SECTION 4–3 Transistor Characteristics and Parameters

1. $\beta_{DC} = I_C/I_B$; $\alpha_{DC} = I_C/I_E$; h_{FE} is β_{DC}.
2. $\beta_{DC} = 100$; $\alpha_{DC} = 100/(100 + 1) = 0.99$
3. I_C is plotted versus V_{CE}.
4. Forward-reverse bias is required for amplifier operation.
5. β_{DC} increases with temperature.
6. No. β_{DC} generally varies some from one device to the next for a given type.

SECTION 4–4 The Transistor as an Amplifier

1. Amplification is the process where a smaller signal is used to produce a larger identical signal.
2. Voltage gain is the ratio of output voltage to input voltage.
3. R_C and r'_e determine the voltage gain.
4. $A_v = 5\text{ V}/250\text{ mV} = 20$
5. $A_v = 1200\ \Omega/20\ \Omega = 60$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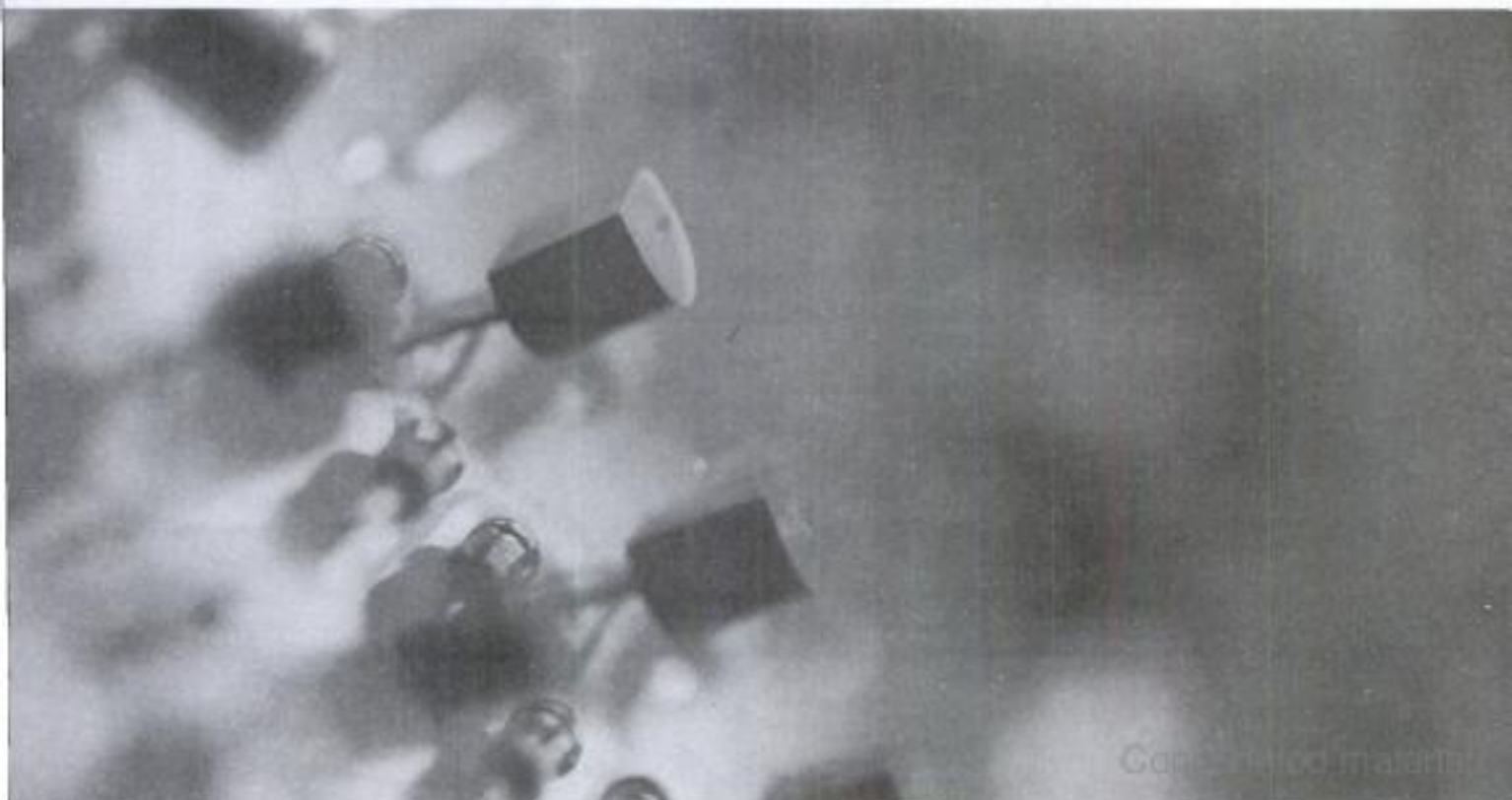
5

TRANSISTOR BIAS CIRCUITS

CHAPTER OUTLINE

INTRODUCTION

A transistor must be properly biased in order to operate as an amplifier. DC biasing is used to establish a steady level of transistor current and voltage called the *dc operating point* or *quiescent point (Q-point)*. In this chapter, several types of bias circuits are discussed. This material lays the groundwork for the study of amplifiers, oscillators, and other circuits that cannot operate without proper biasing.

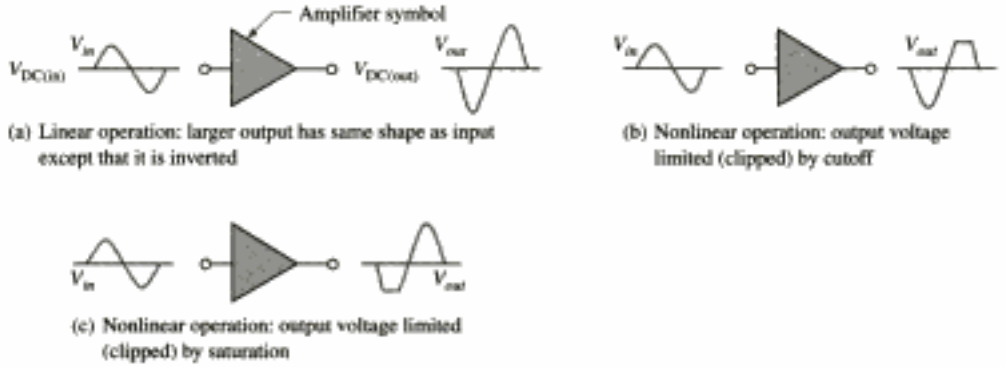


5–1 THE DC OPERATING POINT

A transistor must be properly biased with a dc voltage in order to operate as an amplifier. A dc operating point must be set so that signal variations at the input terminal are amplified and accurately reproduced at the output terminal. As you learned in previous chapter, when you bias a transistor, you establish the dc voltage and current values. This means, for example, that at the dc operating point, I_C and V_{CE} have specified values. The dc operating point is often referred to as the Q-point (quiescent point).

DC Bias

Bias establishes the dc operating point for proper linear operation of an amplifier. If an amplifier is not biased with correct dc voltages on the input and output, it can go into saturation or cutoff when an input signal is applied. Figure 5–1 shows the effects of proper and improper dc biasing of an inverting amplifier. In part (a), the output signal is an amplified replica of the input signal except that it is inverted, which means that it is 180° out of phase with the input. The output signal swings equally above and below the dc bias level of the output, $V_{DC(out)}$. Improper biasing can cause distortion in the output signal, as illustrated in parts (b) and (c). Part (b) illustrates limiting of the positive portion of the output voltage as a result of a **Q-point** (dc operating point) being too close to cutoff. Part (c) shows limiting of the negative portion of the output voltage as a result of a dc operating point being too close to saturation.



(a) Linear operation: larger output has same shape as input except that it is inverted

(b) Nonlinear operation: output voltage limited (clipped) by cutoff

(c) Nonlinear operation: output voltage limited (clipped) by saturation

▲ FIGURE 5–1

Examples of linear and nonlinear operation of an inverting amplifier (the triangle symbol).

Graphical Analysis The transistor in Figure 5–2(a) is biased with variable voltages V_{CC} and V_{BB} to obtain certain values of I_B, I_C, I_E, and V_{CE}. The collector characteristic curves for this particular transistor are shown in Figure 5–2(b); we will use these curves to graphically illustrate the effects of dc bias.

In Figure 5–3, we assign three values to I_B and observe what happens to I_C and V_{CE}. First, V_{BB} is adjusted to produce an I_B of 200 μA, as shown in Figure 5–3(a). Since $I_C = \beta_{DC} I_B$,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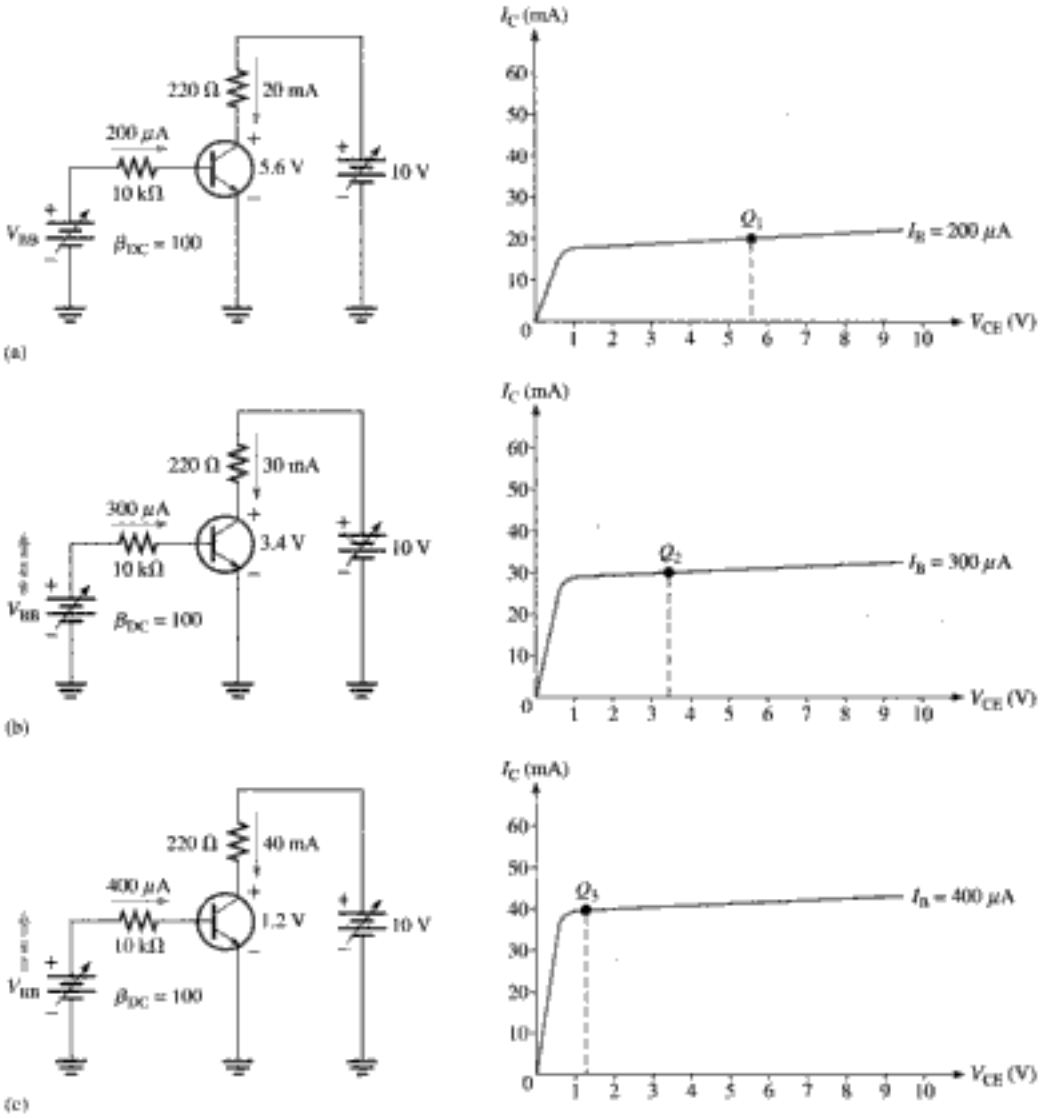

▲ FIGURE 5–3

Illustration of Q-point adjustment.

This results in a straight line equation for the load line of the form $y = mx + b$ as follows:

$$I_C = -\left(\frac{1}{R_C}\right)V_{CE} + \frac{V_{CC}}{R_C}$$

where $-1/R_C$ is the slope and V_{CC}/R_C is the y-axis intercept point.

Linear Operation The region along the load line including all points between saturation and cutoff is generally known as the **linear region** of the transistor's operation. As long as the transistor is operated in this region, the output voltage is ideally a linear reproduction of the input.

Figure 5–5 shows an example of the linear operation of a transistor. AC quantities are indicated by lowercase italic subscripts. Assume a sinusoidal voltage, V_{in}, is superimposed


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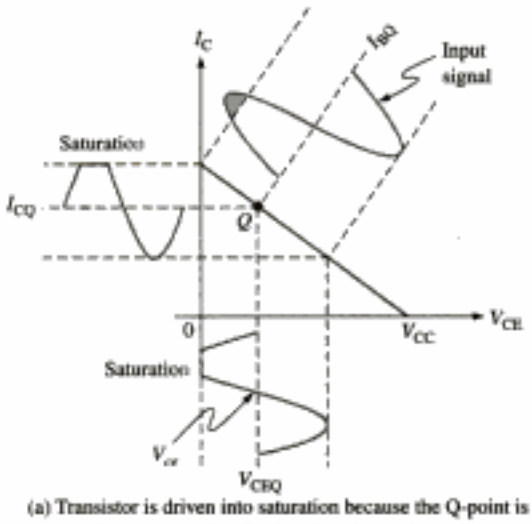
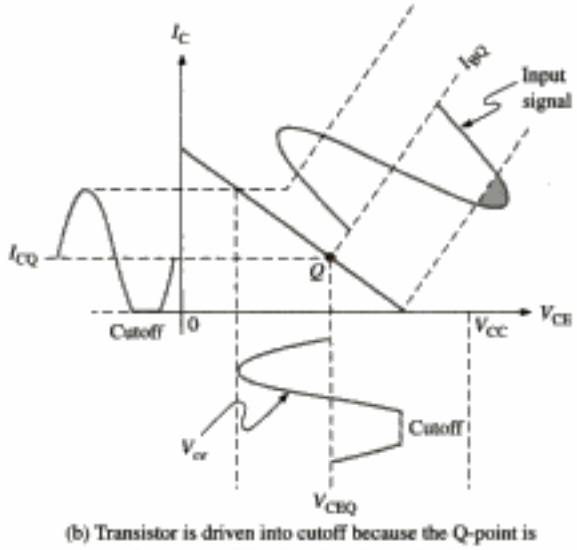
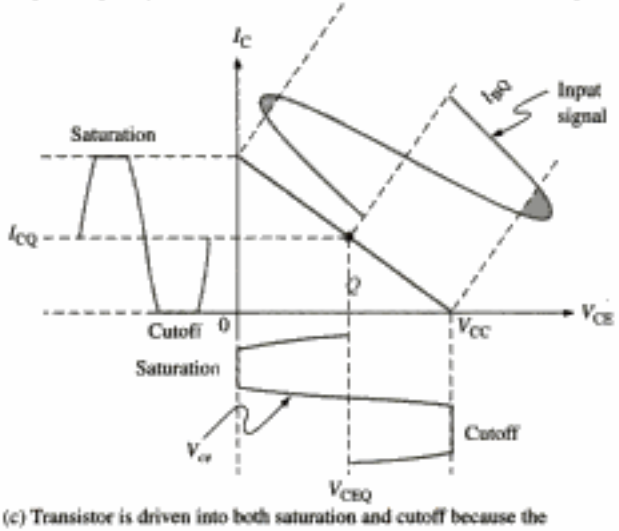


(a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.



(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.



(c) Transistor is driven into both saturation and cutoff because the input signal is too large.

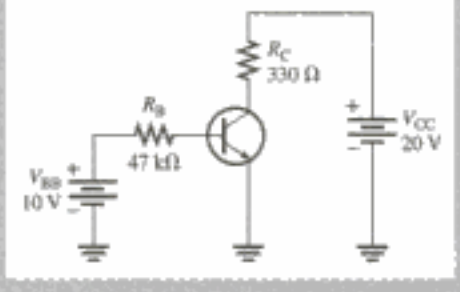
▲ FIGURE 5–6

Graphical load line illustration of a transistor being driven into saturation and/or cutoff.

EXAMPLE 5–1

Determine the Q-point for the circuit in Figure 5–7. Find the maximum peak value of base current for linear operation. Assume $\beta_{DC} = 200$.

► FIGURE 5–7



Solution The Q-point is defined by the values of I_C and V_{CE}. Find these values by using formulas you learned in Chapter 4.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{47\text{ k}\Omega} = 198\ \mu\text{A}$$

$$I_C = \beta_{DC} I_B = (200)(198\ \mu\text{A}) = \mathbf{39.6\ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 20\text{ V} - 13.07\text{ V} = \mathbf{6.93\ V}$$

The Q-point is at $I_C = 39.6$ mA and at $V_{CE} = 6.93$ V.

Since $I_{C(cutoff)} = 0$, you need to know $I_{C(sat)}$ to determine how much variation in collector current can occur and still maintain linear operation of the transistor.

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{20\text{ V}}{330\ \Omega} = 60.6\text{ mA}$$

The dc load line is graphically illustrated in Figure 5–8, showing that before saturation is reached, I_C can increase an amount ideally equal to

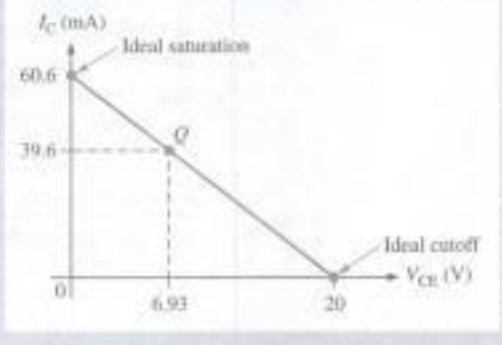
$$I_{C(sat)} - I_{CQ} = 60.6\text{ mA} - 39.6\text{ mA} = 21\text{ mA}$$

However, I_C can decrease by 39.6 mA before cutoff ($I_C = 0$) is reached. Therefore, the limiting excursion is 21 mA because the *Q-point is closer to saturation than to cutoff.* The 21 mA is the maximum peak variation of the collector current. Actually, it would be slightly less in practice because $V_{CE(sat)}$ is not quite zero.

Determine the maximum peak variation of the base current as follows:

$$I_{b(peak)} = \frac{I_{c(peak)}}{\beta_{DC}} = \frac{21\text{ mA}}{200} = \mathbf{105\ \mu A}$$

▶ **FIGURE 5–8**



SECTION 5–1 REVIEW

Answers are at the end of the chapter.

1. What are the upper and lower limits on a dc load line in terms of V_{CE} and I_C?
2. Define *Q-point.*
3. At what point on the load line does saturation begin? At what point does cutoff occur?
4. For maximum V_{out}, where should the Q-point be placed?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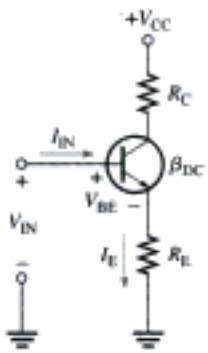
By Ohm's law,

$$R_{IN(base)} = \frac{V_{IN}}{I_{IN}}$$

Kirchhoff's voltage law applied around the base-emitter circuit yields

$$V_{IN} = V_{BE} + I_E R_E$$



◀ **FIGURE 5–11**

DC input resistance is V_{IN}/I_{IN}.

With the assumption that $V_{BE} << I_E R_E$, the equation reduces to

$$V_{IN} \cong I_E R_E$$

Now, since $I_E \cong I_C = \beta_{DC} I_B$,

$$V_{IN} \cong \beta_{DC} I_B R_E$$

The input current is the base current:

$$I_{IN} = I_B$$

By substitution,

$$R_{IN(base)} = \frac{V_{IN}}{I_{IN}} \cong \frac{\beta_{DC} I_B R_E}{I_B}$$

Cancelling the I_B terms gives

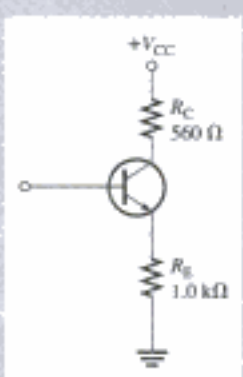
$$R_{IN(base)} \cong \beta_{DC} R_E$$

Equation 5–1

EXAMPLE 5–2

Determine the dc input resistance looking in at the base of the transistor in Figure 5–12. $\beta_{DC} = 125$.

▶ **FIGURE 5–12**



Solution $R_{IN(base)} \cong \beta_{DC} R_E = (125)(1.0\,\text{k}\Omega) = \mathbf{125\,k\Omega}$

Analysis of a Voltage-Divider Bias Circuit

A voltage-divider biased *npn* transistor is shown in Figure 5–13(a). Let's begin the analysis by determining the voltage at the base using the voltage-divider formula, which is developed as follows:

$$R_{IN(base)} \cong \beta_{DC} R_E$$

The total resistance from base to ground is

$$R_2 \| R_{IN(base)}$$

Substituting $R_{IN(base)} \cong \beta_{DC} R_E$,

$$R_2 \| \beta_{DC} R_E$$

A voltage-divider is formed by R_1 and the resistance from base to ground ($\beta_{DC} R_E$) in parallel with R_2 as shown in Figure 5–13(b). Applying the voltage-divider formula yields

Equation 5–2

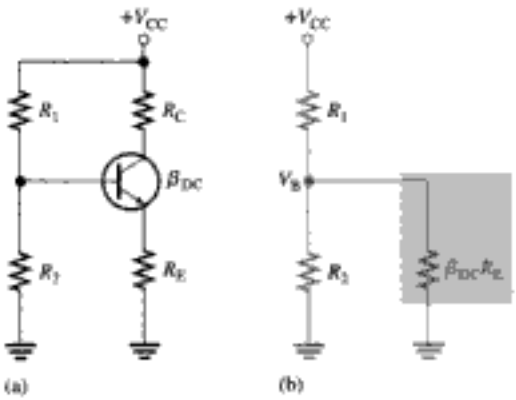
$$V_B = \left(\frac{R_2 \| \beta_{DC} R_E}{R_1 + (R_2 \| \beta_{DC} R_E)} \right) V_{CC}$$

If $\beta_{DC} R_E >> R_2$ (at least ten times greater), then the formula simplifies to

$$V_B \cong \left(\frac{R_2}{R_1 + R_2} \right) V_{CC}$$

▶ FIGURE 5–13

An *npn* transistor with voltage-divider bias.



Once you know the base voltage, you can determine the emitter voltage, which equals V_B less the value of the base-emitter drop (V_{BE}).

Equation 5–3

$$V_E = V_B - V_{BE}$$

You can find the emitter current by using Ohm's law.

Equation 5–4

$$I_E = \frac{V_E}{R_E}$$

Once you know I_E, you can find all the other circuit values.

Equation 5–5

$$I_C \cong I_E$$

Equation 5–6

$$V_C = V_{CC} - I_C R_C$$

Once you know V_C and V_E, you can determine V_{CE}.

$$V_{CE} = V_C - V_E$$

Also, you can express V_{CE} in terms of I_C by using Kirchhoff's voltage law as follows:

$$V_{CC} - I_C R_C - I_E R_E - V_{CE} = 0$$

Since $I_C \cong I_E$,

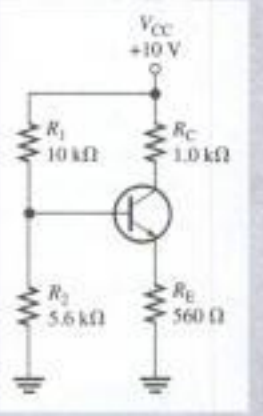
$$V_{CE} \cong V_{CC} - I_C R_C - I_C R_E$$

$$V_{CE} \cong V_{CC} - I_C(R_C + R_E) \qquad \text{Equation 5–7}$$

EXAMPLE 5–3

Determine V_{CE} and I_C in the voltage-divider biased transistor circuit of Figure 5–14 if $\beta_{DC} = 100$.

▶ FIGURE 5–14



Solution First, determine the dc input resistance at the base to see if it can be neglected.

$$R_{IN\,(base)} \cong \beta_{DC} R_E = (100)(560\ \Omega) = 56\ \text{k}\Omega$$

A common rule-of-thumb is that if two resistors are in parallel and one is at least ten times the other, the total resistance is approximately equal to the smaller value. However, in some cases, this may result in unacceptable inaccuracy.

In this case, $R_{IN(base)} = 10R_2$, so neglect $R_{IN(base)}$. In the related exercise, you will rework this example taking $R_{IN(base)}$ into account and compare the difference. Proceed with the analysis by determining the base voltage.

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right) V_{CC} = \left(\frac{5.6\ \text{k}\Omega}{15.6\ \text{k}\Omega}\right) 10\ \text{V} = 3.59\ \text{V}$$

So,

$$V_E = V_B - V_{BE} = 3.59\ \text{V} - 0.7\ \text{V} = 2.89\ \text{V}$$

and

$$I_E = \frac{V_E}{R_E} = \frac{2.89\ \text{V}}{560\ \Omega} = 5.16\ \text{mA}$$

Therefore,

$$I_C \cong I_E = \mathbf{5.16\ mA}$$

and

$$V_{CE} \cong V_{CC} - I_C(R_C + R_E) = 10\ \text{V} - 5.16\ \text{mA}(1.56\ \text{k}\Omega) = \mathbf{1.95\ V}$$

Since $V_{CE} > 0$ V (or greater than a few tenths of a volt), you know that the transistor is *not* in saturation.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This last equation shows that I_E, and therefore I_C, is independent of β_{DC} (notice that β_{DC} does not appear in the equation) for the stated condition. This can be achieved in practice by selecting a value for R_E that is at least ten times the resistance of the parallel combination of the voltage-divider resistors (R_{TH}) divided by the minimum β_{DC}.

Voltage-divider bias is widely used because reasonably good stability is achieved with a single supply voltage.

Voltage-Divider Biased *PNP* Transistor

As you know, a *pnp* transistor requires bias polarities opposite to the *npn*. This can be accomplished with a negative collector supply voltage, as in Figure 5–16(a), or with a positive emitter supply voltage, as in Figure 5–16(b). In a schematic, the *pnp* is often drawn upside down so that the supply voltage line can be drawn across the top of the schematic and ground at the bottom, as in Figure 5–17. The analysis procedure is basically the same as for an *npn* transistor circuit, as demonstrated in the following steps with reference to Figure 5–17. The base voltage is determined by using the voltage-divider formula.

$$V_B = \left(\frac{R_1}{R_1 + R_2 \| \beta_{DC} R_E}\right) V_{EE}$$

and

$$V_E = V_B + V_{BE}$$

By Ohm's law,

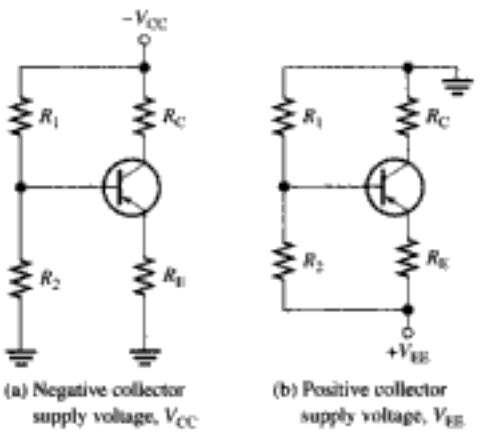
$$I_E = \frac{V_{EE} - V_E}{R_E}$$

and

$$V_C = I_C R_C$$

Therefore,

$$V_{EC} = V_E - V_C$$

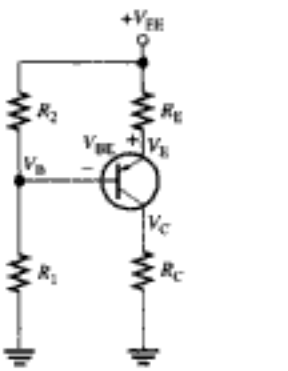


(a) Negative collector supply voltage, V_{CC}

(b) Positive collector supply voltage, V_{EE}

▲ FIGURE 5–16

Voltage-divider biased *pnp* transistor.

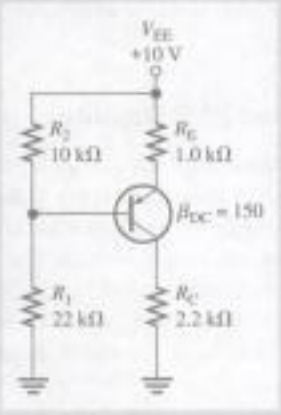


▲ FIGURE 5–17

EXAMPLE 5–4

Find I_C and V_{EC} for the *pnp* transistor circuit in Figure 5–18.

▶ FIGURE 5–18



Solution First, check to see if $R_{IN(base)}$ can be neglected.

$$R_{IN(base)} = \beta_{DC}R_E = (150)(1.0\ \text{k}\Omega) = 150\ \text{k}\Omega$$

Since 150 kΩ is more than ten times R_2, the condition $\beta_{DC}R_E >> R_2$ is met and $R_{IN(base)}$ can be neglected. Now, calculate V_B.

$$V_B \cong \left(\frac{R_1}{R_1 + R_2}\right)V_{EE} = \left(\frac{22\ \text{k}\Omega}{32\ \text{k}\Omega}\right)10\ \text{V} = 6.88\ \text{V}$$

Then

$$V_E = V_B + V_{BE} = 6.88\ \text{V} + 0.7\ \text{V} = 7.58\ \text{V}$$

and

$$I_E = \frac{V_{EE} - V_E}{R_E} = \frac{10\ \text{V} - 7.58\ \text{V}}{1.0\ \text{k}\Omega} = 2.42\ \text{mA}$$

From I_E, you can determine I_C and V_{CE} as follows:

$$I_C \cong I_E = \mathbf{2.42\ mA}$$

and

$$V_C = I_C R_C = (2.42\ \text{mA})(2.2\ \text{k}\Omega) = 5.32\ \text{V}$$

Therefore,

$$V_{EC} = V_E - V_C = 7.58\ \text{V} - 5.32\ \text{V} = \mathbf{2.26\ V}$$

EXAMPLE 5–5

Find I_C and V_{CE} for a *pnp* transistor circuit with these values: $R_1 = 68\ \text{k}\Omega$, $R_2 = 47\ \text{k}\Omega$, $R_C = 1.8\ \text{k}\Omega$, $R_E = 2.2\ \text{k}\Omega$, $V_{CC} = -6\ \text{V}$, and $\beta_{DC} = 75$. Refer to Figure 5–16(a), which shows the schematic with a negative supply voltage.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Kirchhoff's voltage law applied around the collector circuit in Figure 5–19 gives the following equation:

$$V_{CC} - I_C R_C - V_{CE} = 0$$

Solving for V_{CE},

Equation 5–8

$$V_{CE} = V_{CC} - I_C R_C$$

Substituting the expression for I_B into the formula $I_C = \beta_{DC} I_B$ yields

Equation 5–9

$$I_C = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$$

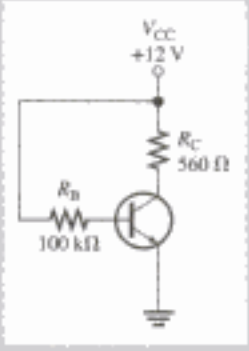
Q-Point Stability of Base Bias Equation 5–9 shows that I_C is dependent on β_{DC}. The disadvantage of this is that a variation in β_{DC} causes I_C and, as a result, V_{CE} to change, thus changing the Q-point of the transistor. This makes the base bias circuit extremely beta-dependent and very unstable.

Recall that β_{DC} varies with temperature and collector current. In addition, there is a large spread of β_{DC} values from one transistor to another of the same type due to manufacturing variations.

EXAMPLE 5–6

Determine how much the Q-point (I_C, V_{CE}) for the circuit in Figure 5–20 will change over a temperature range where β_{DC} increases from 85 to 100 and V_{BE} decreases from 0.7 V to 0.6 V.

▶ **FIGURE 5–20**



Solution For $\beta_{DC} = 85$ and $V_{BE} = 0.7$ V,

$$I_{C(1)} = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = 85\left(\frac{12\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega}\right) = 9.61\text{ mA}$$

$$V_{CE(1)} = V_{CC} - I_C R_C = 12\text{ V} - (9.61\text{ mA})(560\ \Omega) = 6.62\text{ V}$$

For $\beta_{DC} = 100$ and $V_{BE} = 0.6$ V,

$$I_{C(2)} = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = 100\left(\frac{12\text{ V} - 0.6\text{ V}}{100\text{ k}\Omega}\right) = 11.4\text{ mA}$$

$$V_{CE(2)} = V_{CC} - I_C R_C = 12\text{ V} - (11.4\text{ mA})(560\ \Omega) = 5.62\text{ V}$$

The percent change in I_C as β_{DC} changes from 85 to 100 and V_{BE} changes from 0.7 V to 0.6 V is

$$\%\ \Delta I_C = \left(\frac{I_{C(2)} - I_{C(1)}}{I_{C(1)}}\right)100\%$$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25. Determine I_C and V_{CE} in the *pnp* emitter bias circuit of Figure 5–33. Assume $\beta_{DC} = 100$.

26. Determine V_B, V_C, and I_C in Figure 5–34.

27. What value of R_C can be used to decrease I_C in Problem 26 by 25 percent?

28. What is the minimum power rating for the transistor in Problem 27?

29. A collector-feedback circuit uses an *npn* transistor with $V_{CC} = 12$ V, $R_C = 1.2$ kΩ, and $R_B = 47$ kΩ. Determine the collector current and the collector voltage if $\beta_{DC} = 200$.

ANSWERS

SECTION REVIEWS

SECTION 5–1 The DC Operating Point

1. The upper load line limit is $I_{C(sat)}$ and $V_{CE(sat)}$. The lower limit is $I_C = 0$ and $V_{CE(cutoff)}$.
2. The Q-point is the dc point at which a transistor is biased specified by V_{CE} and I_C.
3. Saturation begins at the intersection of the load line and the vertical portion of the collector curve. Cutoff occurs at the intersection of the load line and the $I_B = 0$ curve.
4. The Q-point must be centered on the load line for maximum V_{ce}.

SECTION 5–2 Voltage-Divider Bias

1. $R_{IN(base)} = V_{IN}/I_{IN} = 5\text{ V}/5\ \mu\text{A} = 1\text{ M}\Omega$
2. $R_{IN(base)} = \beta_{DC}R_E = 190(1.0\text{ k}\Omega) = 190\text{ k}\Omega$
3. $V_B = 5$ V
4. Voltage-divider bias is stable and requires only one supply voltage.

SECTION 5–3 Other Bias Methods

1. Base bias is beta-dependent.
2. The Q-point changes due to changes in β_{DC} and V_{CE} over temperature.
3. Emitter bias is much less dependent on the value of beta than is base bias.
4. Emitter bias requires two separate supply voltages.
5. I_C increases with β_{DC}, causing a reduction in V_C and, therefore, less voltage across R_B, thus less I_B.

OBJECTIVE TYPE QUESTIONS

1. (a) **2.** (b) **3.** (b) **4.** (b) **5.** (a) **6.** (c) **7.** (c) **8.** (b) **9.** (c) **10.** (d)
11. (d) **12.** (c) **13.** (a) **14.** (b) **15.** (c) **16.** (d) **17.** (a) **18.** (c) **19.** (a) **20.** (c)
21. (f)

6

BJT AMPLIFIERS

CHAPTER OUTLINE

INTRODUCTION

The things you learned about biasing a transistor are now applied in this chapter where bipolar junction transistor (BJT) circuits are used as small-signal amplifiers. The term *small-signal* refers to the use of signals that take up a relatively small percentage of an amplifier's operational range. Additionally, you will learn how to reduce an amplifier to an equivalent dc and ac circuit for easier analysis, and you will learn about multistage amplifiers. The differential amplifier is also covered.

6–1 AMPLIFIER OPERATION

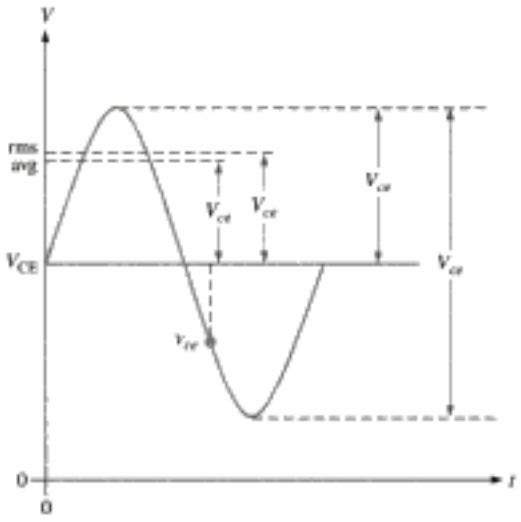
The biasing of a transistor is purely a dc operation. The purpose of biasing is to establish a Q-point about which variations in current and voltage can occur in response to an ac input signal. In applications where small signal voltages must be amplified—such as from an antenna or a microphone—variations about the Q-point are relatively small. Amplifiers designed to handle these small ac signals are often referred to as small-signal amplifiers.

AC Quantities

In the previous chapters, dc quantities were identified by nonitalic uppercase (capital) subscripts such as I_C, I_E, V_C, and V_{CE}. Lowercase italic subscripts are used to indicate ac quantities of rms, peak, and peak-to-peak currents and voltages: for example, I_c, I_e, I_b, V_c, and V_{ce} (rms values are assumed unless otherwise stated). Instantaneous quantities are represented by both lowercase letters and subscripts such as i_c, i_e, i_b, and v_{ce}. Figure 6–1 illustrates these quantities for a specific voltage waveform.

▶ FIGURE 6–1

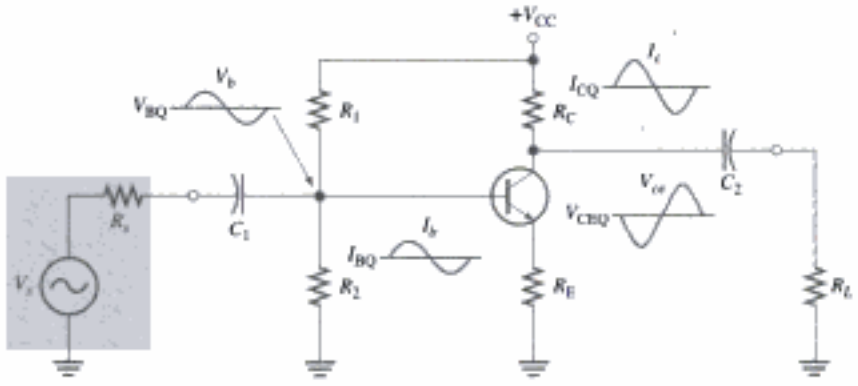
V_{ce} can represent rms, average, peak, or peak-to-peak, but rms will be assumed unless stated otherwise. v_{ce} can be any instantaneous value on the curve.



In addition to currents and voltages, resistances often have different values when a circuit is analyzed from an ac viewpoint as opposed to a dc viewpoint. Lowercase subscripts are used to identify ac resistance values. For example, R_c is the ac collector resistance, and R_C is the dc collector resistance. You will see the need for this distinction later. Resistance values *internal* to the transistor use a lowercase r'. An example is the internal ac emitter resistance, r'_e.

The Linear Amplifier

A voltage-divider biased transistor with a sinusoidal ac source capacitively coupled to the base through C_1 and a load capacitively coupled to the collector through C_2 is shown in Figure 6–2. The coupling capacitors block dc and thus prevent the internal source resistance, R_s, and the load resistance, R_L, from changing the dc bias voltages at the base and collector. The capacitors appear ideally as shorts to the signal voltage. The sinusoidal source voltage causes the base voltage to vary sinusoidally above and below its dc bias level. The resulting variation in base current produces a larger variation in collector current because of the current gain of the transistor.

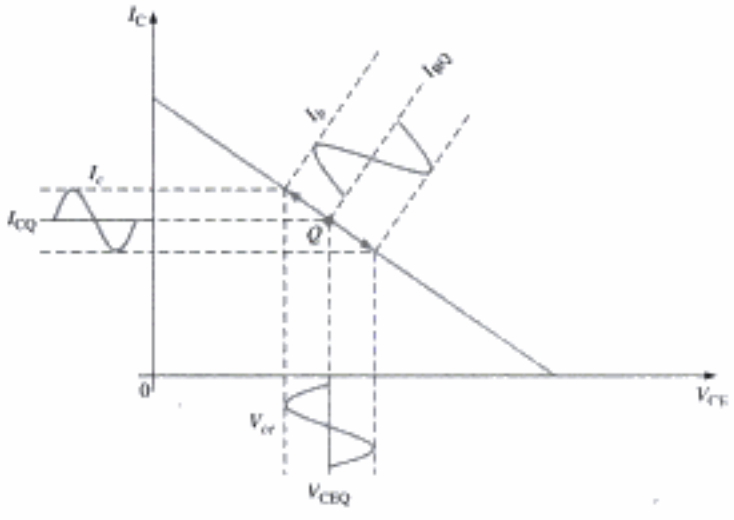


◀ FIGURE 6–2

An amplifier with voltage-divider bias driven by an ac voltage source with an internal resistance, R_s.

As the sinusoidal collector current increases, the collector voltage decreases. The collector current varies above and below its Q-point value in phase with the base current. The sinusoidal collector-to-emitter voltage varies above and below its Q-point value 180° out of phase with the base voltage, as illustrated in Figure 6–2. A transistor always produces a phase inversion between the base voltage and the collector voltage.

A Graphical Picture The operation just described can be illustrated graphically on the ac load line, as shown in Figure 6–3. The sinusoidal voltage at the base produces a base current that varies above and below the Q-point on the ac load line, as shown by the arrows. Lines projected from the peaks of the base current, across to the I_C axis, and down to the V_{CE} axis, indicate the peak-to-peak variations of the collector current and collector-to-emitter voltage, as shown. The ac load line differs from the dc load line because the effective ac collector resistance is R_L in parallel with R_C and is less than the dc collector resistance R_C alone without R_L in parallel. This difference between the dc and the ac load lines is covered in later chapters.



◀ FIGURE 6–3

Graphical operation of the amplifier showing the variation of the base current, collector current, and collector-to-emitter voltage about their dc Q-point values. I_b and I_c are on different scales.

EXAMPLE 6–1

The ac load line operation of a certain amplifier extends 10 μA above and below the Q-point base current value of 50 μA, as shown in Figure 6–4. Determine the resulting peak-to-peak values of collector current and collector-to-emitter voltage from the graph.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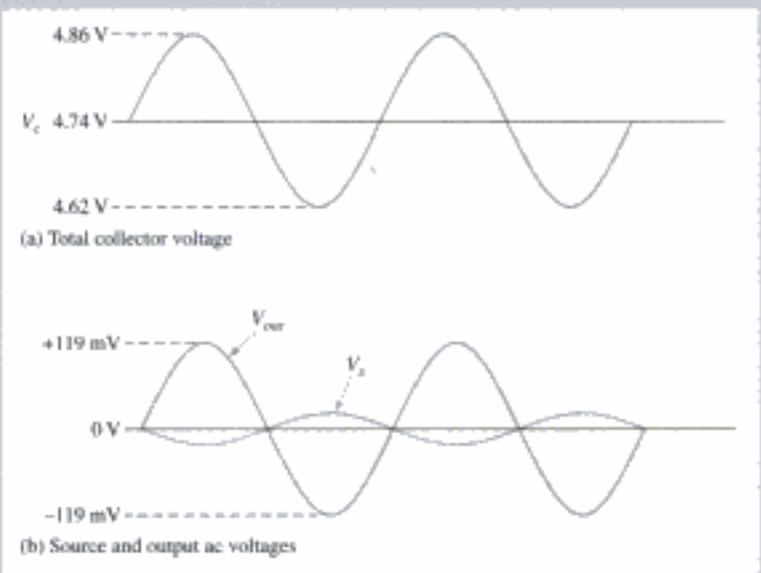
as indicated in Figure 6–23(b). The source voltage is shown to emphasize the phase inversion.

► FIGURE 6–23

Voltages for Figure 6–20.



(a) Total collector voltage

(b) Source and output ac voltages

Current Gain

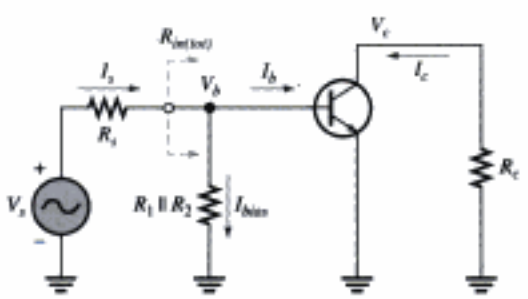
The current gain from base to collector is I_c/I_b or β_{ac}. However, the overall current gain of the common-emitter amplifier is

$$A_i = \frac{I_c}{I_s}$$

Equation 6–10

I_s is the total signal input current produced by the source, part of which (I_b) is base current and part of which (I_{bias}) goes through the bias circuit ($R_1 \mid R_2$), as shown in Figure 6–24. The source "sees" a total resistance of $R_s + R_{in(tot)}$. The total current produced by the source is

$$I_s = \frac{V_s}{R_s + R_{in(tot)}}$$



◄ FIGURE 6–24

Signal currents (directions shown are for the positive half-cycle of V_s).

Power Gain

The overall power gain is the product of the overall voltage gain (A_v') and the overall current gain (A_i).

$$A_p = A_v' A_i$$

Equation 6–11

where $A_v' = V_c/V_s$.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Output Resistance

With the load removed, the output resistance, looking into the emitter of the emitter-follower, is approximated as follows:

$$R_{out} = \left(\frac{R_s}{\beta_{ac}}\right) \| R_E$$

R_s is the resistance of the input source. The derivation of this expression is relatively involved and several simplifying assumptions have been made, as shown in Appendix B. The output resistance is very low, making the emitter-follower useful for driving low-resistance loads.

Current Gain

The overall current gain for the emitter-follower in Figure 6–25 is I_e/I_{in}. You can calculate I_{in} as $V_{in}/R_{in(tot)}$. If the resistance of the parallel combination of the voltage-divider bias resistors R_1 and R_2 is much greater than $R_{in(base)}$, then most of the input current goes into the base; thus, the current gain of the amplifier approaches the current gain of the transistor, β_{ac}, which is equal to I_c/I_b. This is because very little signal current is diverted to the bias resistors. Stated concisely, if

$$R_1 \| R_2 >> \beta_{ac} R_e$$

then

$$A_i = \beta_{ac}$$

Otherwise, the overall current gain is

Equation 6–15

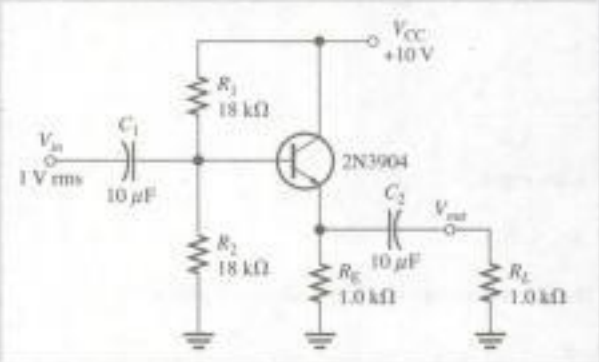
$$A_i = \frac{I_c}{I_{in}}$$

β_{ac} is the maximum achievable current gain in both common-collector and common-emitter amplifiers.

EXAMPLE 6–9

Determine the total input resistance of the emitter-follower in Figure 6–27. Also find the voltage gain, current gain, and power gain in terms of power delivered to the load, R_L. Assume $\beta_{ac} = 175$ and that the capacitive reactances are negligible at the frequency of operation.

► **FIGURE 6–27**



Solution The ac emitter resistance external to the transistor is

$$R_e = R_E \| R_L = 1.0\,\text{k}\Omega \| 1.0\,\text{k}\Omega = 500\,\Omega$$

The approximate resistance, looking in at the base, is

$$R_{in(base)} \cong \beta_{ac} R_e = (175)(500\ \Omega) = 87.5\ \text{k}\Omega$$

The total input resistance i

$$R_{in(tot)} = R_1 \| R_2 \| R_{in(base)} = 18\ \text{k}\Omega \| 18\ \text{k}\Omega \| 87.5\ \text{k}\Omega = \mathbf{8.16\ k\Omega}$$

The voltage gain is $A_v \cong 1$. By using r'_e, you can determine a more precise value of A_v if necessary.

$$V_E = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC} - V_{BE} = (0.5)(10\ \text{V}) - 0.7\ \text{V} = 4.3\ \text{V}$$

Therefore,

$$I_E = \frac{V_E}{R_E} = \frac{4.3\ \text{V}}{1.0\ \text{k}\Omega} = 4.3\ \text{mA}$$

and

$$r'_e \cong \frac{25\ \text{mV}}{I_E} = \frac{25\ \text{mV}}{4.3\ \text{mA}} = 5.8\ \Omega$$

So,

$$A_v = \frac{R_e}{r'_e + R_e} = \frac{500\ \Omega}{505.8\ \Omega} = \mathbf{0.989}$$

The small difference in A_v as a result of considering r'_e is insignificant in most cases.

The overall current gain is $A_i = I_e/I_{in}$. The calculations are as follows:

$$I_e = \frac{V_e}{R_e} = \frac{A_v V_b}{R_e} \cong \frac{1\ \text{V}}{500\ \Omega} = 2\ \text{mA}$$

$$I_{in} = \frac{V_{in}}{R_{in(tot)}} = \frac{1\ \text{V}}{8.16\ \text{k}\Omega} = 123\ \mu\text{A}$$

$$A_i = \frac{I_e}{I_{in}} = \frac{2\ \text{mA}}{123\ \mu\text{A}} = \mathbf{16.3}$$

The overall power gain is

$$A_p \cong A_i = 16.3$$

Since $R_L = R_E$, one-half of the total power is dissipated in R_L. Therefore, in terms of power to the load, the power gain is one-half of the overall power gain.

$$A_{p(load)} = \frac{A_p}{2} = \frac{16.3}{2} = \mathbf{8.15}$$

Power Gain

The common-collector power gain is the product of the voltage gain and the current gain. For the emitter-follower, the overall power gain is approximately equal to the current gain because the voltage gain is approximately 1.

$$A_p = A_v A_i$$

Since $A_v \cong 1$, the overall power gain is

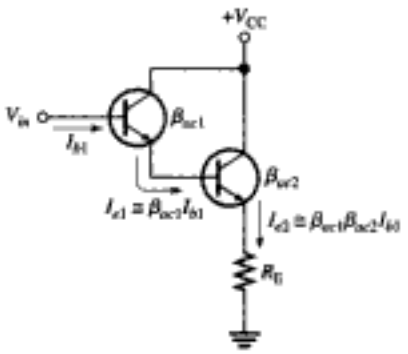
$$A_p \cong A_i$$

Equation 6–16

The Darlington Pair

As you have seen, β_{ac} is a major factor in determining the input resistance of an amplifier. The β_{ac} of the transistor limits the maximum achievable input resistance you can get from a given emitter-follower circuit.

One way to boost input resistance is to use a **darlington pair**, as shown in Figure 6–28. The collectors of two transistors are connected, and the emitter of the first drives the base



◀ **FIGURE 6–28**
A darlington pair multiplies β_{ac}.

of the second. This configuration achieves β_{ac} multiplication as shown in the following steps. The emitter current of the first transistor is

$$I_{e1} \cong \beta_{ac1} I_{b1}$$

This emitter current becomes the base current for the second transistor, producing a second emitter current of

$$I_{e2} \cong \beta_{ac2} I_{e1} = \beta_{ac1}\beta_{ac2} I_{b1}$$

Therefore, the effective current gain of the darlington pair is

$$\beta_{ac} = \beta_{ac1}\beta_{ac2}$$

Neglecting r'_e by assuming that it is much smaller than R_E, the input resistance is

Equation 6–17

$$R_{in} = \beta_{ac1}\beta_{ac2} R_E$$

An Application

The emitter-follower is often used as an interface between a circuit with a high output resistance and a low-resistance load. In such an application, the emitter-follower is called a *buffer*.

Suppose a common-emitter amplifier with a 1.0 kΩ collector resistance must drive a low-resistance load such as an 8 Ω low-power speaker. If the speaker is capacitively coupled to the output of the amplifier, the 8 Ω load appears—to the ac signal—in parallel with the 1.0 kΩ collector resistor. This results in an ac collector resistance of

$$R_c = R_C \,|\, R_L = 1.0\,\text{k}\Omega \,|\, 8\,\Omega = 7.94\,\Omega$$

Obviously, this is not acceptable because most of the voltage gain is lost ($A_v = R_c/r'_e$). For example, if $r'_e = 5\,\Omega$, the voltage gain is reduced from

$$A_v = \frac{R_C}{r'_e} = \frac{1.0\,\text{k}\Omega}{5\,\Omega} = 200$$

EXAMPLE 6–10

In Figure 6–29 for the common-emitter amplifier, $V_{CC} = 12$ V, $R_C = 1.0\ \text{k}\Omega$ and $r'_e = 5\ \Omega$. For the darlington emitter-follower, $R_1 = 10\ \text{k}\Omega$, $R_2 = 22\ \text{k}\Omega$, $R_E = 22\ \Omega$, $R_L = 8\ \Omega$, $V_{CC} = 12$ V, and $\beta_{DC} = \beta_{ac} = 100$ for each transistor.

(a) Determine the voltage gain of the common-emitter amplifier.

(b) Determine the voltage gain of the darlington emitter-follower.

(c) Determine the overall voltage gain and compare to the gain of the common-emitter amplifier driving the speaker directly without the darlington emitter-follower.

Solution **(a)** To determine A_v for the common-emitter amplifier, first find r'_e for the darlington emitter-follower.

$$V_B = \left(\frac{R_2 \| \beta_{DC}^2 R_E}{R_1 + R_2 \| \beta_{DC}^2 R_E}\right) V_{CC} = \left(\frac{20\ \text{k}\Omega}{30\ \text{k}\Omega}\right) 12\ \text{V} = 8.0\ \text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{V_B - 2V_{BE}}{R_E} = \frac{8.0\ \text{V} - 1.4\ \text{V}}{22\ \Omega} = \frac{6.6\ \text{V}}{22\ \Omega} = 300\ \text{mA}$$

$$r'_e = \frac{25\ \text{mV}}{I_E} = \frac{25\ \text{mV}}{300\ \text{mA}} = 83\ \text{m}\Omega$$

Note that R_E must dissipate a power of

$$P_{R_E} = I_E^2 R_E = (300\ \text{mA})^2(22\ \Omega) = 1.98\ \text{W}$$

and transistor Q_2 must dissipate

$$P_{Q2} = (V_{CC} - V_E) I_E = (5.4\ \text{V})(300\ \text{mA}) = 1.62\ \text{W}$$

Next, the ac emitter resistance of the darlington emitter-follower is

$$R_e = R_E \| R_L = 22\ \Omega \| 8\ \Omega = 5.87\ \Omega$$

The total input resistance of the darlington emitter-follower is

$$R_{in(tot)} = R_1 \| R_2 \| \beta_{ac}^2 (r'_e + R_e)$$
$$= 10\ \text{k}\Omega \| 22\ \text{k}\Omega \| 100^2 (83\ \text{m}\Omega + 5.87\ \Omega) = 6.16\ \text{k}\Omega$$

The effective ac collector resistance of the common-emitter amplifier is

$$R_c = R_C \| R_{in(tot)} = 1.0\ \text{k}\Omega \| 6.16\ \text{k}\Omega = 860\ \Omega$$

The voltage gain of the common-emitter amplifier is

$$A_v = \frac{R_c}{r'_e} = \frac{860\ \Omega}{5\ \Omega} = \mathbf{172}$$

(b) The effective ac emitter resistance was found in part (a) to be 5.87 Ω. The voltage gain for the darlington emitter-follower is

$$A_v = \frac{R_e}{r'_e + R_e} = \frac{5.87\ \Omega}{83\ \text{m}\Omega + 5.87\ \Omega} = \mathbf{0.99}$$

(c) The overall voltage gain is

$$A'_v = A_{v(EF)} A_{v(CE)} = (0.99)(172) = \mathbf{170}$$

If the common-emitter amplifier drives the speaker directly, the gain is 1.59 as we previously calculated.

with no load to

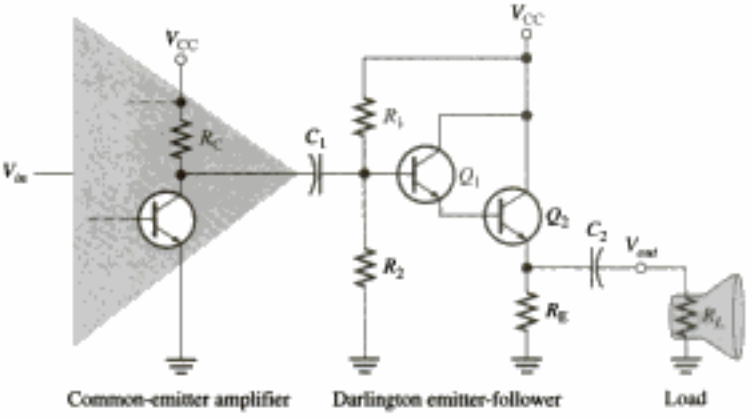
$$A_v = \frac{R_c}{r'_e} = \frac{7.94\ \Omega}{5\ \Omega} = 1.59$$

with an 8 Ω speaker load.

An emitter-follower using a darlington pair can be used to interface the amplifier and the speaker, as shown in Figure 6–29.

▶ FIGURE 6–29

A darlington emitter-follower used as a buffer between a common-emitter amplifier and a low-resistance load such as a speaker.



SECTION 6–4 REVIEW

1. What is a common-collector amplifier called?
2. What is the ideal maximum voltage gain of a common-collector amplifier?
3. What characteristic of the common-collector amplifier makes it a useful circuit?

6–5 THE COMMON-BASE AMPLIFIER

The common-base (**CB**) amplifier provides high voltage gain with a maximum current gain of 1. Since it has a low input resistance, the CB amplifier is the most appropriate type for certain applications where sources tend to have very low-resistance outputs.

A typical **common-base** amplifier is shown in Figure 6–30. The base is the common terminal and is at ac ground because of capacitor C_2. The input signal is capacitively coupled to the emitter. The output is capacitively coupled from the collector to a load resistor.

Voltage Gain

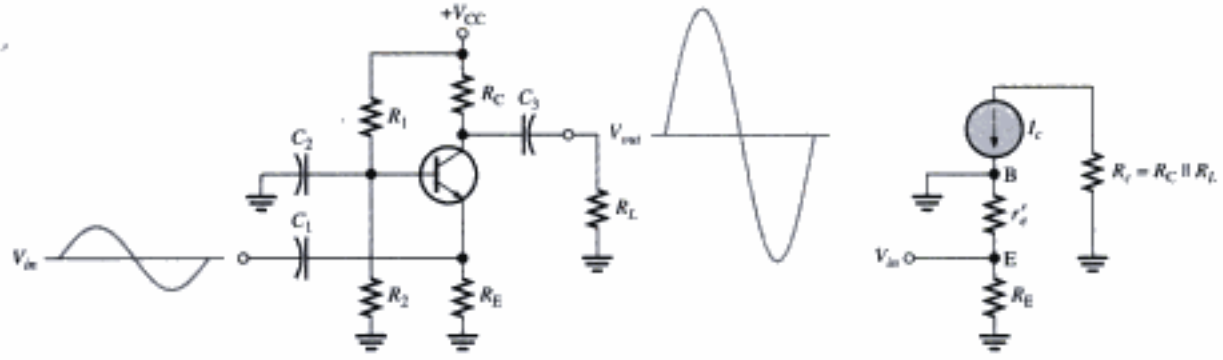
The voltage gain from emitter to collector is developed as follows ($V_{in} = V_e$, $V_{out} = V_c$).

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_c}{V_e} = \frac{I_e R_c}{I_e(r'_e \parallel R_E)} \cong \frac{I_e R_c}{I_e(r'_e \parallel R_E)}$$

If $R_E >> r'_e$, then

Equation 6–18

$$A_v \cong \frac{R_c}{r'_e}$$



(a) Complete circuit with load

(b) AC equivalent model

▲ FIGURE 6–30

Common-base amplifier with voltage-divider bias.

where $R_c = R_C \parallel R_L$. Notice that the gain expression is the same as for the common-emitter amplifier. However, there is no phase inversion from emitter to collector.

Input Resistance

The resistance, looking in at the emitter, is

$$R_{in(emitter)} = \frac{V_{in}}{I_{in}} = \frac{V_e}{I_e} = \frac{I_e(r'_e \parallel R_E)}{I_e}$$ **Equation 6–19**

If $R_E >> r'_e$, then

$$R_{in(emitter)} \cong r'_e$$

R_E is typically much greater than r'_e, so the assumption that $r'_e \parallel R_E \cong r'_e$ is usually valid.

Output Resistance

Looking into the collector, the ac collector resistance, r'_c, appears in parallel with R_C. As you have previously seen in connection with the CE amplifier, r'_c is typically much larger than R_C, so a good approximation for the output resistance is

$$R_{out} \cong R_C$$ **Equation 6–20**

Current Gain

The current gain is the output current divided by the input current. I_c is the ac output current, and I_e is the ac input current. Since $I_c \cong I_e$, the current gain is approximately 1.

$$A_i \cong 1$$ **Equation 6–21**

Power Gain

Since the current gain is approximately 1 for the common-base amplifier and $A_p = A_v A_i$, the power gain is approximately equal to the voltage gain.

$$A_p \cong A_v$$ **Equation 6–22**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6–6 MULTISTAGE AMPLIFIERS

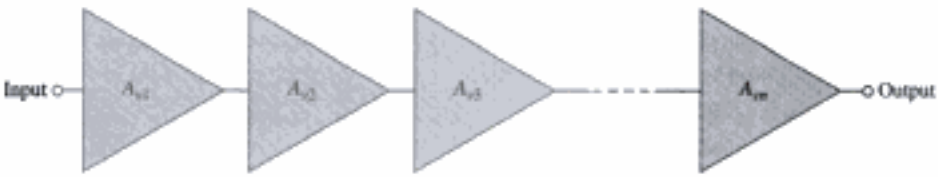
Two or more amplifiers can be connected in a cascaded arrangement with the output of one amplifier driving the input of the next. Each amplifier in a cascaded arrangement is known as a stage. The basic purpose of a multistage arrangement is to increase the overall voltage gain. Although discrete multistage amplifiers are not as common as they once were, a familiarization with this area provides insight into how some circuits affect each other when they are connected together.

Multistage Voltage Gain

The overall voltage gain, A_v', of **cascaded** amplifiers, as shown in Figure 6–32, is the product of the individual voltage gains.

$$A_v' = A_{v1}A_{v2}A_{v3}\cdots A_{vn} \qquad \textbf{Equation 6–23}$$

where n is the number of **stages**.



◀ FIGURE 6–32
Cascaded amplifiers. Each triangular symbol represents a separate amplifier.

Voltage Gain Expressed in Decibels

Amplifier voltage gain is often expressed in **decibels** (dB) as follows:

$$A_{v(\text{dB})} = 20 \log A_v \qquad \textbf{Equation 6–24}$$

This is particularly useful in **multistage** systems because the overall voltage gain in dB is the *sum* of the individual voltage gains in dB.

$$A_{v(\text{dB})}' = A_{v1(\text{dB})} + A_{v2(\text{dB})} + \cdots + A_{vn(\text{dB})} \qquad \textbf{Equation 6–25}$$

EXAMPLE 6–12

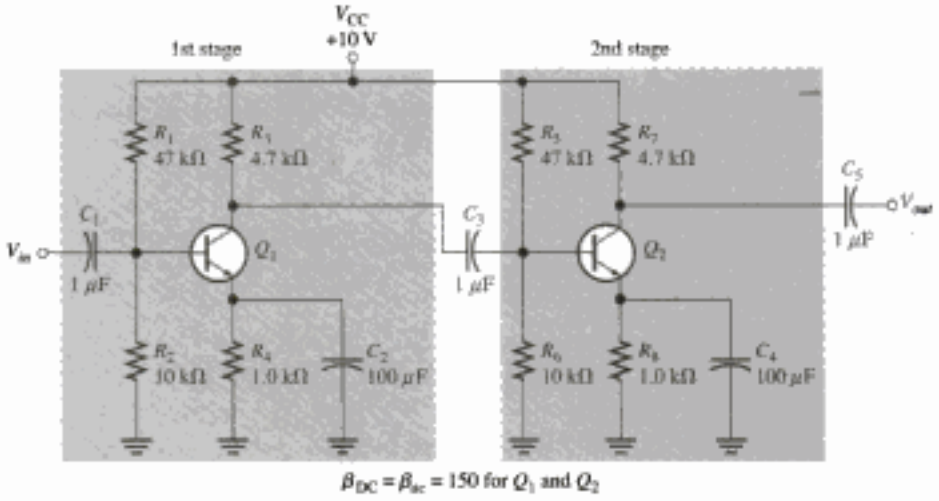
A certain cascaded amplifier arrangement has the following voltage gains: $A_{v1} = 10$, $A_{v2} = 15$, and $A_{v3} = 20$. What is the overall voltage gain? Also express each gain in decibels (dB) and determine the total voltage gain in dB.

Solution

$$A_v' = A_{v1}A_{v2}A_{v3} = (10)(15)(20) = \mathbf{3000}$$
$$A_{v1(\text{dB})} = 20 \log 10 = \mathbf{20.0\ dB}$$
$$A_{v2(\text{dB})} = 20 \log 15 = \mathbf{23.5\ dB}$$
$$A_{v3(\text{dB})} = 20 \log 20 = \mathbf{26.0\ dB}$$
$$A_{v(\text{dB})}' = 20.0\ \text{dB} + 23.5\ \text{dB} + 26.0\ \text{dB} = \mathbf{69.5\ dB}$$

▶ FIGURE 6–33

A two-stage common-emitter amplifier.



Multistage Amplifier Analysis

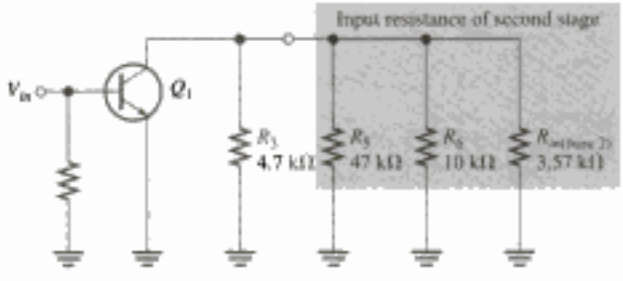
For purposes of illustration, we will use the two-stage capacitively coupled amplifier in Figure 6–33. Notice that both stages are identical common-emitter amplifiers with the output of the first stage capacitively coupled to the input of the second stage. Capacitive coupling prevents the dc bias of one stage from affecting that of the other but allows the ac signal to pass without attenuation because $X_C \cong 0\ \Omega$ at the frequency of operation. Notice, also, that the transistors are labeled Q_1 and Q_2.

Loading Effects In determining the voltage gain of the first stage, you must consider the loading effect of the second stage. Because the coupling capacitor C_3 effectively appears as a short at the signal frequency, the total input resistance of the second stage presents an ac load to the first stage.

Looking from the collector of Q_1, the two biasing resistors in the second stage, R_5 and R_6, appear in parallel with the input resistance at the base of Q_2. In other words, the signal at the collector of Q_1 "sees" R_3, R_5, R_6, and $R_{in(base2)}$ of the second stage all in parallel to ac ground. Thus, the effective ac collector resistance of Q_1 is the total of all these resistances in parallel, as Figure 6–34 illustrates. The voltage gain of the first stage is reduced by the loading of the second stage because the effective ac collector resistance of the first stage is less than the actual value of its collector resistor, R_3. Remember that $A_v = R_c/r'_e$.

▶ FIGURE 6–34

AC equivalent of first stage in Figure 6–33, showing loading from second stage input resistance.



Voltage Gain of the First Stage The ac collector resistance of the first stage is

$$R_{c1} = R_3 \,|\, R_5 \,\|\, R_6 \,\|\, R_{in\,(base2)}$$

Remember that lowercase italic subscripts denote ac quantities such as for R_c.

You can verify that $I_E = 1.05$ mA, $r'_e = 23.8\ \Omega$, and $R_{in(base2)} = 3.57$ kΩ. The effective ac collector resistance of the first stage is as follows:

$$R_{c1} = 4.7\ \text{k}\Omega \,\|\, 47\ \text{k}\Omega \,\|\, 10\ \text{k}\Omega \,\|\, 3.57\ \text{k}\Omega = 1.63\ \text{k}\Omega$$

Therefore, the base-to-collector voltage gain of the first stage is

$$A_{v1} = \frac{R_{c1}}{r'_e} = \frac{1.63\ \text{k}\Omega}{23.8\ \Omega} = 68.5$$

Voltage Gain of the Second Stage The second stage has no load resistor, so the ac collector resistance is R_7, and the gain is

$$A_{v2} = \frac{R_7}{r'_e} = \frac{4.7\ \text{k}\Omega}{23.8\ \Omega} = 197$$

Compare this to the gain of the first stage, and notice how much the loading from the second stage reduced the gain.

Overall Voltage Gain The overall amplifier gain with no load on the output is

$$A'_v = A_{v1}A_{v2} = (68.5)(197) = 13{,}495$$

If an input signal of 100 μV, for example, is applied to the first stage and if there is no attenuation in the input base circuit due to the source resistance, an output from the second stage of (100 μV)(13,495) $\cong$ 1.35 V will result. The overall voltage gain can be expressed in dB as follows:

$$A'_{v(\text{dB})} = 20 \log(13{,}495) = 82.6\ \text{dB}$$

DC Voltages in the Capacitively Coupled Multistage Amplifier Since both stages in Figure 6–33 are identical, the dc voltages for Q_1 and Q_2 are the same. Since $\beta_{DC}R_4 >> R_2$ and $\beta_{DC}R_8 >> R_6$, the dc base voltage for Q_1 and Q_2 is

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{10\ \text{k}\Omega}{57\ \text{k}\Omega}\right)10\ \text{V} = 1.75\ \text{V}$$

The dc emitter and collector voltages are as follows:

$$V_E = V_B - 0.7\ \text{V} = 1.05\ \text{V}$$

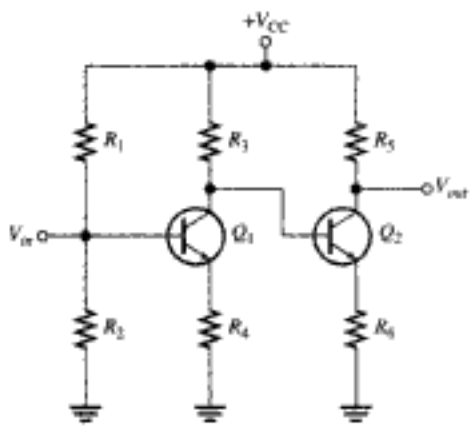
$$I_E = \frac{V_E}{R_4} = \frac{1.05\ \text{V}}{1.0\ \text{k}\Omega} = 1.05\ \text{mA}$$

$$I_C \cong I_E = 1.05\ \text{mA}$$

$$V_C = V_{CC} - I_C R_3 = 10\ \text{V} - (1.05\ \text{mA})(4.7\ \text{k}\Omega) = 5.07\ \text{V}$$

Direct-Coupled Multistage Amplifiers

A basic two-stage, direct-coupled amplifier is shown in Figure 6–35. Notice that there are no coupling or bypass capacitors in this circuit. The dc collector voltage of the first stage provides the base-bias voltage for the second stage. Because of the direct coupling, this type of amplifier has a better low-frequency response than the capacitively coupled type in



◀ FIGURE 6–35

A basic two-stage direct-coupled amplifier.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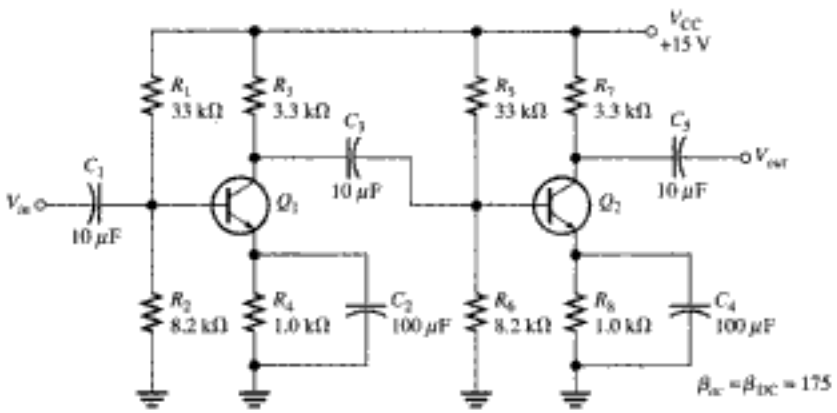
30. If the multistage amplifier in Figure 6–42 is driven by a 75 Ω, 50 μV source and the second stage is loaded with an R_L = 18 kΩ, determine

(a) voltage gain of each stage

(b) overall voltage gain

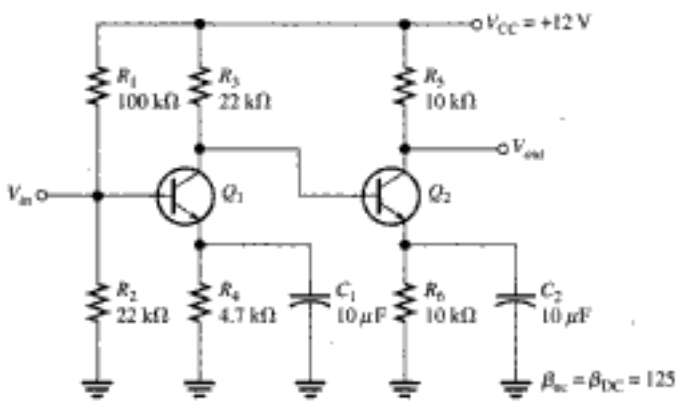
(c) Express the gains found in (a) and (b) in dB.

◀ **FIGURE 6–42**



31. Figure 6–43 shows a direct-coupled (that is, with no coupling capacitors between stages) two-stage amplifier. The dc bias of the first stage sets the dc bias of the second. Determine all dc voltages for both stages and the overall ac voltage gain.

◀ **FIGURE 6–43**



32. Express the following voltage gains in dB:

(a) 12 **(b)** 50 **(c)** 100 **(d)** 2500

33. Express the following voltage gains in dB as standard voltage gains:

(a) 3 dB **(b)** 6 dB **(c)** 10 dB **(d)** 20 dB **(e)** 40 dB

ANSWERS

SECTION REVIEWS

SECTION 6–1 *Amplifier Operation*

1. Positive, negative

2. V_{CE} is a dc quantity and V_{ce} is an ac quantity.

3. R_e is the external emitter ac resistance, r'_e is the internal emitter ac resistance.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7

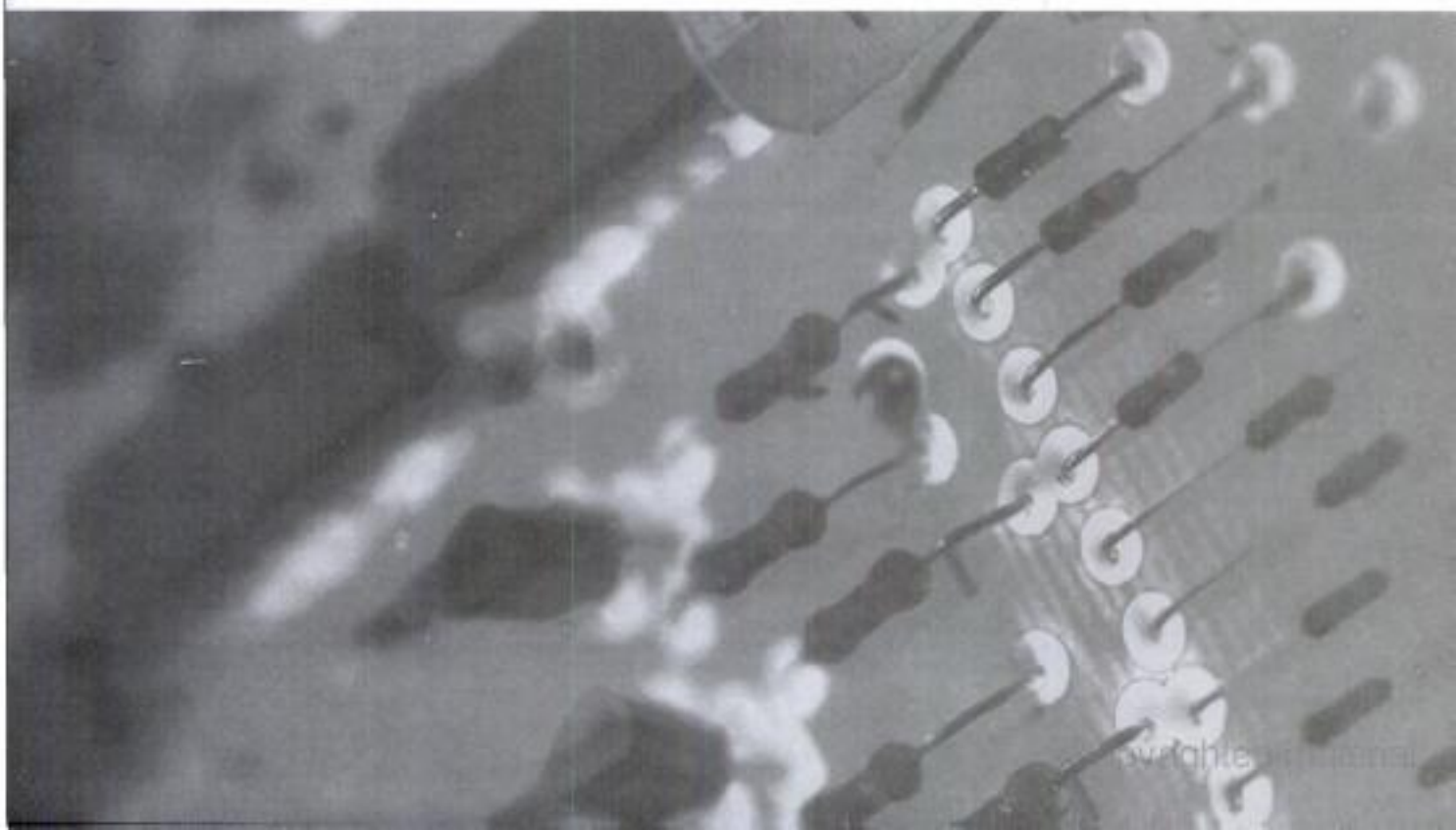
FIELD-EFFECT TRANSISTORS (FETs)

CHAPTER OUTLINE

INTRODUCTION

Field-effect transistors (FETs) are unipolar devices because, unlike bipolar junction transistors (BJTs) that use both electron and hole current, they operate only with one type of charge carrier. The two main types of FETs are the junction field-effect transistor (JFET) and the metal oxide semiconductor field-effect transistor (MOSFET).

Recall that a BJT is a current-controlled device; that is, the base current controls the amount of collector current. A FET is different. It is a voltage-controlled device, where the voltage between two of the terminals (gate and source) controls the current through the device. As you will learn, a major feature of FETs is their very high input resistance.

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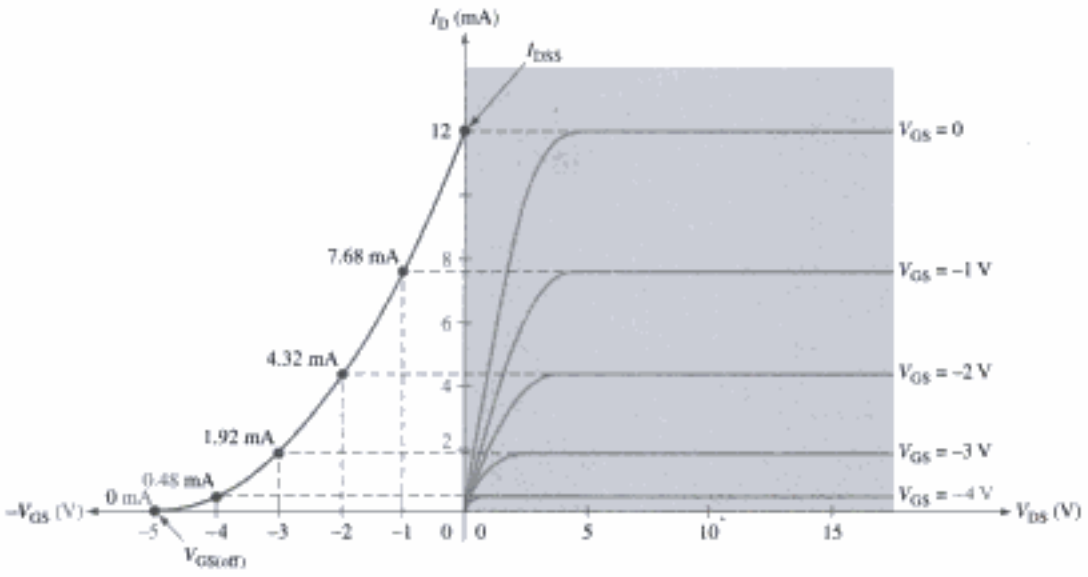

▲ FIGURE 7–13

Example of the development of an *n*-channel JFET transfer characteristic curve (black) from the JFET drain characteristic curves (gray).

EXAMPLE 7–3

The JFET has typically $I_{DSS} = 9$ mA and $V_{GS(off)} = -8$ V (maximum). Using these values, determine the drain current for $V_{GS} = 0$ V, -1 V, and -4 V.

Solution For $V_{GS} = 0$ V,

$$I_D = I_{DSS} = \mathbf{9\ mA}$$

For $V_{GS} = -1$ V, use Equation 7–1.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (9\text{ mA})\left(1 - \frac{-1\text{ V}}{-8\text{ V}}\right)^2$$
$$= (9\text{ mA})(1 - 0.125)^2 = (9\text{ mA})(0.766) = \mathbf{6.89\ mA}$$

For $V_{GS} = -4$ V,

$$I_D = (9\text{ mA})\left(1 - \frac{-4\text{ V}}{-8\text{ V}}\right)^2 = (9\text{ mA})(1 - 0.5)^2 = (9\text{ mA})(0.25) = \mathbf{2.25\ mA}$$

JFET Forward Transconductance

The forward **transconductance** (transfer conductance), g_m, is the change in drain current (ΔI_D) for a given change in gate-to-source voltage (ΔV_{GS}) with the drain-to-source voltage constant. It is expressed as a ratio and has the unit of siemens (S).

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Other common designations for this parameter are g_fs and y_{fs} (forward transfer admittance). The g_m is important in FET amplifiers as a major factor in determining the voltage gain.

Because the transfer characteristic curve for a JFET is nonlinear, g_m varies in value depending on the location on the curve as set by V_{GS}. The value for g_m is greater near


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The source voltage is

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 and R_2 as expressed by the following equation using the voltage-divider formula:

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$$

The gate-to-source voltage is

$$V_{GS} = V_G - V_S$$

and the source voltage is

$$V_S = V_G - V_{GS}$$

The drain current can be expressed as

$$I_D = \frac{V_S}{R_S}$$

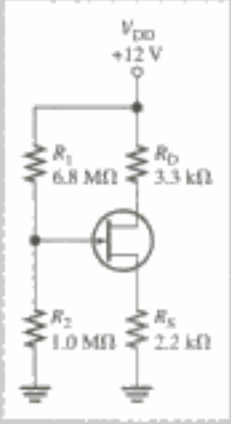
Substituting for V_S,

$$I_D = \frac{V_G - V_{GS}}{R_S}$$

EXAMPLE 7–11

Determine I_D and V_{GS} for the JFET with voltage-divider bias in Figure 7–23, given that for this particular JFET the internal parameter values are such that $V_D \cong 7$ V.

▶ **FIGURE 7–23**



Solution

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12\text{ V} - 7\text{ V}}{3.3\text{ k}\Omega} = \frac{5\text{ V}}{3.3\text{ k}\Omega} = \mathbf{1.52\text{ mA}}$$

Calculate the gate-to-source voltage as follows:

$$V_S = I_D R_S = (1.52\text{ mA})(2.2\text{ k}\Omega) = 3.34\text{ V}$$

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} = \left(\frac{1.0\text{ M}\Omega}{7.8\text{ M}\Omega}\right) 12\text{ V} = 1.54\text{ V}$$

$$V_{GS} = V_G - V_S = 1.54\text{ V} - 3.34\text{ V} = \mathbf{-1.8\text{ V}}$$

If V_D had not been given in this example, the Q-point values could not have been found without the transfer characteristic curve.

Graphical Analysis of a JFET with Voltage-Divider Bias

An approach similar to the one used for self-bias can be used with voltage-divider bias to graphically determine the Q-point of a circuit on the transfer characteristic curve.

In a JFET with voltage-divider bias when $I_D = 0$, V_{GS} is not zero, as in the self-biased case, because the voltage divider produces a voltage at the gate independent of the drain current. The voltage-divider dc load line is determined as follows.

For $I_D = 0$,

$$V_S = I_D R_S = (0)R_S = 0\text{ V}$$

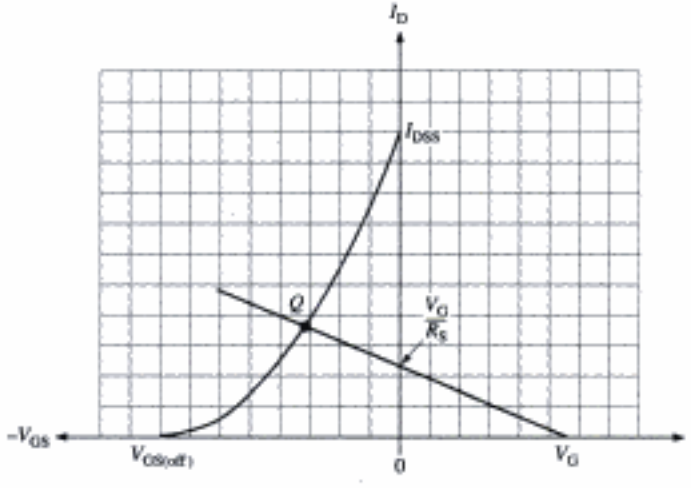
$$V_{GS} = V_G - V_S = V_G - 0\text{ V} = V_G$$

Therefore, one point on the line is at $I_D = 0$ and $V_{GS} = V_G$.

For $V_{GS} = 0$,

$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{V_G}{R_S}$$

A second point on the line is at $I_D = V_G/R_S$ and $V_{GS} = 0$. The generalized dc load line is shown in Figure 7–24. The point at which the load line intersects the transfer characteristic curve is the Q-point.



◀ FIGURE 7–24

Generalized dc load line for a JFET with voltage-divider bias.

EXAMPLE 7–12

Determine the approximate Q-point for the JFET with voltage-divider bias in Figure 7–25(a), given that this particular device has a transfer characteristic curve as shown in Figure 7–25(b).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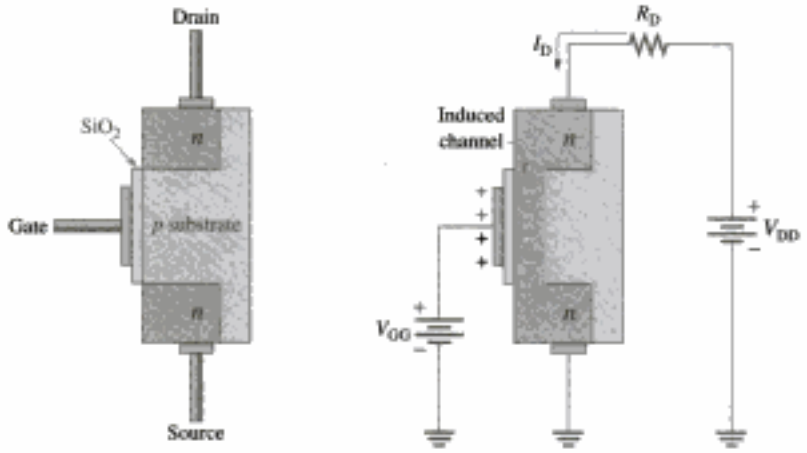
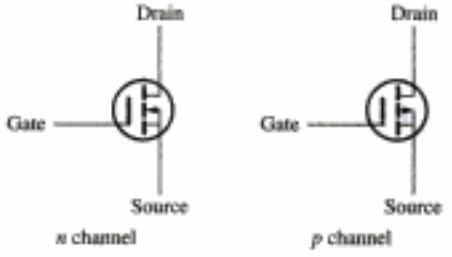
▶ FIGURE 7–31

Representation of the basic E-MOSFET construction and operation (*n*-channel).



▶ FIGURE 7–32

E-MOSFET schematic symbols.



SECTION 7–4 REVIEW

1. Name the two basic types of MOSFETs.
2. If the gate-to-source voltage in an *n*-channel depletion MOSFET is made more negative, does the drain current increase or decrease?
3. If the gate-to-source voltage in an *n*-channel E-MOSFET is made more positive, does the drain current increase or decrease?

7–5 MOSFET CHARACTERISTICS AND PARAMETERS

Much of the discussion concerning JFET characteristics and parameters applies equally to MOSFETs. In this section, MOSFET parameters are discussed.

D-MOSFET Transfer Characteristic

As previously discussed, the D-MOSFET can operate with either positive or negative gate voltages. This is indicated on the general transfer characteristic curves in Figure 7–33 for both *n*-channel and *p*-channel MOSFETs. The point on the curves where $V_{GS} = 0$ corresponds to I_{DSS}. The point where $I_D = 0$ corresponds to $V_{GS(off)}$. As with the JFET, $V_{GS(off)} = -V_P$.

The square-law expression in Equation 7–1 for the JFET curve also applies to the D-MOSFET curve, as Example 7–13 demonstrates.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E-MOSFET does not have a significant I_{DSS} parameter, as do the JFET and the D-MOSFET. Notice also that there is ideally no drain current until V_{GS} reaches a certain nonzero value called the *threshold voltage*, $V_{GS(th)}$.

The equation for the parabolic transfer characteristic curve of the E-MOSFET differs from that of the JFET and the D-MOSFET because the curve starts at $V_{GS(th)}$ rather than $V_{GS(off)}$ on the horizontal axis and never intersects the vertical axis. The equation for the E-MOSFET transfer characteristic curve is

Equation 7–4

$$I_D = K(V_{GS} - V_{GS(th)})^2$$

The constant K depends on the particular MOSFET and can be determined from the data sheet by taking the specified value of I_D, called $I_{D(on)}$, at the given value of V_{GS} and substituting the values into Equation 7–4.

EXAMPLE 7–14

A 2N7008 E-MOSFET gives $I_{D(on)} = 500$ mA (minimum) at $V_{GS} = 10$ V and $V_{GS(th)} = 1$ V. Determine the drain current for $V_{GS} = 5$ V.

Solution First, solve for K using Equation 7–4.

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{500\text{ mA}}{(10\text{ V} - 1\text{ V})^2} = \frac{500\text{ mA}}{81\text{ V}^2} = 6.17\text{ mA/V}^2$$

Next, using the value of K, calculate I_D for $V_{GS} = 5$ V.

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (6.17\text{ mA/V}^2)(5\text{ V} - 1\text{ V})^2 = \mathbf{98.7\text{ mA}}$$

SECTION 7–5 REVIEW

1. What is the major difference in construction of the D-MOSFET and the E-MOSFET?
2. Name two parameters of an E-MOSFET that are not specified for D-MOSFETs?
3. What is ESD?

7–6 MOSFET BIASING

Three ways to bias a MOSFET are zero-bias, voltage-divider bias, and drain-feedback bias. Biasing is important in FET amplifiers, which you will study in the next chapter.

D-MOSFET Bias

Recall that D-MOSFETs can be operated with either positive or negative values of V_{GS}. A simple bias method is to set $V_{GS} = 0$ so that an ac signal at the gate varies the gate-to-source voltage above and below this 0 V bias point. A MOSFET with zero bias is shown in Figure 7–35(a). Since $V_{GS} = 0$, $I_D = I_{DSS}$ as indicated. The drain-to-source voltage is expressed as follows:

$$V_{DS} = V_{DD} - I_{DSS}R_D$$

The purpose of R_G is to accommodate an ac signal input by isolating it from ground, as shown in Figure 7–35(b). Since there is no dc gate current, R_G does not affect the zero gate-to-source bias.


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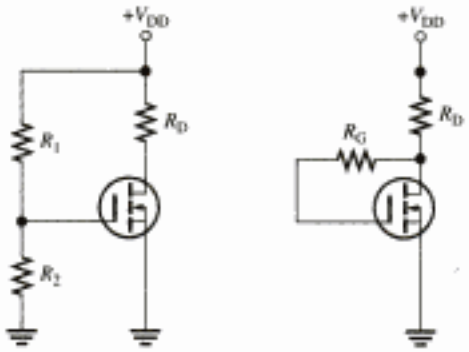
▶ FIGURE 7–37

Common E-MOSFET biasing arrangements.

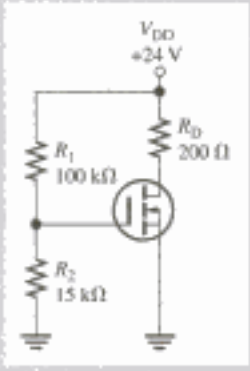


(a) Voltage-divider bias (b) Drain-feedback bias

EXAMPLE 7–16

Determine V_{GS} and V_{DS} for the E-MOSFET circuit in Figure 7–38. Assume this particular MOSFET has minimum values of $I_{D(on)} = 200$ mA at $V_{GS} = 4$ V and $V_{GS(th)} = 2$ V.

▶ FIGURE 7–38



Solution For the E-MOSFET in Figure 7–38, the gate-to-source voltage is

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{15\text{ k}\Omega}{115\text{ k}\Omega}\right)24\text{ V} = \mathbf{3.13\text{ V}}$$

To determine V_{DS}, first find K using the minimum value of $I_{D(on)}$ and the specified voltage values.

$$K = \frac{I_{D(on)}}{(V_{GS} - V_{GS(th)})^2} = \frac{200\text{ mA}}{(4\text{ V} - 2\text{ V})^2} = \frac{200\text{ mA}}{4\text{ V}^2} = 50\text{ mA/V}^2$$

Now calculate I_D for $V_{GS} = 3.13$ V.

$$I_D = K(V_{GS} - V_{GS(th)})^2 = (50\text{ mA/V}^2)(3.13\text{ V} - 2\text{ V})^2$$
$$= (50\text{ mA/V}^2)(1.13\text{ V})^2 = 63.8\text{ mA}$$

Finally, calculate V_{DS}.

$$V_{DS} = V_{DD} - I_D R_D = 24\text{ V} - (63.8\text{ mA})(200\ \Omega) = \mathbf{11.2\text{ V}}$$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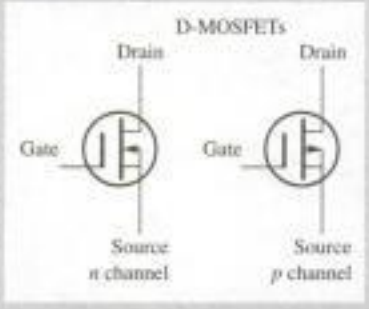
SUMMARY OF FIELD-EFFECT TRANSISTORS, *continued*

D-MOSFETs

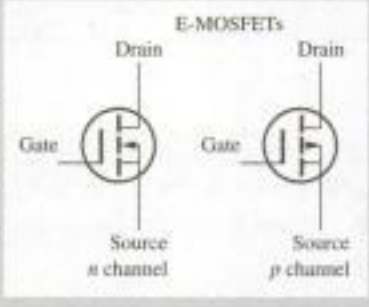


Except that it can be operated in enhancement mode, the D-MOSFET characteristics are the same as JFET.

- *Depletion mode:*
  - *n* channel: V_{GS} negative
  - *p* channel: V_{GS} positive
- *Enhancement mode:*
  - *n* channel: V_{GS} positive
  - *p* channel: V_{GS} negative
- V_{GS} controls I_D.
- Value of V_{GS} at which I_D becomes zero is the cutoff voltage, $V_{GS(off)}$.
- I_{DSS} is drain current when $V_{GS} = 0$.
- Transfer characteristic:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

E-MOSFETs



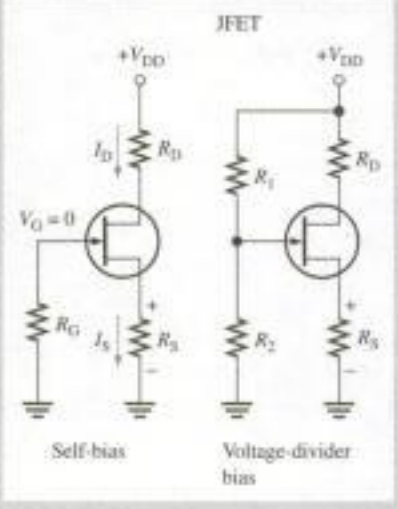
There is no depletion mode and characteristics differ from D-MOSFET.

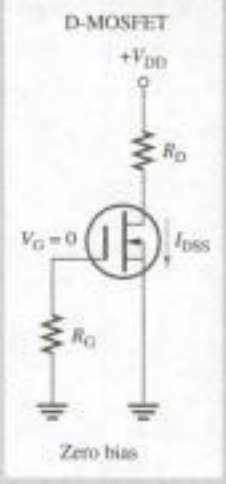
- *Enhancement mode:*
  - *n* channel: V_{GS} positive
  - *p* channel: V_{GS} negative
- V_{GS} controls I_D.
- Value of V_{GS} at which I_D begins is the threshold voltage, $V_{GS(th)}$.
- Transfer characteristic:

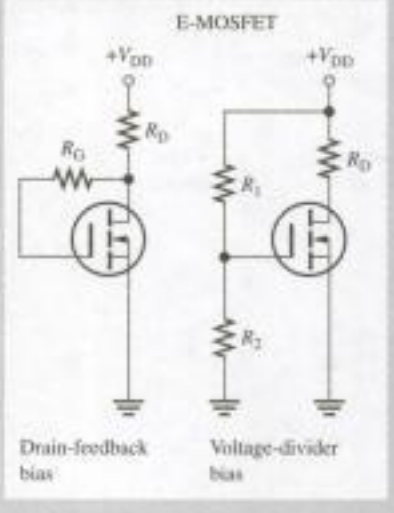
$$I_D = K(V_{GS} - V_{GS(th)})^2$$

- K in formula can be calculated by substituting data sheet values $I_{D(on)}$ for I_D and V_{GS} at which $I_{D(on)}$ is specified for V_{GS}.

FET BIASING (voltage polarities and current directions reverse for *p* channel)





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8. If R_2 in Figure 7–39 opens, V_{GS} will

(a) increase **(b)** decrease **(c)** not change

9. The JFET is

(a) a unipolar device **(b)** a voltage-controlled device

(c) a current-controlled device **(d)** answers (a) and (c)

(e) answers (a) and (b)

10. The channel of a JFET is between the

(a) gate and drain **(b)** drain and source **(c)** gate and source **(d)** input and output

11. A JFET always operates with

(a) the gate-to-source *pn* junction reverse-biased

(b) the gate-to-source *pn* junction forward-biased

(c) the drain connected to ground

(d) the gate connected to the source

12. For $V_{GS} = 0$ V, the drain current becomes constant when V_{DS} exceeds

(a) cutoff **(b)** V_{DD} **(c)** V_P **(d)** 0 V

13. The constant-current area of a FET lies between

(a) cutoff and saturation **(b)** cutoff and pinch-off

(c) 0 and I_{DSS} **(d)** pinch-off and breakdown

14. I_{DSS} is

(a) the drain current with the source shorted **(b)** the drain current at cutoff

(c) the maximum possible drain current **(d)** the midpoint drain current

15. Drain current in the constant-current area increases when

(a) the gate-to-source bias voltage decreases

(b) the gate-to-source bias voltage increases

(c) the drain-to-source voltage increases

(d) the drain-to-source voltage decreases

16. In a certain FET circuit, $V_{GS} = 0$ V, $V_{DD} = 15$ V, $I_{DSS} = 15$ mA, and $R_D = 470\ \Omega$. If R_D is decreased to 330 Ω, I_{DSS} is

(a) 19.5 mA **(b)** 10.5 mA **(c)** 15 mA **(d)** 1 mA

17. At cutoff, the JFET channel is

(a) at its widest point **(b)** completely closed by the depletion region

(c) extremely narrow **(d)** reverse-biased

18. A certain JFET data sheet gives $V_{GS(off)} = -4$ V. The pinch-off voltage, V_P,

(a) cannot be determined **(b)** is −4 V **(c)** depends on V_{GS} **(d)** is +4 V

19. The JFET in Question 10

(a) is an *n* channel **(b)** is a *p* channel **(c)** can be either

20. For a certain JFET, $I_{GSS} = 10$ nA at $V_{GS} = 10$ V. The input resistance is

(a) 100 MΩ **(b)** 1 MΩ **(c)** 1000 MΩ **(d)** 1000 mΩ

21. For a certain *p*-channel JFET, $V_{GS(off)} = 8$ V. The value of V_{GS} for an approximate midpoint bias is

(a) 4 V **(b)** 0 V **(c)** 1.25 V **(d)** 2.34 V

22. A MOSFET differs from a JFET mainly because

(a) of the power rating **(b)** the MOSFET has two gates

(c) the JFET has a *pn* junction **(d)** MOSFETs do not have a physical channel

23. A certain D-MOSFET is biased at $V_{GS} = 0$ V. Its data sheet specifies $I_{DSS} = 20$ mA and $V_{GS(off)} = -5$ V. The value of the drain current

(a) is 0 A **(b)** cannot be determined **(c)** is 20 mA


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SECTION 7–4 The MOSFET

28. Draw the schematic symbols for *n*-channel and *p*-channel D-MOSFETs and E-MOSFETs. Label the terminals.

29. In what mode is an *n*-channel D-MOSFET with a positive V_{GS} operating?

30. Describe the basic difference between a D-MOSFET and an E-MOSFET.

31. Explain why both types of MOSFETs have an extremely high input resistance at the gate.

SECTION 7–5 MOSFET Characteristics and Parameters

32. The data sheet for a certain D-MOSFET gives $V_{GS(off)} = -5$ V and $I_{DSS} = 8$ mA.

(a) Is this device *p* channel or *n* channel?

(b) Determine I_D for values of V_{GS} ranging from -5 V to $+5$ V in increments of 1 V.

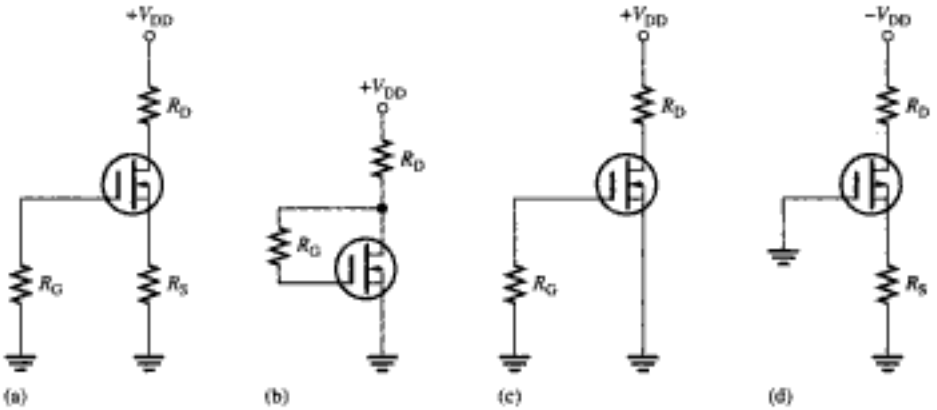
(c) Plot the transfer characteristic curve using the data from part (b).

33. Determine I_{DSS}, given $I_D = 3$ mA, $V_{GS} = -2$ V, and $V_{GS(off)} = -10$ V.

34. For an E-MOSFET, $I_{D(on)} = 10$ mA at $V_{GS} = -12$ V and $V_{GS(th)} = -3$ V. Find I_D when $V_{GS} = -6$ V.

SECTION 7–6 MOSFET Biasing

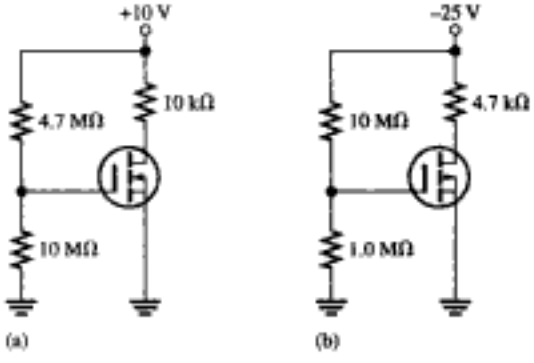
35. Determine in which mode (depletion, enhancement or neither) each D-MOSFET in Figure 7–49 is biased.



▲ **FIGURE 7–49**

36. Each E-MOSFET in Figure 7–50 has a $V_{GS(th)}$ of $+5$ V or -5 V, depending on whether it is an *n*-channel or a *p*-channel device. Determine whether each MOSFET is on or off.

▶ **FIGURE 7–50**

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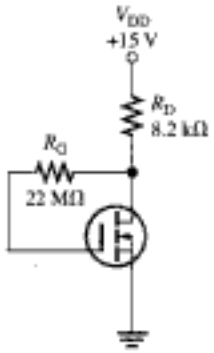
40. Determine the actual gate-to-source voltage in Figure 7–54 by taking into account the gate leakage current, I_{GSS}. Assume that I_{GSS} is 50 pA and I_D is 1 mA under the existing bias conditions.

► **FIGURE 7–54**



ANSWERS

SECTION REVIEWS

SECTION 7–1 The JFET

1. Drain, source, and gate
2. An *n*-channel JFET requires a negative V_{GS}.
3. I_D is controlled by V_{GS}.

SECTION 7–2 JFET Characteristics and Parameters

1. When $V_{DS} = 7$ V at pinch-off and $V_{GS} = 0$ V, $V_P = -7$ V.
2. As V_{GS} increases negatively, I_D decreases.
3. For $V_P = -3$ V, $V_{GS(off)} = +3$ V.

SECTION 7–3 JFET Biasing

1. A *p*-channel JFET requires a positive V_{GS}.
2. $V_{GS} = V_G - V_S = 0\text{ V} - (8\text{ mA})(1.0\text{ k}\Omega) = -8\text{ V}$
3. $V_{GS} = V_G - V_S = 3\text{ V} - 5\text{ V} = -2\text{ V}$

SECTION 7–4 The MOSFET

1. Depletion MOSFET (D-MOSFET) and enhancement MOSFET (E-MOSFET)
2. I_D decreases.
3. I_D increases.

SECTION 7–5 MOSFET Characteristics and Parameters

1. The D-MOSFET has a structural channel; the E-MOSFET does not.
2. $V_{GS(th)}$ and K are not specified for D-MOSFETs.
3. ESD is ElectroStatic Discharge.

SECTION 7–6 MOSFET Biasing

1. When $V_{GS} = 0$ V, the drain current is equal to I_{DSS}.
2. V_{GS} must exceed $V_{GS(th)} = 2$ V for conduction to occur.

OBJECTIVE TYPE QUESTIONS

1. (b) **2.** (c) **3.** (b) **4.** (b) **5.** (c) **6.** (b) **7.** (a) **8.** (a) **9.** (e) **10.** (b)
11. (a) **12.** (c) **13.** (d) **14.** (c) **15.** (a) **16.** (c) **17.** (b) **18.** (d) **19.** (a) **20.** (c)
21. (d) **22.** (c) **23.** (c) **24.** (b) **25.** (a) **26.** (c)

8

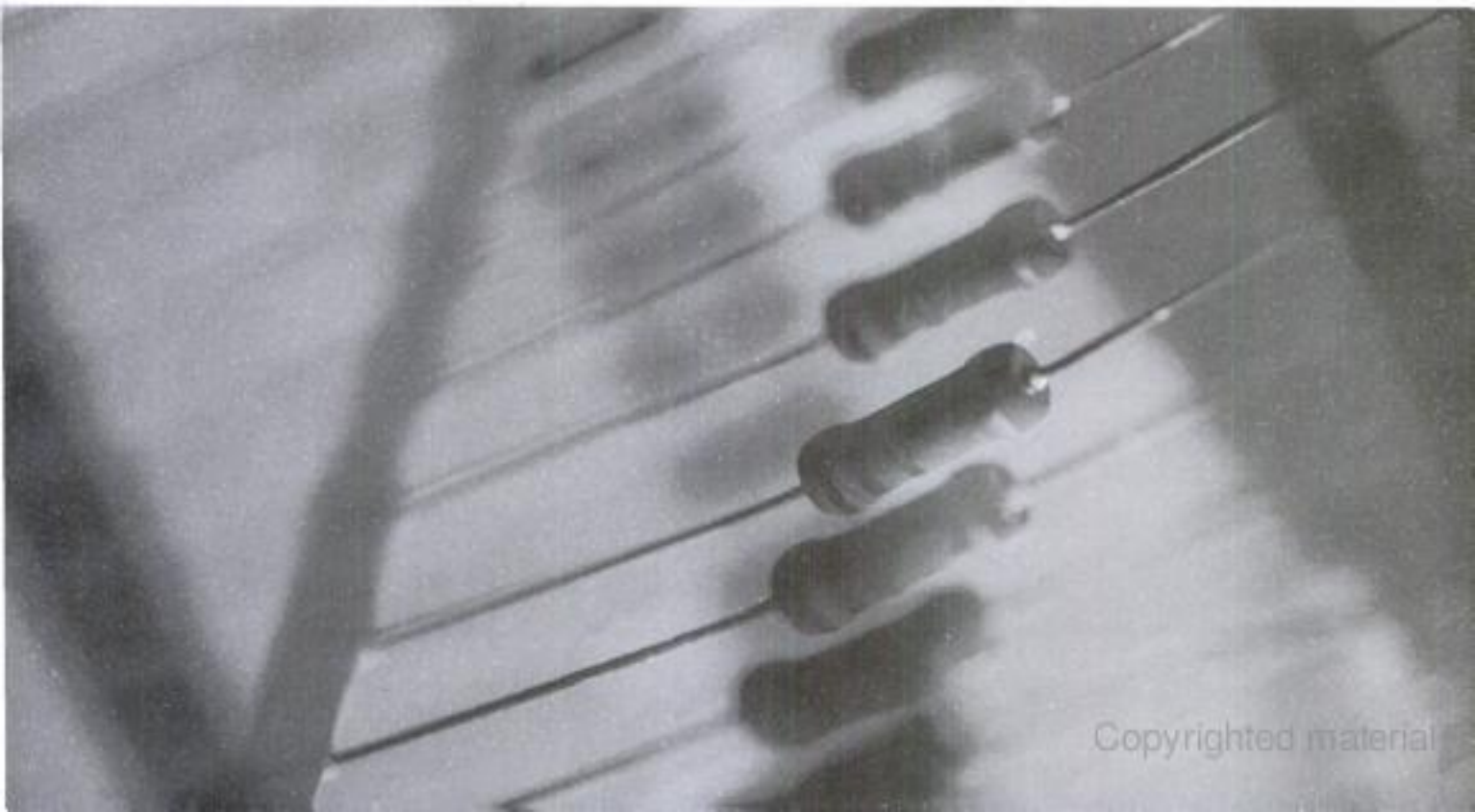
FET AMPLIFIERS

CHAPTER OUTLINE

INTRODUCTION

The things you learned about biasing FETs are carried forward into this chapter where FET circuits are used as small-signal amplifiers. Because of their high input resistance and other characteristics, FETs are often preferred over BJTs (bipolar junction transistors) for certain types of applications.

Many of the concepts that relate to amplifiers using BJTs apply as well to FET amplifiers. The three FET amplifier configurations are common-source, common-drain, and common-gate. These are analogous to the common-emitter, common-collector, and common-base configurations in BJT amplifiers.



8–1 FET AMPLIFICATION

In this section, you will learn about the amplification properties of FETs and how the gain is affected by certain parameters and circuit components. We will simplify the FET to an equivalent circuit to get to the essence of its operation.

The transconductance is defined as $g_m = \Delta I_D/\Delta V_{GS}$. In ac quantities, $g_m = I_d/V_{gs}$. By rearranging the terms,

Equation 8–1

$$I_d = g_m V_{gs}$$

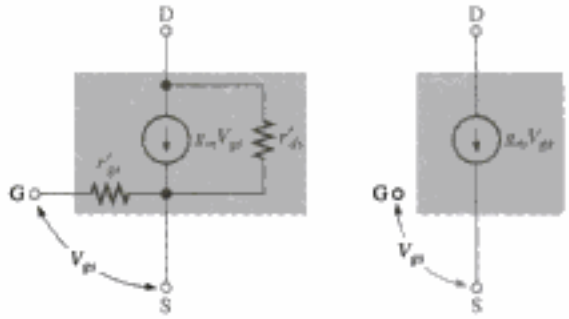
This equation states that the output current, I_d, equals the input voltage, V_{gs}, multiplied by the transconductance, g_m.

Equivalent Circuit

A FET equivalent circuit representing the relationship in Equation 8–1 is shown in Figure 8–1. In part (a), the internal resistance, r'_{gs}, appears between the gate and source, and a current source equal to $g_m V_{gs}$ appears between the drain and source. Also, the internal drain-to-source resistance, r'_{ds}, is included. In part (b), a simplified ideal model is shown. The resistance, r'_{gs}, is assumed to be infinitely large so that there is an open circuit between the gate and source. Also, r'_{ds} is assumed large enough to neglect.

▶ FIGURE 8–1

Internal FET equivalent circuits.



(a) Complete (b) Simplified

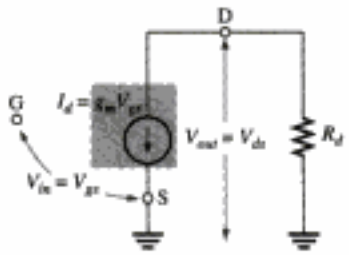
Voltage Gain

An ideal FET equivalent circuit with an external ac drain resistance is shown in Figure 8–2. The ac voltage gain of this circuit is V_{out}/V_{in}, where $V_{in} = V_{gs}$ and $V_{out} = V_{ds}$. The voltage gain expression is, therefore,

$$A_v = \frac{V_{ds}}{V_{gs}}$$

▶ FIGURE 8–2

Simplified FET equivalent circuit with an external ac drain resistance.

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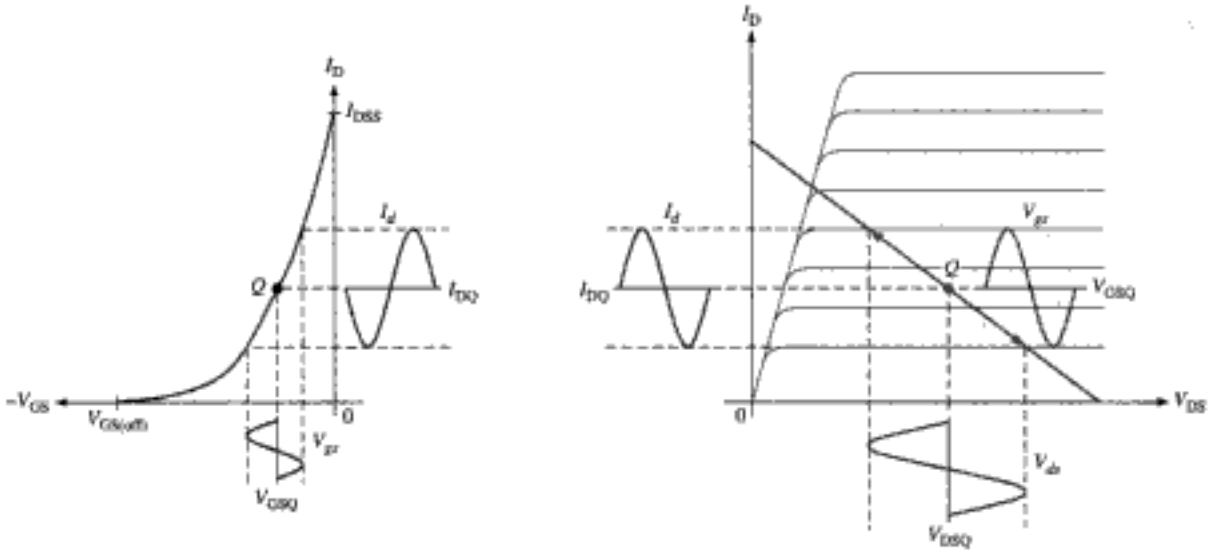


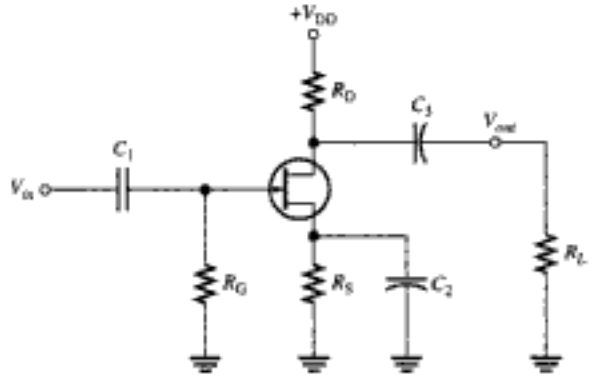
(a) JFET (*n*-channel) transfer characteristic curve showing signal operation

(b) JFET (*n*-channel) drain curves showing signal operation

▲ FIGURE 8–6

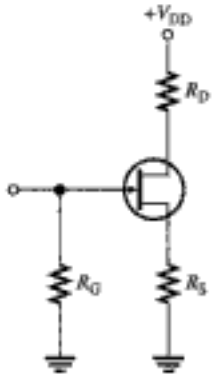
JFET characteristic curves.

substitution of $V_{GS} = I_D R_S$ into Equation 7–1.) A solution of the equation for I_D involves expanding it into a quadratic form and then finding the root of the quadratic, as developed in Appendix B.



▲ FIGURE 8–7

JFET common-source amplifier.



▲ FIGURE 8–8

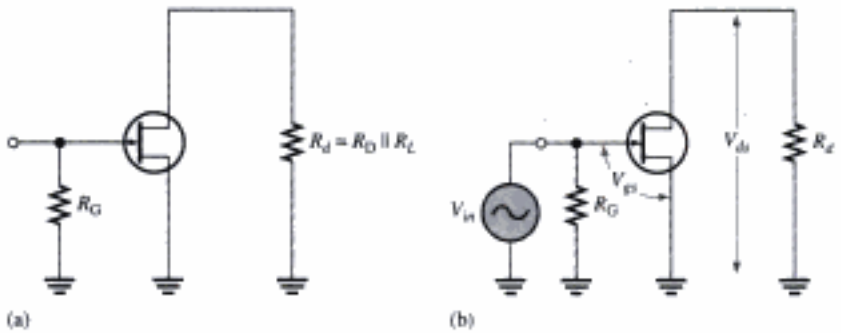
DC equivalent circuit for the amplifier in Figure 8–7.

Equation 8–5

$$I_D = I_{DSS}\left(1 - \frac{I_D R_S}{V_{GS(off)}}\right)^2$$

AC Equivalent Circuit

To analyze the signal operation of the amplifier in Figure 8–7, develop an ac equivalent circuit as follows. Replace the capacitors by effective shorts, based on the simplifying assumption that $X_C \equiv 0$ at the signal frequency. Replace the dc source by a ground, based on the assumption that the voltage source has a zero internal resistance. The V_{DD} terminal is at a zero-volt ac potential and therefore acts as an ac ground.



◄ FIGURE 8–9

AC equivalent for the amplifier in Figure 8–7.

The ac equivalent circuit is shown in Figure 8–9(a). Notice that the $+V_{DD}$ end of R_d and the source terminal are both effectively at ac ground. Recall that in ac analysis, the ac ground and the actual circuit ground are treated as the same point.

Signal Voltage at the Gate An ac voltage source is shown connected to the input in Figure 8–9(b). Since the input resistance to a FET is extremely high, practically all of the input voltage from the signal source appears at the gate with very little voltage dropped across the internal source resistance.

$$V_{gs} = V_{in}$$

Voltage Gain The expression for FET voltage gain that was given in Equation 8–2 applies to the common-source amplifier.

$$A_v = g_m R_d$$

Equation 8–6

The output signal voltage V_{ds} at the drain is

$$V_{out} = V_{ds} = A_v V_{gs}$$

or

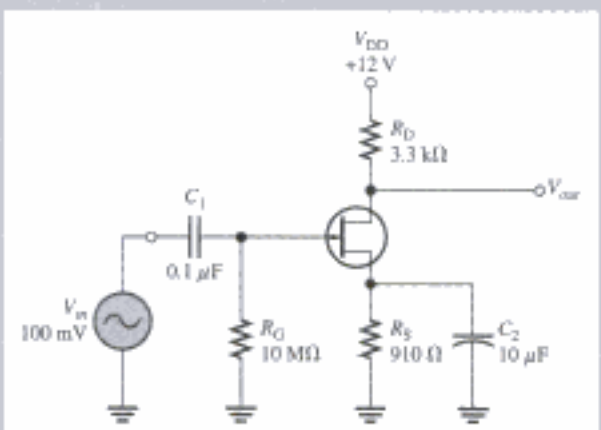
$$V_{out} = g_m R_d V_{in}$$

where $R_d = R_D \| R_L$ and $V_{in} = V_{gs}$.

EXAMPLE 8–4

What is the total output voltage of the unloaded amplifier in Figure 8–10? For this particular JFET, I_{DSS} is 12 mA and $V_{GS(off)}$ is −3 V.

► FIGURE 8–10

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Calculation of V_{out} yields

$$V_{out} = A_v V_{in} = g_m R_d V_{in} = (3.25\ \text{mS})(1.94\ \text{k}\Omega)(100\ \text{mV}) = \mathbf{631\ mV\ rms}$$

The unloaded ac output voltage was 1.07 V rms in Example 8–4.

Phase Inversion

The output voltage (at the drain) is 180° out of phase with the input voltage (at the gate). The phase inversion can be designated by a negative voltage gain, $-A_v$. Recall that the common-emitter BJT amplifier also exhibited a phase inversion.

Input Resistance

Because the input to a common-source amplifier is at the gate, the input resistance is extremely high. Ideally, it approaches infinity and can be neglected. As you know, the high input resistance is produced by the reverse-biased *pn* junction in a JFET and by the insulated gate structure in a MOSFET. The actual input resistance seen by the signal source is the gate-to-ground resistor, R_G, in parallel with the FET's input resistance, V_{GS}/I_{GSS}. The reverse leakage current, I_{GSS}, is typically given on the data sheet for a specific value of V_{GS} so that the input resistance of the device can be calculated.

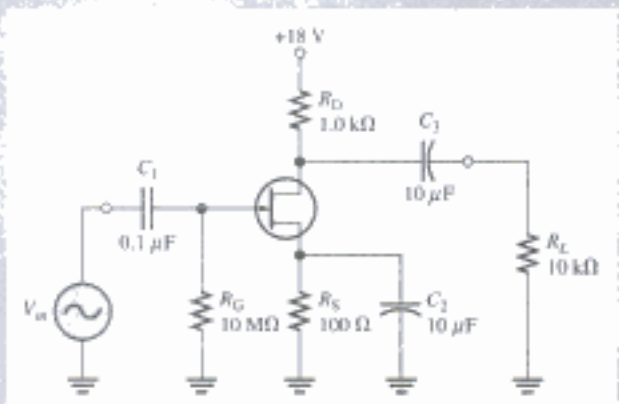
$$R_{in} = R_G \| \left(\frac{V_{GS}}{I_{GSS}} \right)$$

Equation 8–7

EXAMPLE 8–6

What input resistance is seen by the signal source in Figure 8–12? $I_{GSS} = 30$ nA at $V_{GS} = 10$ V.

▶ FIGURE 8–12



Solution The input resistance at the gate of the JFET is

$$R_{IN(gate)} = \frac{V_{GS}}{I_{GSS}} = \frac{10\ \text{V}}{30\ \text{nA}} = 333\ \text{M}\Omega$$

The input resistance seen by the signal source is

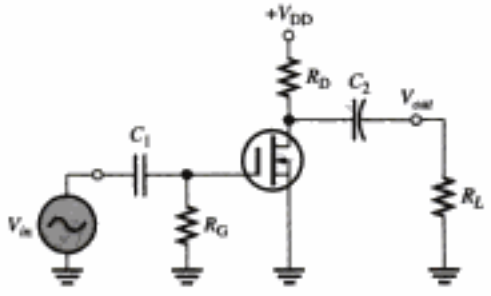
$$R_{in} = R_G \| R_{IN(gate)} = 10\ \text{M}\Omega \| 333\ \text{M}\Omega = \mathbf{9.7\ M\Omega}$$

D-MOSFET Amplifier Operation

A zero-biased common-source *n*-channel D-MOSFET with an ac source capacitively coupled to the gate is shown in Figure 8–13. The gate is at approximately 0 V dc and the source terminal is at ground, thus making $V_{GS} = 0$ V.

▶ **FIGURE 8–13**

Zero-biased D-MOSFET common-source amplifier.



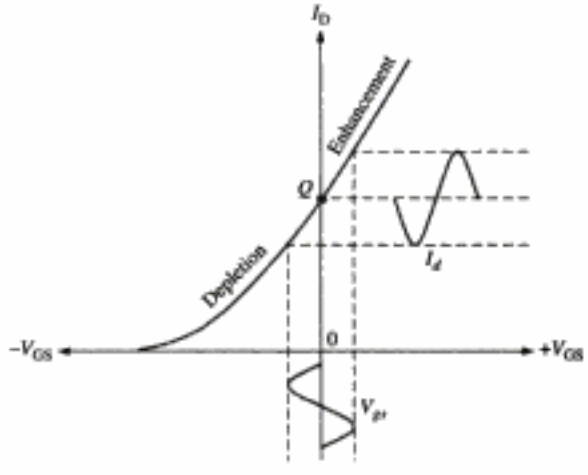
The signal voltage causes V_{gs} to swing above and below its zero value, producing a swing in I_d, as shown in Figure 8–14. The negative swing in V_{gs} produces the depletion mode, and I_d decreases. The positive swing in V_{gs} produces the enhancement mode, and I_d increases. Note that the enhancement mode is to the right of the vertical axis ($V_{GS} = 0$), and the depletion mode is to the left. The dc analysis of this amplifier is somewhat easier than for a JFET because $I_D = I_{DSS}$ at $V_{GS} = 0$. Once I_D is known, the analysis involves calculating only V_D.

$$V_D = V_{DD} - I_D R_D$$

The ac analysis is the same as for the JFET amplifier.

▶ **FIGURE 8–14**

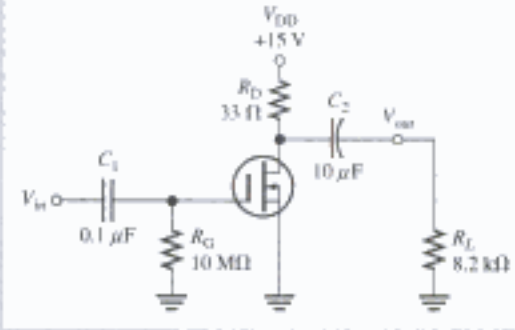
Depletion–enhancement operation of D-MOSFET shown on transfer characteristic curve.



EXAMPLE 8–7

The particular D-MOSFET used in the amplifier of Figure 8–15 has an I_{DSS} of 200 mA and a g_m of 200 mS. Determine both the dc drain voltage and ac output voltage. $V_{in} = 500$ mV.

► FIGURE 8–15



Solution Since the amplifier is zero-biased,

$$I_D = I_{DSS} = 200 \text{ mA}$$

and, therefore,

$$V_D = V_{DD} - I_D R_D = 15 \text{ V} - (200 \text{ mA})(33 \Omega) = \mathbf{8.4 \text{ V}}$$

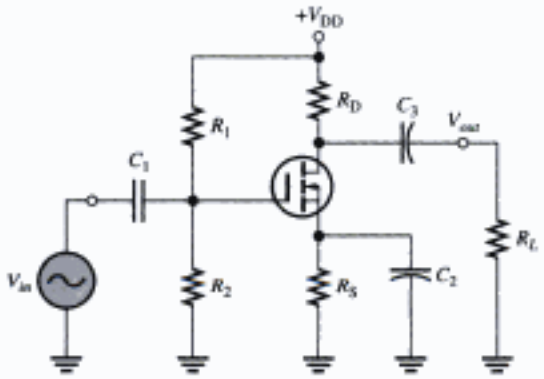
$$R_d = R_D \| R_L = 33 \Omega \| 8.2 \text{ k}\Omega = 32.9 \Omega$$

The ac output voltage is

$$V_{out} = g_m R_d V_{in} = (200 \text{ mS})(32.9 \Omega)(500 \text{ mV}) = \mathbf{3.29 \text{ V}}$$

E-MOSFET Amplifier Operation

A common-source *n*-channel E-MOSFET with voltage-divider bias with an ac source capacitively coupled to the gate is shown in Figure 8–16. The gate is biased with a positive voltage such that $V_{GS} > V_{GS(th)}$.



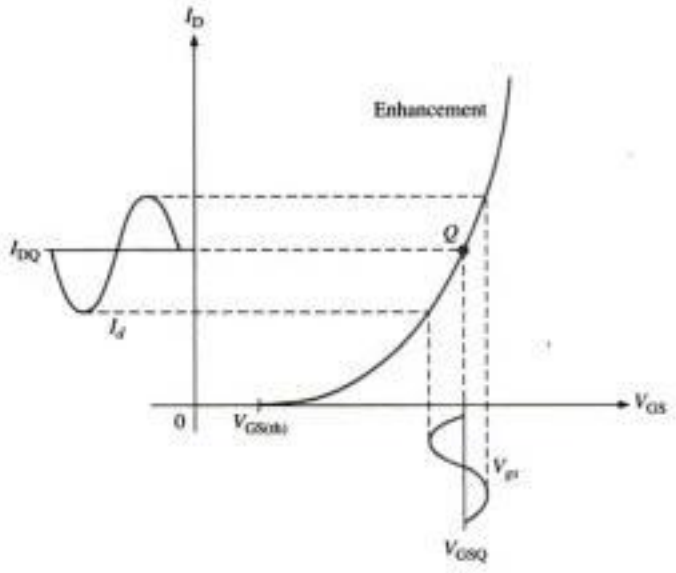
◄ FIGURE 8–16

Common-source E-MOSFET amplifier with voltage-divider bias.

As with the JFET and D-MOSFET, the signal voltage produces a swing in V_{gs} above and below its Q-point value, V_{GSQ}. This, in turn, causes a swing in I_d above and below its Q-point value, I_{DQ}, as illustrated in Figure 8–17. Operation is entirely in the enhancement mode.

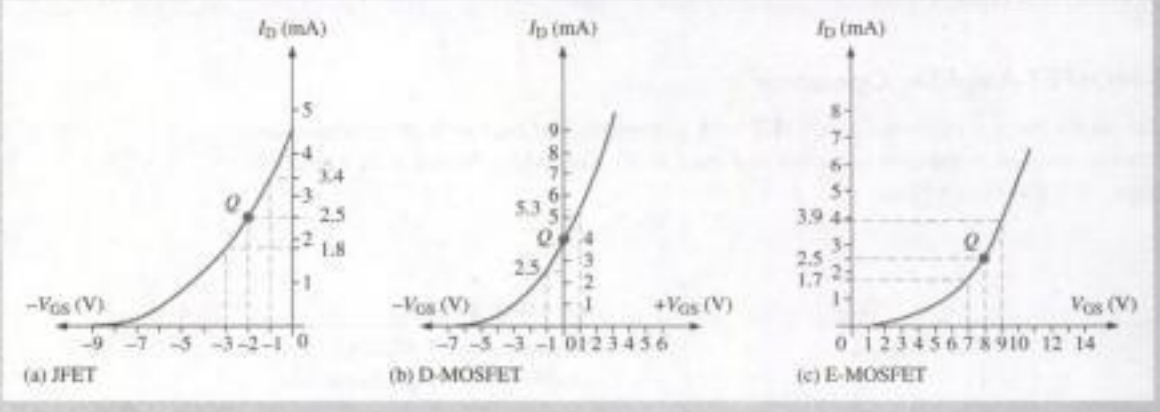
▶ FIGURE 8–17

E-MOSFET (*n*-channel) operation shown on transfer characteristic curve.



EXAMPLE 8–8

Transfer characteristic curves for a particular *n*-channel JFET, D-MOSFET, and E-MOSFET are shown in Figure 8–18. Determine the peak-to-peak variation in I_d when V_{gs} is varied ±1 V about its Q-point value for each curve.



▲ FIGURE 8–18

Solution

(a) The JFET Q-point is at $V_{GS} = -2$ V and $I_D = 2.5$ mA. From the graph in Figure 8–18(a), $I_D = 3.4$ mA when $V_{GS} = -1$ V, and $I_D = 1.8$ mA when $V_{GS} = -3$ V. The peak-to-peak drain current is therefore **1.6 mA.**

(b) The D-MOSFET Q-point is at $V_{GS} = 0$ V and $I_D = I_{DSS} = 4$ mA. From the graph in Figure 8–18(b), $I_D = 2.5$ mA when $V_{GS} = -1$ V, and $I_D = 5.3$ mA when $V_{GS} = +1$ V. The peak-to-peak drain current is therefore **2.8 mA.**

(c) The E-MOSFET Q-point is at $V_{GS} = +8$ V and $I_D = 2.5$ mA. From the graph in Figure 8–18(c), $I_D = 3.9$ mA when $V_{GS} = +9$ V, and $I_D = 1.7$ mA when $V_{GS} = +7$ V. The peak-to-peak drain current is therefore **2.2 mA.**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SECTION 8–2 REVIEW

1. When V_{gs} is at its positive peak, at what points are I_d and V_{ds}?
2. What is the difference between V_{gs} and V_{GS}?
3. Which of the three types of FETs can operate with a gate-to-source Q-point value of 0 V?
4. What factors determine the voltage gain of a common-source FET amplifier?
5. A certain amplifier has an $R_D = 1.0\ \text{k}\Omega$. When a load resistance of 1.0 kΩ is capacitively coupled to the drain, how much does the gain change?

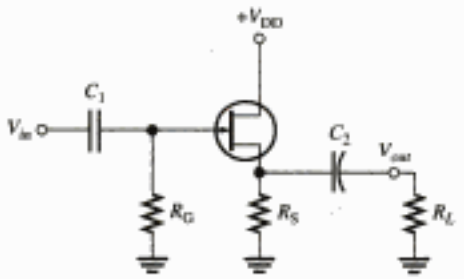
8–3 COMMON-DRAIN AMPLIFIERS

The common-drain (CD) amplifier covered in this section is comparable to the common-collector BJT amplifier. Recall that the CC amplifier is called an emitter-follower. Similarly, the common-drain amplifier is called a source-follower because the voltage at the source is approximately the same amplitude as the input (gate) voltage and is in phase with it. In other words, the source voltage follows the gate input voltage.

A **common-drain** JFET amplifier is one that has no drain resistor, as shown in Figure 8–20. A common-drain amplifier is also called a **source-follower.** Self-biasing is used in this particular circuit. The input signal is applied to the gate through a coupling capacitor, C_1, and the output signal is coupled to the load resistor through C_2.

▶ **FIGURE 8–20**

JFET common-drain amplifier (source-follower).



Voltage Gain

As in all amplifiers, the voltage gain is $A_v = V_{out}/V_{in}$. For the source-follower, V_{out} is I_dR_s and V_{in} is $V_{gs} + I_dR_s$, as shown in Figure 8–21. Therefore, the gate-to-source voltage gain is $I_dR_s/(V_{gs} + I_dR_s)$. Substituting $I_d = g_mV_{gs}$ into the expression gives the following result:

$$A_v = \frac{g_mV_{gs}R_s}{V_{gs} + g_mV_{gs}R_s}$$

The V_{gs} terms cancel, so

Equation 8–9

$$A_v = \frac{g_mR_s}{1 + g_mR_s}$$

Notice here that the gain is always slightly less than one. If $g_mR_s >> 1$, then a good approximation is $A_v \cong 1$. Since the output voltage is at the source, it is in phase with the gate (input) voltage.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Most of the power from the dc source is supplied to the output stage. The current in the output stage can be computed from the emitter voltage of Q_3 which is approximately 9.5 V, taking the loading into account. This results in a Q_3 emitter current of approximately 0.6 A. Neglecting the other transistor and bias currents, which are very small, the total dc supply current is about 0.6 A. The power from the dc source is

$$P_{DC} = I_{CC}V_{CC} = (0.6\text{ A})(15\text{ V}) = 9\text{ W}$$

Therefore, the efficiency of the amplifier for this input is

$$eff = \frac{P_{out}}{P_{DC}} = \frac{0.454\text{ W}}{9\text{ W}} \cong \mathbf{0.05}$$

This represents an efficiency of 5%.

SECTION 9–1 REVIEW

Answers are at the end of the chapter.

1. What is the purpose of a heat sink?
2. Which lead of a BJT is connected to the case?
3. What are the two types of clipping with a class A power amplifier?
4. What is the maximum theoretical efficiency for a class A amplifier?
5. How can the power gain of a CC amplifier be expressed in terms of a ratio of resistances?

9–2 CLASS B AND CLASS AB PUSH-PULL AMPLIFIERS

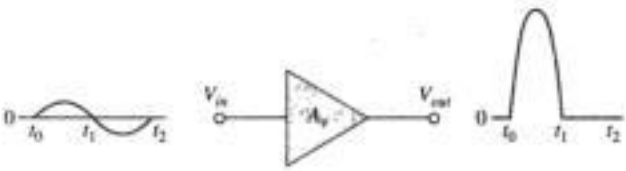
When an amplifier is biased at cutoff so that it operates in the linear region for 180° of the input cycle and is in cutoff for 180°, it is a **class B** amplifier. Class AB amplifiers are biased to conduct for slightly more than 180°. The primary advantage of a class B or class AB amplifier over a class A amplifier is that either one is more efficient than a class A amplifier; you can get more output power for a given amount of input power. A disadvantage of class B or class AB is that it is more difficult to implement the circuit in order to get a linear reproduction of the input waveform. As you will see in this section, the term *push-pull* refers to a common type of class B or class AB amplifier circuit in which the input wave shape is reproduced at the output.

Class B Operation

The class B operation is illustrated in Figure 9–6, where the output waveform is shown relative to the input in terms of time (t).

► **FIGURE 9–6**

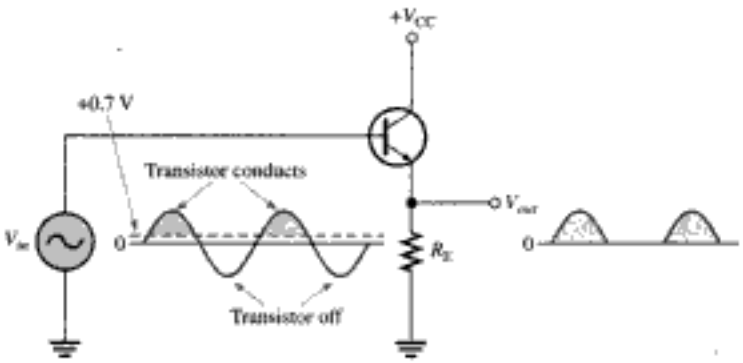
Basic class B amplifier operation (noninverting).



The Q-Point Is at Cutoff The class B amplifier is biased at the cutoff point so that $I_{CQ} = 0$ and $V_{CEQ} = V_{CE(cutoff)}$. It is brought out of cutoff and operates in its linear region when the input signal drives the transistor into conduction. This is illustrated in Figure 9–7 with an emitter-follower circuit where, as you can see, the output is not a replica of the input.

Class B Push-Pull Operation

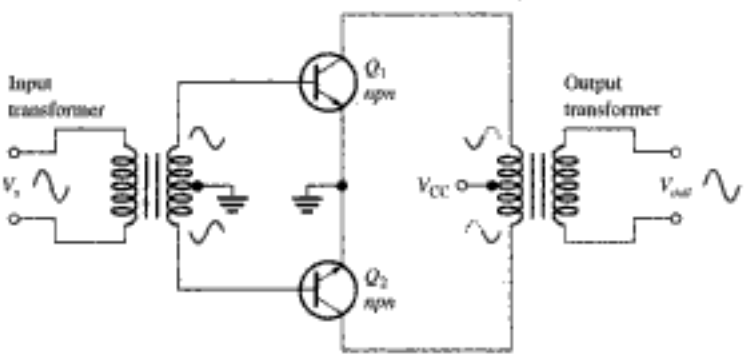
As you can see, the circuit in Figure 9–7 only conducts for the positive half of the cycle. To amplify the entire cycle, it is necessary to add a second class B amplifier that operates on the negative half of the cycle. The combination of two class B amplifiers working together is called **push-pull** operation.



◀ **FIGURE 9–7**
Common-collector class B amplifier.

There are two common approaches for using push-pull amplifiers to reproduce the entire waveform. The first approach uses transformer coupling. The second uses two **complementary symmetry transistors**; these are a matching pair of *npn*/*pnp* BJTs or a matching pair of *n*-channel/*p*-channel FETs.

Transformer Coupling Transformer coupling is illustrated in Figure 9–8. The input transformer has a center-tapped secondary that is connected to ground, producing phase inversion of one side with respect to the other. The input transformer thus converts the input signal to two out-of-phase signals for the transistors. Notice that both transistors are *npn* types. Because of the signal inversion, Q_1 will conduct on the positive part of the cycle and Q_2 will conduct on the negative part. The output transformer combines the signals by permitting current in both directions, even though one transistor is always cut off. The positive power supply signal is connected to the center tap of the output transformer.



◀ **FIGURE 9–8**
Transformer coupled push-pull amplifiers. Q_1 conducts during the positive half-cycle; Q_2 conducts during the negative half-cycle. The two halves are combined by the output transformer.

Complementary Symmetry Transistors Figure 9–9 shows one of the most popular types of push-pull class B amplifiers using two emitter-followers and both positive and negative power supplies. This is a complementary amplifier because one emitter-follower uses an *npn* transistor and the other a *pnp*, which conduct on opposite alternations of the input cycle. Notice that there is no dc base bias voltage ($V_B = 0$). Thus, only the signal voltage drives the transistors into conduction. Transistor Q_1 conducts during the positive half of the input cycle, and Q_2 conducts during the negative half.

Crossover Distortion When the dc base voltage is zero, both transistors are off and the input signal voltage must exceed V_{BE} before a transistor conducts. Because of this, there is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The ac cutoff voltage for a two-supply operation is at V_{CC} with an I_{CQ} as given earlier. The ac saturation current for a two-supply operation with a push-pull amplifier is

Equation 9–5

$$I_{c(sat)} = \frac{V_{CC}}{R_L}$$

The ac load line for the *npn* transistor is as shown in Figure 9–13. The dc load line can be found by drawing a line that passes through V_{CEQ} and the dc saturation current, $I_{C(sat)}$. However, the saturation current for dc is the current if the collector to emitter is shorted on both transistors! This assumed short across the power supplies obviously would cause maximum current from the supplies and implies the dc load line passes almost vertically through the cutoff as shown. Operation along the dc load line, such as caused by thermal runaway, could produce such a high current that the transistors are destroyed.

▶ FIGURE 9–13

Load lines for a complementary symmetry push-pull amplifier. Only the load lines for the *npn* transistor are shown.

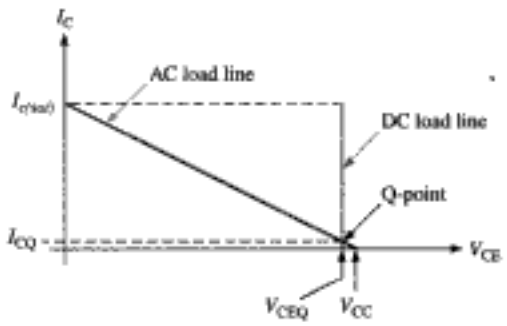
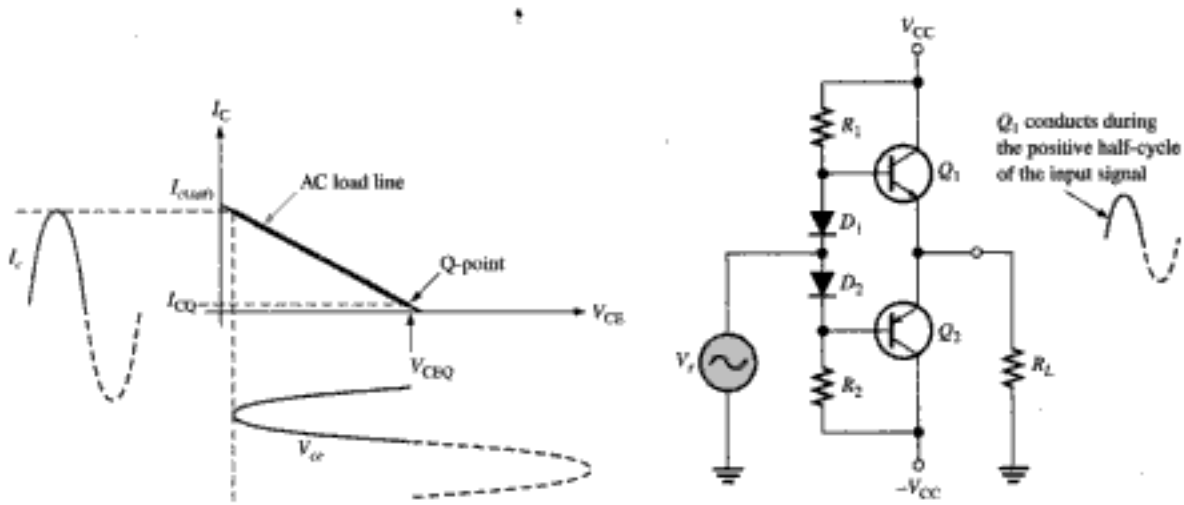


Figure 9–14(a) illustrates the ac load line for Q_1 of the class AB amplifier in Figure 9–14(b). In the case illustrated, a signal is applied that swings over the region of the ac load line shown in bold. At the upper end of the ac load line, the voltage across the transistor (V_{ce}) is a minimum, and the output voltage is maximum.



(a) AC load line for Q_1

(b) Circuit

▲ FIGURE 9–14

Under maximum conditions, transistors Q_1 and Q_2 are alternately driven from near cutoff to near saturation. During the positive alternation of the input signal, the Q_1 emitter is driven from its Q-point value of 0 to nearly V_{CC}, producing a positive peak voltage a little less than V_{CC}. Likewise, during the negative alternation of the input signal, the Q_2 emitter

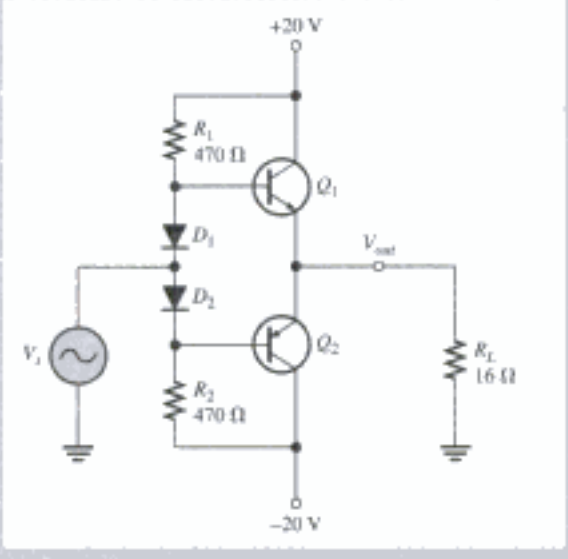
is driven from its Q-point value of 0 V, to near $-V_{CC}$, producing a negative peak voltage almost equal to $-V_{CC}$. Although it is possible to operate close to the saturation current, this type of operation results in increased distortion of the signal.

The ac saturation current (Equation 9–5) is also the peak output current. Each transistor can essentially operate over its entire load line. Recall that in class A operation, the transistor can also operate over the entire load line but with a significant difference. In class A operation, the Q-point is near the middle and there is significant current in the transistors even with no signal. In class B operation, when there is no signal, the transistors have only a very small current and therefore dissipate very little power. Thus, the efficiency of a class B amplifier can be much higher than a class A amplifier. It will be shown later that the maximum theoretical efficiency of a class B amplifier is 79%.

EXAMPLE 9–3

Determine the ideal maximum peak output voltage and current for the circuit shown in Figure 9–15.

▶ **FIGURE 9–15**



Solution The ideal maximum peak output voltage is

$$V_{out(peak)} \cong V_{CEQ} \cong V_{CC} = \mathbf{20\ V}$$

The ideal maximum peak current is

$$I_{out(peak)} \cong I_{C(sat)} \cong \frac{V_{CC}}{R_L} = \frac{20\ \text{V}}{16\ \Omega} = \mathbf{1.25\ A}$$

The actual maximum values of voltage and current are slightly smaller.

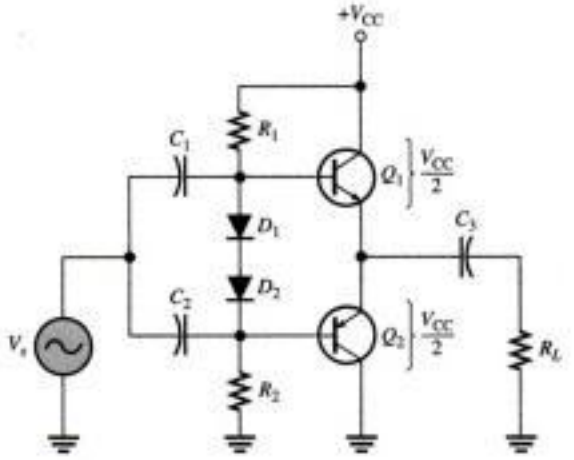
Single-Supply Push-Pull Amplifier

Push-pull amplifiers using complementary symmetry transistors can be operated from a single voltage source as shown in Figure 9–16. The circuit operation is the same as that described previously, except the bias is set to force the output emitter voltage to be $V_{CC}/2$ instead of zero volts used with two supplies. Because the output is not biased at zero volts,

capacitive coupling for the input and output is necessary to block the bias voltage from the source and the load resistor. Ideally, the output voltage can swing from zero to V_{CC}, but in practice it does not quite reach these ideal values.

► **FIGURE 9–16**

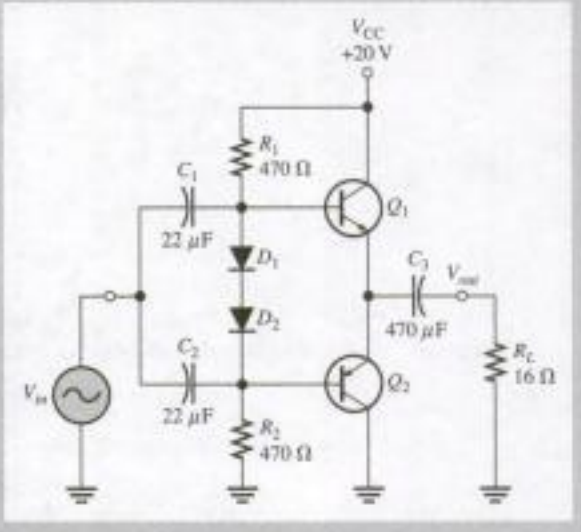
Single-ended push-pull amplifier.



EXAMPLE 9–4

Determine the maximum ideal peak values for the output voltage and current in Figure 9–17.

► **FIGURE 9–17**



Solution The maximum peak output voltage is

$$V_{out(peak)} \cong V_{CEQ} = \frac{V_{CC}}{2} = \frac{20\text{ V}}{2} = \mathbf{10\text{ V}}$$

The maximum peak output current is

$$I_{out(peak)} \cong I_{c(sat)} = \frac{V_{CEQ}}{R_L} = \frac{10\text{ V}}{16\ \Omega} = \mathbf{625\text{ mA}}$$

Class B/AB Power

Maximum Output Power You have seen that the maximum peak output current for both dual-supply and single-supply push-pull amplifiers is approximately $I_{c(sat)}$, and the maximum peak output voltage is approximately V_{CEQ}. The maximum *average* output power is, therefore,

$$P_{out} = I_{out(rms)}V_{out(rms)}$$

Since

$$I_{out(rms)} = 0.707I_{out(peak)} = 0.707I_{c(sat)}$$

and

$$V_{out(rms)} = 0.707V_{out(peak)} = 0.707V_{CEQ}$$

then

$$P_{out} = 0.5I_{c(sat)}V_{CEQ}$$

Substituting $V_{CC}/2$ for V_{CEQ}, the maximum average output power is

$$P_{out} = 0.25I_{c(sat)}V_{CC} \qquad \textbf{Equation 9–6}$$

DC Input Power The dc input power comes from the V_{CC} supply and is

$$P_{DC} = I_{CC}V_{CC}$$

Since each transistor draws current for a half-cycle, the current is a half-wave signal with an average value of

$$I_{CC} = \frac{I_{c(sat)}}{\pi}$$

So,

$$P_{DC} = \frac{I_{c(sat)}V_{CC}}{\pi}$$

Efficiency An advantage of push-pull class B and class AB amplifiers over class A is a much higher efficiency. This advantage usually overrides the difficulty of biasing the class AB push-pull amplifier to eliminate crossover distortion. Recall that efficiency is defined as the ratio of ac output power to dc input power.

$$\text{Efficiency} = \frac{P_{out}}{P_{DC}}$$

The maximum efficiency for a class B amplifier (class AB is slightly less) is designated η_{max} and is developed as follows, starting with Equation 9–6.

$$P_{out} = 0.25I_{c(sat)}V_{CC}$$

$$\eta_{max} = \frac{P_{out}}{P_{DC}} = \frac{0.25I_{c(sat)}V_{CC}}{I_{c(sat)}V_{CC}/\pi} = 0.25\pi$$

$$\eta_{max} = 0.79 \qquad \textbf{Equation 9–7}$$

or, as a percentage,

$$\eta_{max} = 79\%$$

Recall that the maximum efficiency for class A is 0.25 (25 percent).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R_c is the equivalent parallel resistance of the collector tank circuit and represents the parallel combination of the coil resistance and the load resistance. It usually has a low value. The total power that must be supplied to the amplifier is

$$P_T = P_{out} + P_{D(avg)}$$

Therefore, the efficiency is

Equation 9–10

$$\eta = \frac{P_{out}}{P_{out} + P_{D(avg)}}$$

When $P_{out} >> P_{D(avg)}$, the class C efficiency closely approaches 1 (100 percent).

EXAMPLE 9–8

Suppose the class C amplifier described in Example 9–7 has a V_{CC} equal to 24 V and the R_c is 100 Ω. Determine the efficiency.

Solution From Example 9–7, $P_{D(avg)} = 4$ mW.

$$P_{out} = \frac{0.5V_{CC}^2}{R_c} = \frac{0.5(24\text{ V})^2}{100\ \Omega} = 2.88\text{ W}$$

Therefore,

$$\eta = \frac{P_{out}}{P_{out} + P_{D(avg)}} = \frac{2.88\text{ W}}{2.88\text{ W} + 4\text{ mW}} = \mathbf{0.999}$$

or

$$\eta \times 100\% = 99.9\%$$

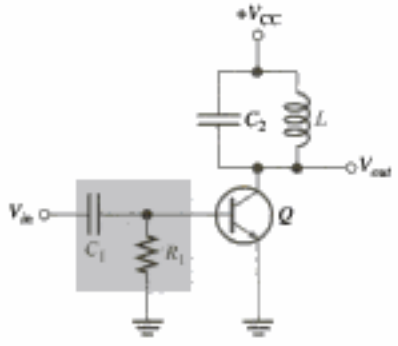
Clamper Bias for a Class C Amplifier

Figure 9–27 shows a class C amplifier with a base bias clamping circuit. The base-emitter junction functions as a diode.

When the input signal goes positive, capacitor C_1 is charged to the peak value with the polarity shown in Figure 9–28(a) on the next page. This action produces an average voltage at the base of approximately $-V_p$. This places the transistor in cutoff except at the positive peaks, when the transistor conducts for a short interval. For good clamping action, the R_1C_1 time constant of the clamping circuit must be much greater than the period of the input signal. Parts (b) through (f) of Figure 9–28 illustrate the bias clamping action in more detail. During the time up to the positive peak of the input (t_0 to t_1), the capacitor charges to $V_p - 0.7$ V through the base-emitter diode, as shown in part (b).

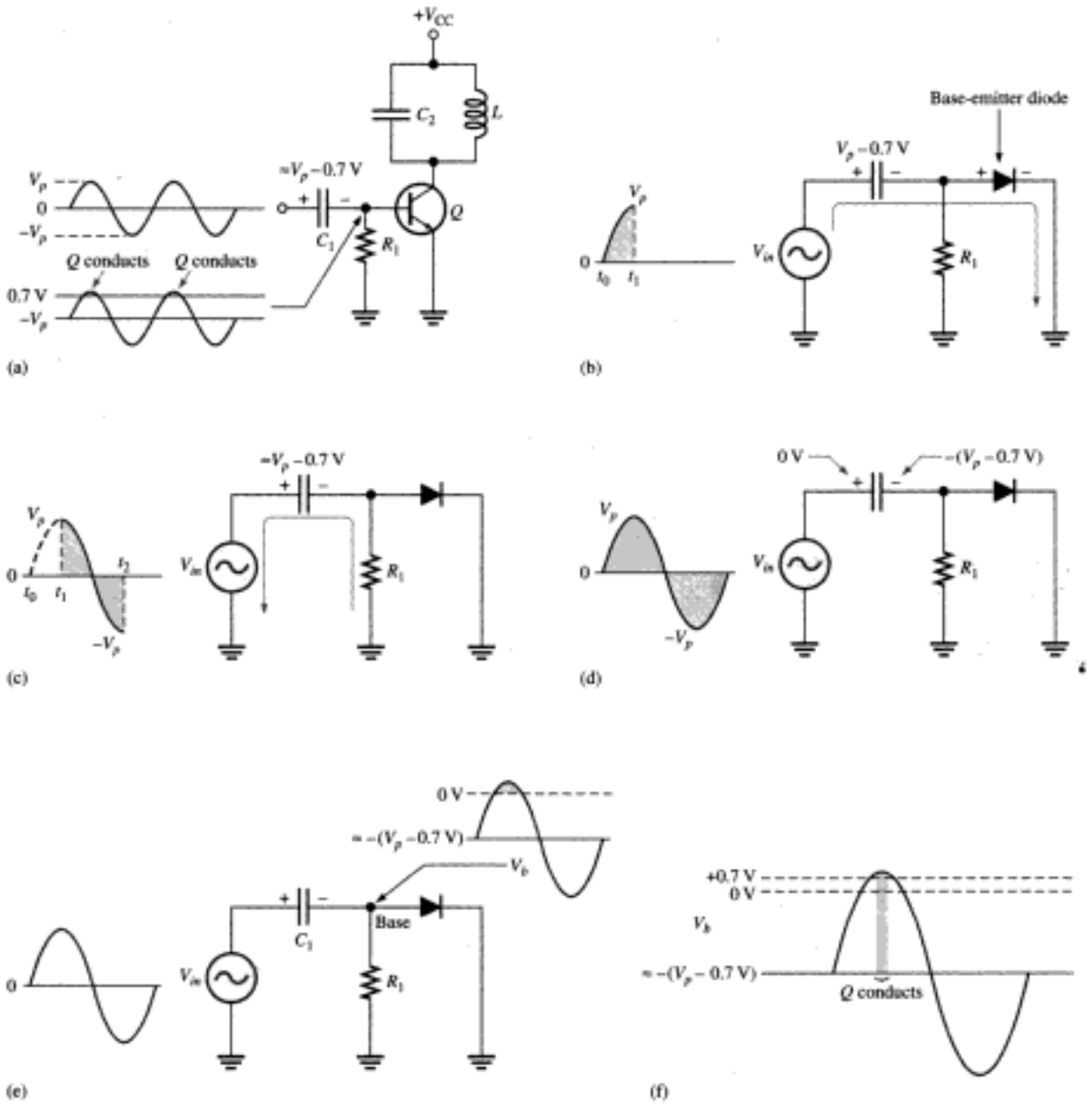
▶ **FIGURE 9–27**

Tuned class C amplifier with clamper bias.



During the time from t_1 to t_2, as shown in part (c), the capacitor discharges very little because of the large RC time constant. The capacitor, therefore, maintains an average charge slightly less than $V_p - 0.7$ V.

Since the dc value of the input signal is zero (positive side of C_1), the dc voltage at the base (negative side of C_1) is slightly more positive than $-(V_p - 0.7\text{ V})$, as indicated in Figure 9–28(d). As shown in Figure 9–28(e), the capacitor couples the ac input signal through to the base so that the voltage at the transistor's base is the ac signal riding on a dc level slightly more positive than $-(V_p - 0.7\text{ V})$. Near the positive peaks of the input voltage, the base voltage goes slightly above 0.7 V and causes the transistor to conduct for a short time, as shown in Figure 9–28(f).



▲ FIGURE 9–28

Clamper bias action.

SECTION 9–3 REVIEW

1. At what point is a class C amplifier normally biased?
2. What is the purpose of the tuned circuit in a class C amplifier?
3. A certain class C amplifier has a power dissipation of 100 mW and an output power of 1 W. What is its percent efficiency?

CHAPTER SUMMARY

- A class A power amplifier operates entirely in the linear region of the transistor's characteristic curves. The transistor conducts during the full 360° of the input cycle.
- The Q-point must be centered on the load line for maximum class A output signal swing.
- The maximum efficiency of a class A power amplifier is 25 percent.
- A class B amplifier operates in the linear region for half of the input cycle (180°), and it is in cutoff for the other half.
- The Q-point is at cutoff for class B operation.
- Class B amplifiers are normally operated in a push-pull configuration in order to produce an output that is a replica of the input.
- The maximum efficiency of a class B amplifier is 79 percent.
- A class AB amplifier is biased slightly above cutoff and operates in the linear region for slightly more than 180° of the input cycle.
- Class AB eliminates crossover distortion found in pure class B.
- A class C amplifier operates in the linear region for only a small part of the input cycle.
- The class C amplifier is biased below cutoff.
- Class C amplifiers are normally operated as tuned amplifiers to produce a sinusoidal output.
- The maximum efficiency of a class C amplifier is higher than that of either class A or class B amplifiers. Under conditions of low power dissipation and high output power, the efficiency can approach 100 percent.

OBJECTIVE TYPE QUESTIONS

Answers are at the end of the chapter.

1. If the value of R_1 in Figure 9–5 is decreased, the voltage gain of the first stage will
(a) increase **(b)** decrease **(c)** not change

2. If the value of R_{E2} in Figure 9–5 is increased, the voltage gain of the first stage will
(a) increase **(b)** decrease **(c)** not change

3. If C_2 in Figure 9–5 opens, the dc voltage at the emitter of Q_1 will
(a) increase **(b)** decrease **(c)** not change

4. If the value of R_4 in Figure 9–5 is increased, the dc voltage at the base of Q_2 will
(a) increase **(b)** decrease **(c)** not change

5. If V_{CC} in Figure 9–18 is increased, the peak output voltage will
(a) increase **(b)** decrease **(c)** not change

6. If the value of R_L in Figure 9–18 is increased, the ac output power will
(a) increase **(b)** decrease **(c)** not change

7. If the value of R_7 in Figure 9–20 is decreased, the voltage gain will
(a) increase **(b)** decrease **(c)** not change

8. If the value of R_5 in Figure 9–20 is increased, the output power will
(a) increase **(b)** decrease **(c)** not change

9. If the values of R_8 and R_9 in Figure 9–20 are increased, the voltage gain will
(a) increase **(b)** decrease **(c)** not change

10. If the value of C_2 in Figure 9–24 is decreased, the resonant frequency will
(a) increase **(b)** decrease **(c)** not change

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3. Cutoff and saturation clipping
4. 25%
5. The ratio of input resistance to output resistance

SECTION 9–2 Class B and Class AB Push-Pull Amplifiers

1. The class B Q-point is at cutoff.
2. The barrier potential of the base-emitter junction causes crossover distortion.
3. Maximum efficiency of a class B amplifier is 79%.
4. Push-pull reproduces both positive and negative alternations of the input signal with greater efficiency.
5. Both transistors in class AB are biased slightly above cutoff. In class B they are biased at cutoff.

SECTION 9–3 Class C Amplifiers

1. Class C is biased well into cutoff.
2. The purpose of the tuned circuit is to produce a sinusoidal voltage output.
3. $\eta = [1\text{ W}/(1\text{ W} + 0.1\text{ W})]100 = 90.9\%$

OBJECTIVE TYPE QUESTIONS

1. (c) **2.** (c) **3.** (c) **4.** (a) **5.** (a) **6.** (b) **7.** (b) **8.** (b) **9.** (c) **10.** (a)
11. (a) **12.** (b) **13.** (b) **14.** (a) **15.** (b) **16.** (c) **17.** (a) **18.** (e) **19.** (c) **20.** (c)
21. (a) **22.** (c) **23.** (b) **24.** (d) **25.** (a) **26.** (d) **27.** (c)

10

AMPLIFIER FREQUENCY RESPONSE

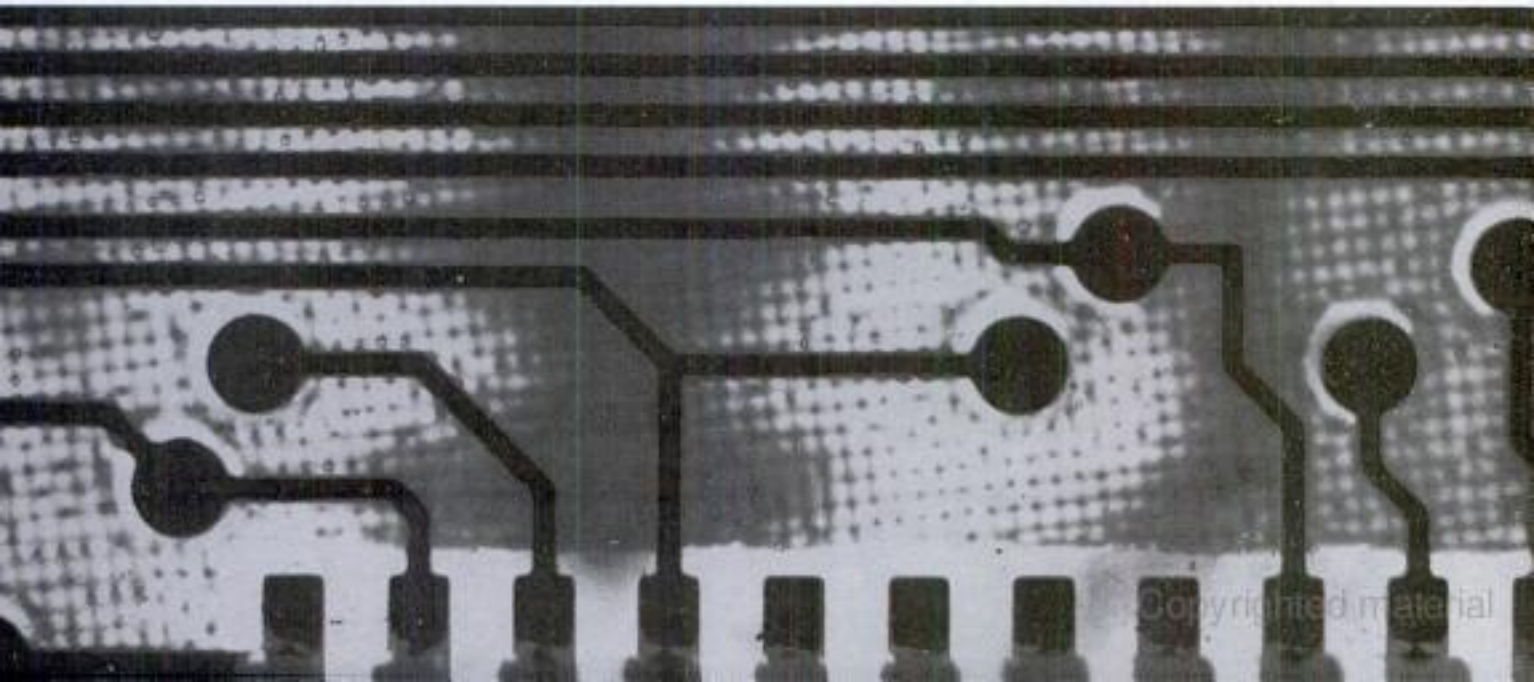
CHAPTER OUTLINE

INTRODUCTION

In the previous chapters on amplifiers, the effects of the input frequency on an amplifier's operation due to capacitive elements in the circuit were neglected in order to focus on other concepts. The coupling and bypass capacitors were considered to be ideal shorts and the internal transistor capacitances were considered to be ideal opens. This treatment is valid when the frequency is in an amplifier's midrange.

As you know, capacitive reactance decreases with increasing frequency and vice versa. When the frequency is low enough, the coupling and bypass capacitors can no longer be considered as shorts because their reactances are large enough to have a significant effect. Also, when the frequency is high enough, the internal transistor capacitances can no longer be considered as opens because their reactances become small enough to have a significant effect on the amplifier operation. A complete picture of an amplifier's response must take into account the full range of frequencies over which the amplifier can operate.

In this chapter, you will study the frequency effects on amplifier gain and phase shift. The coverage applies to both BJT and FET amplifiers, and a mix of both are included to illustrate the concepts.



10–1 BASIC CONCEPTS

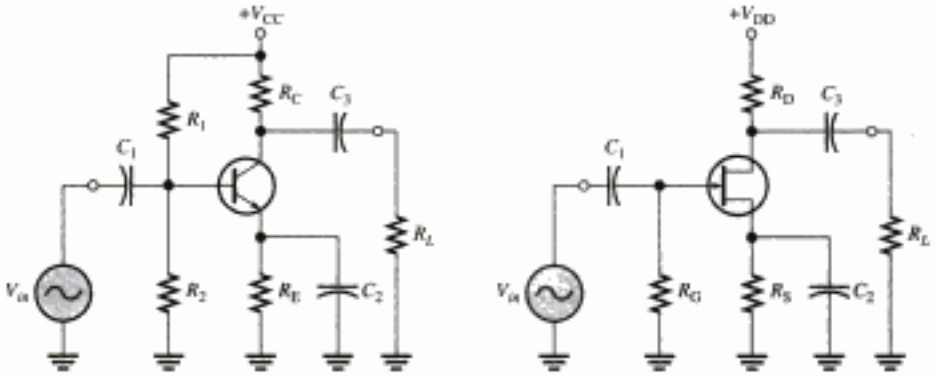
In the previous coverage of amplifiers, the capacitive reactance of the coupling and bypass capacitors was assumed to be 0 Ω at the signal frequency and, therefore, had no effect on an amplifier's gain or phase shift. Also, the internal transistor capacitances were assumed to be small enough to neglect at the operating frequency. All of these simplifying assumptions are valid and necessary for studying amplifier theory. However, these simplifying assumptions give a limited picture of an amplifier's total operation, so in this section you begin to study the frequency effects of these capacitances. The **frequency response** of an amplifier is the change in gain or phase shift over a specified range of input signal frequencies.

Effect of Coupling Capacitors

Recall from basic circuit theory that $X_C = 1/(2\pi fC)$. This formula shows that the capacitive reactance varies inversely with frequency. At lower frequencies the reactance is greater, and it decreases as the frequency increases. At lower frequencies—for example, audio frequencies below 10 Hz—capacitively coupled amplifiers such as those in Figure 10–1 have less voltage gain than they have at higher frequencies. The reason is that at lower frequencies more signal voltage is dropped across C_1 and C_3 because their reactances are higher. This higher signal voltage drop at lower frequencies reduces the voltage gain. Also, a phase shift is introduced by the coupling capacitors because C_1 forms a lead circuit with the R_{in} of the amplifier and C_3 forms a lead circuit with R_L in parallel with R_C or R_D. Recall that a *lead circuit* is an RC circuit in which the output voltage across R leads the input voltage in phase.

▶ FIGURE 10–1

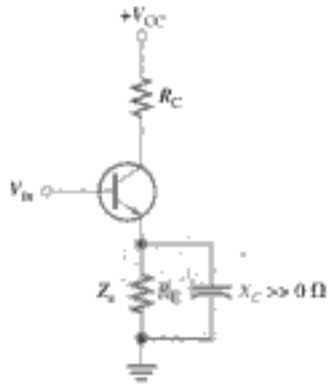
Examples of capacitively coupled BJT and FET amplifiers.



Effect of Bypass Capacitors

At lower frequencies, the reactance of the bypass capacitor, C_2 in Figure 10–1, becomes significant and the emitter (or FET source terminal) is no longer at ac ground. The capacitive reactance X_{C2} in parallel with R_E (or R_S) creates an impedance that reduces the gain. This is illustrated in Figure 10–2.

For example, when the frequency is sufficiently high, $X_C \approx 0\ \Omega$ and the voltage gain of the CE amplifier is $A_v = R_C/r'_e$. At lower frequencies, $X_C >> 0\ \Omega$ and the voltage gain is $A_v = R_C/(r'_e + Z_e)$.



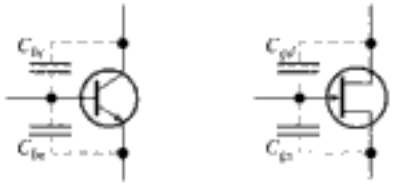
◀ FIGURE 10–2

Nonzero reactance of the bypass capacitor in parallel with R_E creates an emitter impedance, (Z_e), which reduces the voltage gain.

Effect of Internal Transistor Capacitances

At high frequencies, the coupling and bypass capacitors become effective ac shorts and do not affect an amplifier's response. Internal transistor junction capacitances, however, do come into play, reducing an amplifier's gain and introducing phase shift as the signal frequency increases.

Figure 10–3 shows the internal *pn* junction capacitances for both a bipolar junction transistor and a JFET. In the case of the BJT, C_{be} is the base-emitter junction capacitance and C_{bc} is the base-collector junction capacitance. In the case of the JFET, C_{gs} is the capacitance between gate and source and C_{gd} is the capacitance between gate and drain.



(a) BJT (b) JFET

◀ FIGURE 10–3

Internal transistor capacitances.

Data sheets often refer to the BJT capacitance C_{bc} as the output capacitance, often designated C_{ob}. The capacitance C_{be} is often designated as the input capacitance C_{ib}. Data sheets for FETs normally specify input capacitance C_{iss} and reverse transfer capacitance C_{rss}. From these, C_{gs} and C_{gd} can be calculated, as you will see in Section 10–4.

At lower frequencies, the internal capacitances have a very high reactance because of their low capacitance value (usually only a few picofarads) and the low frequency value. Therefore, they look like opens and have no effect on the transistor's performance. As the frequency goes up, the internal capacitive reactances go down, and at some point they begin to have a significant effect on the transistor's gain. When the reactance of C_{be} (or C_{gs}) becomes small enough, a significant amount of the signal voltage is lost due to a voltage-divider effect of the signal source resistance and the reactance of C_{be}, as illustrated in Figure 10–4(a). When the reactance of C_{bc} (or C_{gd}) becomes small enough, a significant amount of output signal voltage is fed back out of phase with the input (negative feedback), thus effectively reducing the voltage gain. This is illustrated in Figure 10–4(b).

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SECTION 10–2 REVIEW

1. How much increase in actual voltage gain corresponds to +12 dB?
2. Convert a power gain of 25 to decibels.
3. What power corresponds to 0 dBm?

10–3 LOW-FREQUENCY AMPLIFIER RESPONSE

In this section, we will examine how the voltage gain and phase shift of a capacitively coupled amplifier are affected by frequencies below which the reactance of the coupling capacitors becomes too large to neglect.

BJT Amplifiers

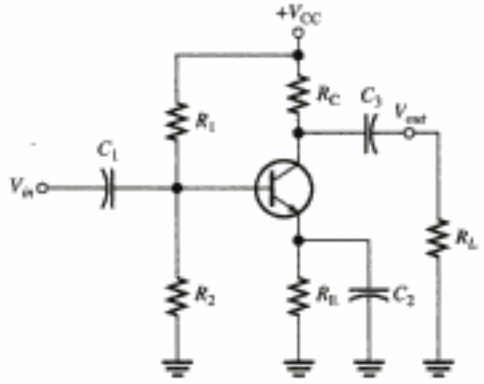
A typical capacitively coupled common-emitter amplifier is shown in Figure 10–8. Assuming that the coupling and bypass capacitors are ideal shorts at the midrange signal frequency, you can determine the midrange voltage gain using Equation 10–5, where $R_c = R_C \parallel R_L$.

Equation 10–5

$$A_{v(mid)} = \frac{R_c}{r'_e}$$

► FIGURE 10–8

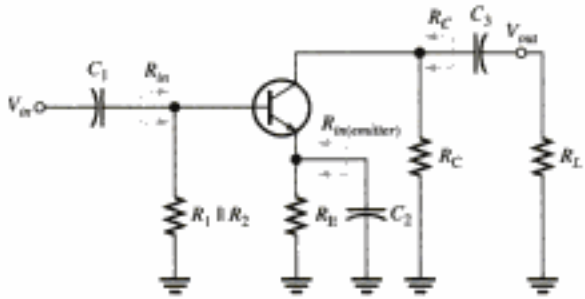
A capacitively coupled amplifier.



The BJT amplifier in Figure 10–8 has three high-pass *RC* circuits that affect its gain as the frequency is reduced below midrange. These are shown in the low-frequency ac equivalent circuit in Figure 10–9. Unlike the ac equivalent circuit used in previous chapters, which represented midrange response ($X_C \equiv 0\ \Omega$), the low-frequency equivalent circuit retains the coupling and bypass capacitors because X_C is not small enough to neglect when the signal frequency is sufficiently low.

► FIGURE 10–9

The low-frequency ac equivalent circuit of the amplifier in Figure 10–8 consists of three high-pass *RC* circuits.



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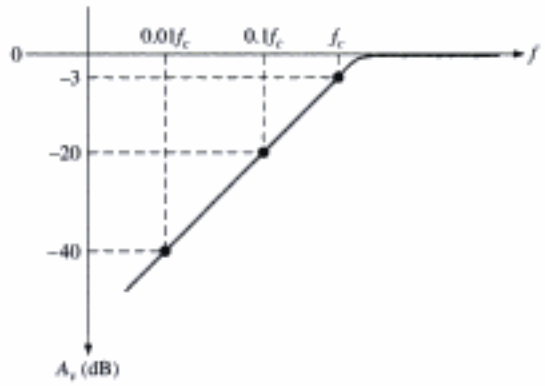

◀ FIGURE 10–11

dB voltage gain versus frequency for the input *RC* circuit.

decrease in frequency from 100 kHz to 50 kHz is also an octave. A rate of −20 dB/decade is approximately equivalent to −6 dB/octave, a rate of −40 dB/decade is approximately equivalent to −12 dB/octave, and so on.

EXAMPLE 10–4

The midrange voltage gain of a certain amplifier is 100. The input *RC* circuit has a lower critical frequency of 1 kHz. Determine the actual voltage gain at $f = 1$ kHz, $f = 100$ Hz, and $f = 10$ Hz.

Solution When $f = 1$ kHz, the voltage gain is 3 dB less than at midrange. At −3 dB, the voltage gain is reduced by a factor of 0.707.

$$A_v = (0.707)(100) = \mathbf{70.7}$$

When $f = 100\text{ Hz} = 0.1f_c$, the voltage gain is 20 dB less than at f_c. The voltage gain at −20 dB is one-tenth of that at the midrange frequencies.

$$A_v = (0.1)(100) = \mathbf{10}$$

When $f = 10\text{ Hz} = 0.01f_c$, the voltage gain is 20 dB less than at $f = 0.1f_c$ or −40 dB. The voltage gain at −40 dB is one-tenth of that at −20 dB or one-hundredth that at the midrange frequencies.

$$A_v = (0.01)(100) = \mathbf{1}$$

Phase Shift in the Input RC Circuit In addition to reducing the voltage gain, the input *RC* circuit also causes an increasing phase shift through an amplifier as the frequency decreases. At midrange frequencies, the phase shift through the input *RC* circuit is approximately zero because the capacitive reactance, X_{C1}, is approximately 0 Ω. At lower frequencies, higher values of X_{C1} cause a phase shift to be introduced, and the output voltage of the *RC* circuit leads the input voltage. As you learned in ac circuit theory, the phase angle in an input *RC* circuit is expressed as

$$\theta = \tan^{-1}\left(\frac{X_{C1}}{R_{in}}\right)$$

Equation 10–7

For midrange frequencies, $X_{C1} \cong 0\ \Omega$, so

$$\theta = \tan^{-1}\left(\frac{0\ \Omega}{R_{in}}\right) = \tan^{-1}(0) = 0°$$

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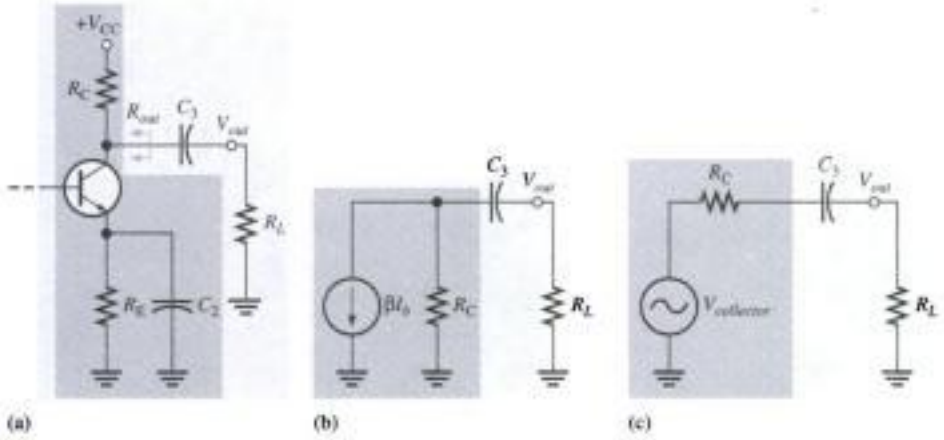


◀ FIGURE 10–14

Development of the equivalent low-frequency output *RC* circuit.

EXAMPLE 10–5

For an output *RC* circuit in a certain amplifier, $R_C = 10\ \text{k}\Omega$, $C_3 = 0.1\ \mu\text{F}$, and $R_L = 10\ \text{k}\Omega$.

(a) Determine the critical frequency.

(b) What is the attenuation of the output *RC* circuit at the midrange frequencies and at the critical frequency?

(c) If the midrange voltage gain of the amplifier is 50, what is the gain at the critical frequency?

Solution **(a)**
$$f_c = \frac{1}{2\pi(R_C + R_L)C_3} = \frac{1}{2\pi(20\ \text{k}\Omega)(0.1\ \mu\text{F})} = \mathbf{79.6\ Hz}$$

(b) For the midrange frequencies, $X_{C3} \cong 0\ \Omega$; thus, the attenuation of the circuit as determined from Figure 10–14(c) is

$$\frac{V_{out}}{V_{collector}} = \frac{R_L}{R_C + R_L} = \frac{10\ \text{k}\Omega}{20\ \text{k}\Omega} = \mathbf{0.5}$$

or, in dB, $V_{out}/V_{collector} = 20\log(0.5) = -6\ \text{dB}$. This shows that, in this case, the midrange voltage gain is reduced by 6 dB because of the load resistor. At the critical frequency, $X_{C3} = R_C + R_L$ and the attenuation is

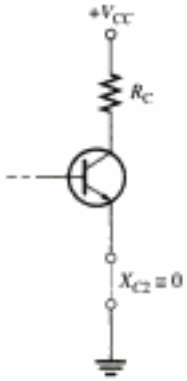
$$\frac{V_{out}}{V_{in}} = \frac{R_L}{\sqrt{(R_C + R_L)^2 + X_{C3}^2}} = \frac{10\ \text{k}\Omega}{\sqrt{(20\ \text{k}\Omega)^2 + (20\ \text{k}\Omega)^2}} = \mathbf{0.354}$$

or, in dB, $V_{out}/V_{collector} = 20\log(0.354) = -9\ \text{dB}$. As you can see, the gain at f_c is 3 dB less than the gain at midrange.

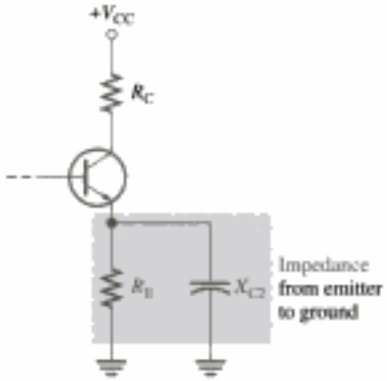
(c) $A_v = 0.707A_{v(mid)} = 0.707(50) = \mathbf{35.4}$

▶ FIGURE 10–15

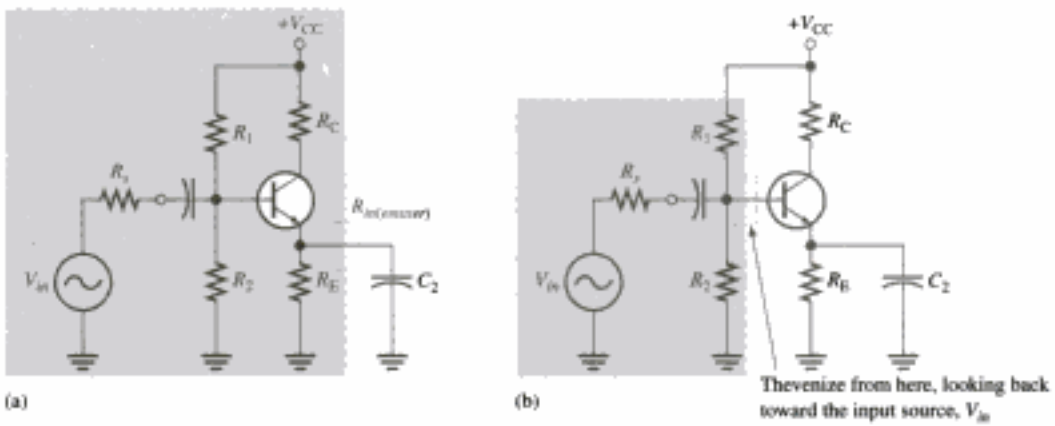
At low frequencies, X_{C2} in parallel with R_E creates an impedance that reduces the voltage gain.

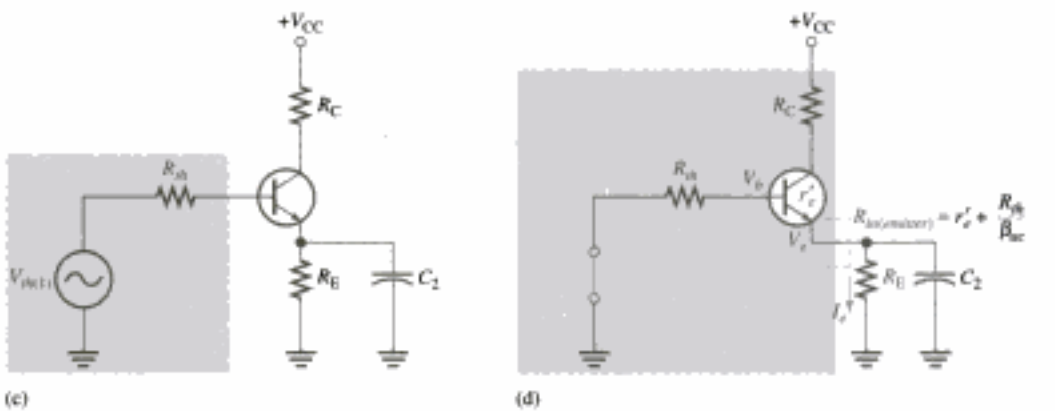


(a) For midrange frequencies, C_2 effectively shorts the emitter to ground.



(b) Below f_s, X_{C2} and R_E form an impedance between the emitter and ground.





▲ FIGURE 10–16

Development of the equivalent bypass *RC* circuit.

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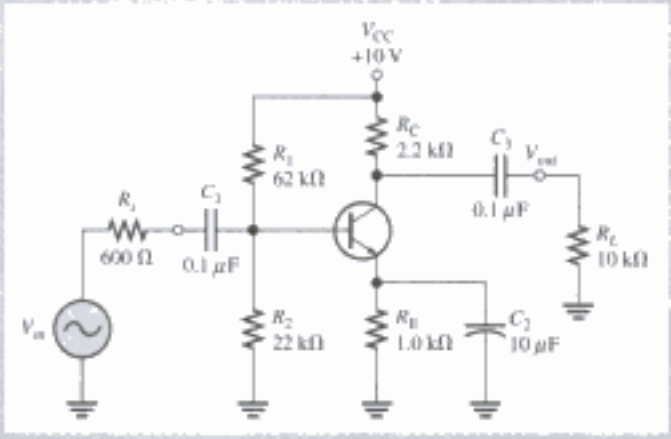
EXAMPLE 10–9

Determine the total low-frequency response of the BJT amplifier in Figure 10–26. $\beta_{ac} = 100$ and $r'_e = 16\ \Omega$.

▶ FIGURE 10–26



Solution Each *RC* circuit is analyzed to determine its critical frequency. For the input *RC* circuit with the source resistance, R_s, taken into account:

$$R_{in} = R_1 \parallel R_2 \parallel \beta_{ac} r'_e = 62\ \text{k}\Omega \parallel 22\ \text{k}\Omega \parallel 1.6\ \text{k}\Omega = 1.46\ \text{k}\Omega$$

$$f_{c(input)} = \frac{1}{2\pi(R_s + R_{in})C_1} = \frac{1}{2\pi(600\ \Omega + 1.46\ \text{k}\Omega)(0.1\ \mu\text{F})} = \mathbf{773\ Hz}$$

For the bypass *RC* circuit:

$$R_{bb} = R_1 \parallel R_2 \parallel R_s = 62\ \text{k}\Omega \parallel 22\ \text{k}\Omega \parallel 600\ \Omega = 579\ \Omega$$

$$R_{in(emitter)} = r'_e + \frac{R_{bb}}{\beta_{ac}} = 16\ \Omega + \frac{579\ \Omega}{100} = 21.8\ \Omega$$

$$f_{c(bypass)} = \frac{1}{2\pi(R_{in(emitter)} \parallel R_E)C_2} = \frac{1}{2\pi(21.8\ \Omega \parallel 1.0\ \text{k}\Omega)(10\ \mu\text{F})}$$

$$= \frac{1}{2\pi(21.3\ \Omega)(10\ \mu\text{F})} = \mathbf{747\ Hz}$$

For the output *RC* circuit:

$$f_{c(output)} = \frac{1}{2\pi(R_C + R_L)C_3} = \frac{1}{2\pi(2.2\ \text{k}\Omega + 10\ \text{k}\Omega)(0.1\ \mu\text{F})} = \mathbf{130.5\ Hz}$$

The analysis shows that the input circuit produces the dominant (which is the highest f_c) lower critical frequency. The midrange voltage gain of the amplifier is

$$A_{v(mid)} = \frac{R_c}{r'_e} = \frac{R_C \parallel R_L}{r'_e} = \frac{2.2\ \text{k}\Omega \parallel 10\ \text{k}\Omega}{16\ \Omega} = 113$$

The midrange attenuation of the input circuit is

$$\frac{R_1 \parallel R_2 \parallel \beta_{ac} r'_e}{R_s + R_1 \parallel R_2 \parallel \beta_{ac} r'_e} = \frac{62\ \text{k}\Omega \parallel 22\ \text{k}\Omega \parallel 1600\ \Omega}{600\ \Omega + 62\ \text{k}\Omega \parallel 22\ \text{k}\Omega \parallel 1600\ \Omega} \approx \frac{1456}{2056} = 0.708$$

The overall voltage gain is

$$A'_{v(mid)} = 0.708(113) = 80$$

and is expressed in dB as

$$A'_{v(mid)(dB)} = 20 \log(80) = 38.1\ \text{dB}$$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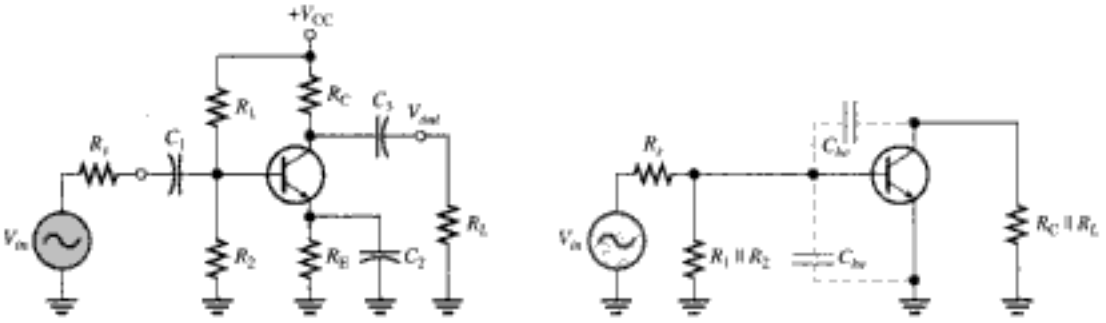


(a) Capacitively coupled amplifier (b) High-frequency equivalent circuit

▲ FIGURE 10–28

Capacitively coupled amplifier and its high-frequency equivalent circuit.

which are significant only at high frequencies, do appear in the diagram. As previously mentioned, C_{be} is sometimes called the input capacitance C_{ib}, and C_{bc} is sometimes called the output capacitance C_{ob}. C_{be} is specified on data sheets at a certain value of V_{BE}. Often, a data sheet will list C_{ib} as C_{ibo} and C_{ob} as C_{obo}. The o as the last letter in the subscript indicates the capacitance is measured with the base open. For example, a 2N2222A transistor has a C_{be} of 25 pF at $V_{EB} = 0.5$ V dc, $I_C = 0$, and $f = 1$ MHz. Also, C_{bc} is specified at a certain value of V_{CB}. The 2N2222A has a maximum C_{bc} of 8 pF at $V_{CB} = 10$ V dc.

Miller's Theorem in High-Frequency Analysis By applying Miller's theorem to the circuit in Figure 10–28(b) and using the midrange voltage gain, you have a circuit that can be analyzed for high-frequency response. Looking in from the signal source, the capacitance C_{bc} appears in the Miller input capacitance from base to ground.

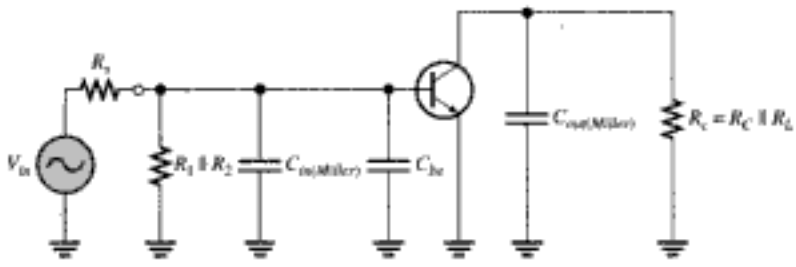
$$C_{in(Miller)} = C_{bc}(A_v + 1)$$

C_{be} simply appears as a capacitance to ac ground, as shown in Figure 10–29, in parallel with $C_{in(Miller)}$. Looking in at the collector, C_{bc} appears in the Miller output capacitance from collector to ground. As shown in Figure 10–29, it appears in parallel with R_c.

$$C_{out(Miller)} = C_{bc}\left(\frac{A_v + 1}{A_v}\right)$$

These two Miller capacitances create a high-frequency input RC circuit and a high-frequency output RC circuit. These two circuits differ from the low-frequency input and output circuits, which act as high-pass filters, because the capacitances go to ground and therefore act as low-pass filters. The equivalent circuit in Figure 10–29 is an ideal model because stray capacitances that are due to circuit interconnections are neglected.

The Input RC Circuit At high frequencies, the input circuit is as shown in Figure 10–30(a), where $\beta_{ac}r'_e$ is the input resistance at the base of the transistor because the bypass capacitor effectively shorts the emitter to ground. By combining C_{be} and $C_{in(Miller)}$ in parallel and repositioning, you get the simplified circuit shown in Figure 10–30(b). Next, by thevenizing the circuit to the left of the capacitor, as indicated, the input RC circuit is reduced to the equivalent form shown in Figure 10–30(c).



◀ FIGURE 10–29

High-frequency equivalent circuit after applying Miller's theorem.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Phase Shift of the Input RC Circuit Because the output voltage of a high-frequency input *RC* circuit is across the capacitor, the output of the circuit lags the input. The phase angle is expressed as

Equation 10–17

$$\theta = \tan^{-1}\left(\frac{R_s \,|\, R_1 \,\|\, R_2 \,\|\, \beta_{ac} r'_e}{X_{C_{int}}}\right)$$

At the critical frequency, the phase angle is 45° with the signal voltage at the base of the transistor lagging the input signal. As the frequency increases above f_c, the phase angle increases above 45° and approaches 90° when the frequency is sufficiently high.

The Output RC Circuit The high-frequency output *RC* circuit is formed by the Miller output capacitance and the resistance looking in at the collector, as shown in Figure 10–33(a). In determining the output resistance, the transistor is treated as a current source (open) and one end of R_C is effectively ac ground, as shown in Figure 10–33(b). By rearranging the position of the capacitance in the diagram and thevenizing the circuit to the left, as shown in Figure 10–33(c), you get the equivalent circuit in Figure 10–33(d). The equivalent output *RC* circuit consists of a resistance equal to R_C and R_L in parallel in series with a capacitance that is determined by the following Miller formula:

$$C_{out(Miller)} = C_{bc}\left(\frac{A_v + 1}{A_v}\right)$$

If the voltage gain is at least 10, this formula can be approximated as

$$C_{out(Miller)} \cong C_{bc}$$

The critical frequency is determined with the following equation, where $R_c = R_C \,\|\, R_L$.

Equation 10–18

$$f_c = \frac{1}{2\pi R_c C_{out(Miller)}}$$

Just as in the input *RC* circuit, the output *RC* circuit reduces the gain by 3 dB at the critical frequency. When the frequency goes above the critical value, the gain drops at a −20 dB/decade rate. The phase angle introduced by the output *RC* circuit is

Equation 10–19

$$\theta = \tan^{-1}\left(\frac{R_c}{X_{C_{out(Miller)}}}\right)$$

▶ FIGURE 10–33

Development of the equivalent high-frequency output *RC* circuit.

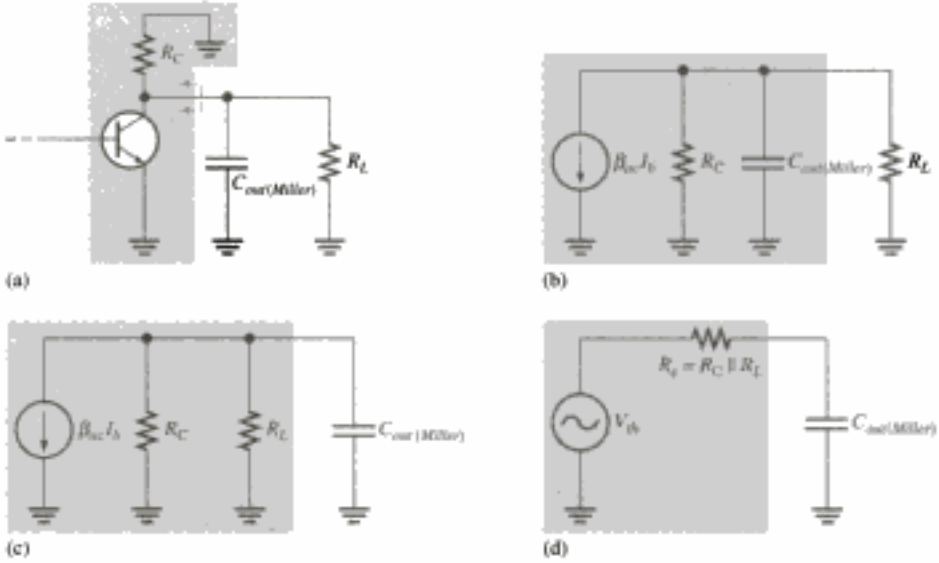


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Figure 10–35(b).Notice that the coupling and bypass capacitors are assumed to have negligible reactances and are considered to be shorts. The internal capacitances C_{gs} and C_{gd} appear in the equivalent circuit because their reactances are significant at high frequencies.

Values of C_{gs}, C_{gd}, and C_{ds} FET data sheets do not normally provide values for C_{gs}, C_{gd}, or C_{ds}. Instead, three other values are usually specified because they are easier to measure. These are C_{iss}, the input capacitance; C_{rss}, the reverse transfer capacitance; and C_{oss}, the output capacitance. Because of the manufacturer's method of measurement, the following relationships allow you to determine the capacitor values needed for analysis.

Equation 10–20
$$C_{gd} = C_{rss}$$

Equation 10–21
$$C_{gs} = C_{iss} - C_{rss}$$

Equation 10–22
$$C_{ds} = C_{oss} - C_{rss}$$

C_{oss} is not specified as often as the other values on data sheets. Sometimes, it is designated as $C_{d(sub)}$, the drain-to-substrate capacitance. In cases where a value is not available, you must either assume a value or neglect C_{ds}.

EXAMPLE 10–12

The data sheet for a 2N3823 JFET gives $C_{iss} = 6$ pF and $C_{rss} = 2$ pF. Determine C_{gd} and C_{gs}.

Solution

$$C_{gd} = C_{rss} = \mathbf{2\ pF}$$
$$C_{gs} = C_{iss} - C_{rss} = 6\text{ pF} - 2\text{ pF} = \mathbf{4\ pF}$$

Using Miller's Theorem Miller's theorem is applied the same way in FET amplifier high-frequency analysis as was done in BJT amplifiers. Looking in from the signal source in Figure 10–35(b), C_{gd} effectively appears in the Miller input capacitance, which was given in Equation 10–1, as follows:

$$C_{in\,(Miller)} = C_{gd}(A_v + 1)$$

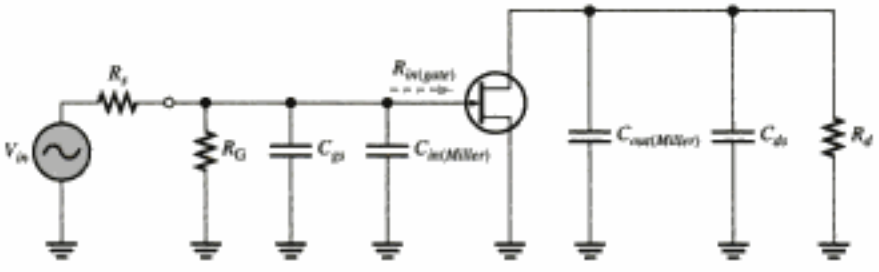
C_{gs} simply appears as a capacitance to ac ground in parallel with $C_{in(Miller)}$, as shown in Figure 10–36. Looking in at the drain, C_{gd} effectively appears in the Miller output capacitance (from Equation 10–2) from drain to ground in parallel with R_d, as shown in Figure 10–36.

$$C_{out(Miller)} = C_{gd}\left(\frac{A_v + 1}{A_v}\right)$$

These two Miller capacitances contribute to a high-frequency input *RC* circuit and a high-frequency output *RC* circuit. Both are low-pass filters which produce phase lag.

▶ **FIGURE 10–36**

High-frequency equivalent circuit after applying Miller's theorem.



The Input RC Circuit The high-frequency input circuit forms a low-pass type of filter and is shown in Figure 10–37(a). Because both R_G and the input resistance at the gate of FETs are extremely high, the controlling resistance for the input circuit is the resistance

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The total input capacitance is

$$C_{in(tot)} = C_{gs} + C_{in(Miller)} = 5\text{ pF} + 22.5\text{ pF} = 27.5\text{ pF}$$

The critical frequency is

$$f_c = \frac{1}{2\pi R_s C_{in(tot)}} = \frac{1}{2\pi(50\ \Omega)(27.5\text{ pF})} = \mathbf{116\text{ MHz}}$$

The Output RC Circuit The high-frequency output *RC* circuit is formed by the Miller output capacitance and the output resistance looking in at the drain, as shown in Figure 10–39(a). As in the case of the BJT, the FET is treated as a current source. When you apply Thevenin's theorem, you get an equivalent output *RC* circuit consisting of R_D in parallel with R_L and an equivalent output capacitance.

$$C_{out(Miller)} = C_{gd}\left(\frac{A_v + 1}{A_v}\right)$$

This equivalent output circuit is shown in Figure 10–39(b). The critical frequency of the output *RC* lag circuit is

Equation 10–25

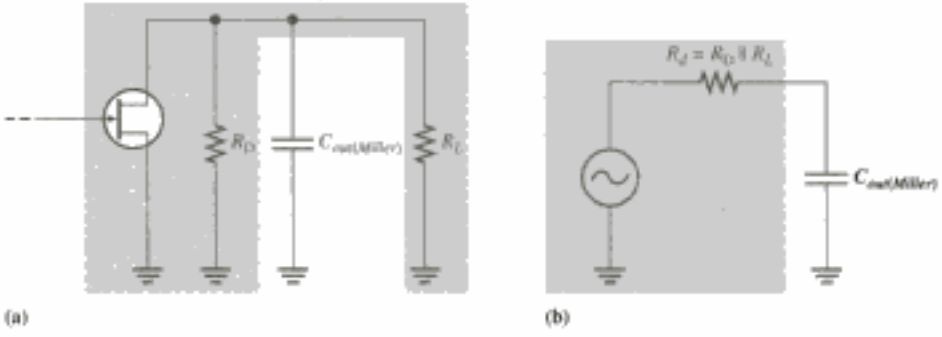
$$f_c = \frac{1}{2\pi R_d C_{out(Miller)}}$$

The output circuit produces a phase shift of

Equation 10–26

$$\theta = \tan^{-1}\left(\frac{R_d}{X_{C_{out(Miller)}}}\right)$$

► FIGURE 10–39
Output *RC* circuit.



EXAMPLE 10–14

Determine the critical frequency of the output *RC* circuit for the FET amplifier in Figure 10–38. What is the phase shift introduced by this circuit at the critical frequency? Which *RC* circuit is dominant?

Solution Since R_L is very large compared to R_D, it can be neglected, and the equivalent output resistance is

$$R_d \cong R_D = 1.0\text{ k}\Omega$$

The equivalent output capacitance is

$$C_{out(Miller)} = C_{gd}\left(\frac{A_v + 1}{A_v}\right) = (3\text{ pF})\left(\frac{7.5}{6.5}\right) = 3.46\text{ pF}$$

Therefore, the critical frequency is

$$f_c = \frac{1}{2\pi R_s C_{out(Miller)}} = \frac{1}{2\pi(1.0\text{ k}\Omega)(3.46\text{ pF})} = \mathbf{46\text{ MHz}}$$

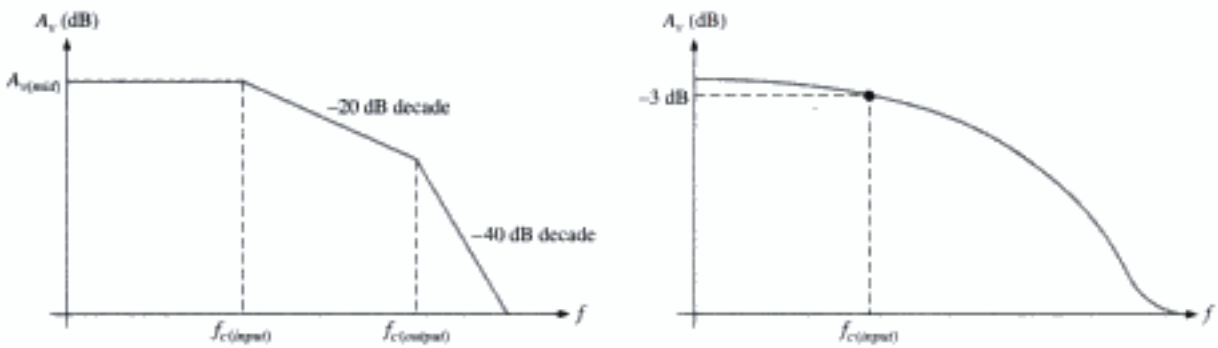
Although it has been neglected, any stray wiring capacitance could significantly affect the frequency response because $C_{out(Miller)}$ is very small.

The phase angle is always **45°** at f_c for an *RC* circuit and the output lags.

In Example 10–13, the critical frequency of the input *RC* circuit was found to be 116 MHz. Therefore, the critical frequency for the output circuit is dominant because it is the lesser of the two.

Total High-Frequency Response of an Amplifier

As you have seen, the two *RC* circuits created by the internal transistor capacitances influence the high-frequency response of both BJT and FET amplifiers. As the frequency increases and reaches the high end of its midrange values, one of the *RC* circuits will cause the amplifier's gain to begin dropping off. The frequency at which this occurs is the dominant critical frequency; it is the lower of the two critical high frequencies. An ideal high-frequency Bode plot is shown in Figure 10–40(a). It shows the first break point at $f_{c(input)}$ where the voltage gain begins to roll off at −20 dB/decade. At $f_{c(output)}$, the gain begins dropping at −40 dB/decade because each *RC* circuit is providing a −20 dB/decade roll-off. Figure 10–40(b) shows a nonideal Bode plot where the voltage gain is actually −3 dB below midrange at $f_{c(input)}$. Other possibilities are that the output *RC* circuit is dominant or that both circuits have the same critical frequency.



(a) Ideal (b) Nonideal

▲ FIGURE 10–40

High-frequency Bode plots.

SECTION 10–4 REVIEW

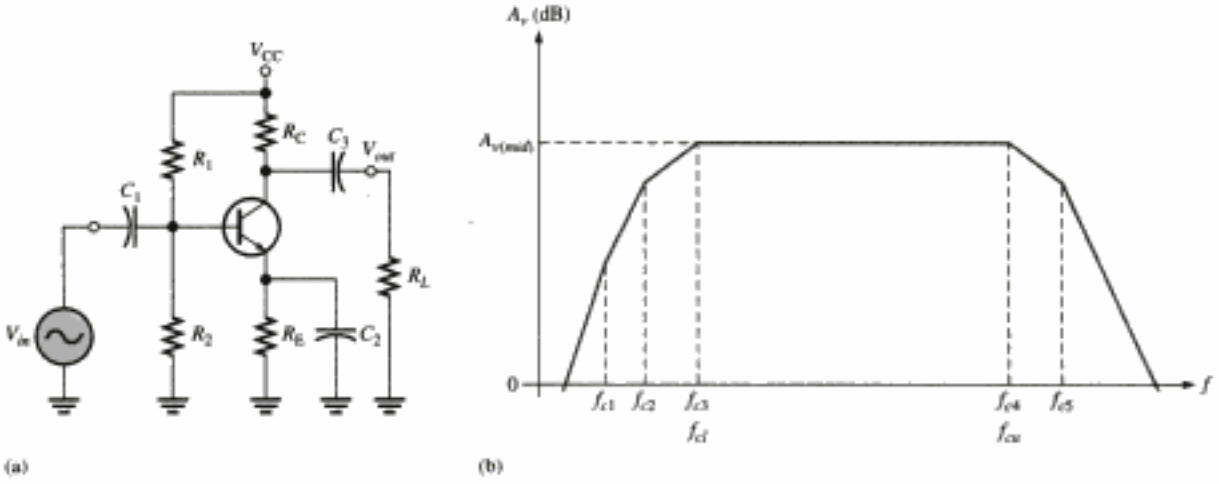
1. What determines the high-frequency response of an amplifier?
2. If an amplifier has a midrange voltage gain of 80, the transistor's C_{bc} is 4 pF, and C_{be} = 8 pF, what is the total input capacitance?
3. A certain amplifier has $f_{c(input)}$ = 3.5 MHz and $f_{c(output)}$ = 8.2 MHz. Which circuit dominates the high-frequency response?
4. What are the capacitances that are usually specified on a FET data sheet?
5. If C_{gs} = 4 pF and C_{gd} = 3 pF, what is the total input capacitance of a FET amplifier whose voltage gain is 25?

10–5 TOTAL AMPLIFIER FREQUENCY RESPONSE

In the previous sections, you learned how each *RC* circuit in an amplifier affects the frequency response. In this section, we will bring these concepts together and examine the total response of typical amplifiers and the specifications relating to their performance.

Figure 10–41(b) shows a generalized ideal response curve (Bode plot) for the BJT amplifier shown in Figure 10–41(a). As previously discussed, the three break points at the lower critical frequencies (f_{c1}, f_{c2}, and f_{c3}) are produced by the three low-frequency *RC* circuits formed by the coupling and bypass capacitors. The break points at the upper critical frequencies, f_{c4} and f_{c5}, are produced by the two high-frequency *RC* circuits formed by the transistor's internal capacitances.

Of particular interest are the two dominant critical frequencies, f_{c3} and f_{c4}, in Figure 10–41(b). These two frequencies are where the voltage gain of the amplifier is 3 dB below its midrange value. These dominant frequencies are referred to as the *lower critical frequency*, f_{cl}, and the *upper critical frequency*, f_{cu}.



▲ FIGURE 10–41

A BJT amplifier and its generalized ideal response curve (Bode plot).

The upper and lower critical frequencies are sometimes called the *half-power frequencies*. This term is derived from the fact that the output power of an amplifier at its critical frequencies is one-half of its midrange power, as previously mentioned. This can be shown as follows, starting with the fact that the output voltage is 0.707 of its midrange value at the critical frequencies.

$$V_{out(f_c)} = 0.707V_{out(mid)}$$

$$P_{out(f_c)} = \frac{V^2_{out(f_c)}}{R_{out}} = \frac{(0.707V_{out(mid)})^2}{R_{out}} = \frac{0.5V^2_{out(mid)}}{R_{out}} = 0.5P_{out(mid)}$$

Bandwidth

An amplifier normally operates with signal frequencies between f_{cl} and f_{cu}. As you know, when the input signal frequency is at f_{cl} or f_{cu}, the output signal voltage level is 70.7% of its midrange value or −3 dB. If the signal frequency drops below f_{cl}, the gain and thus the output signal level drops at 20 dB/decade until the next critical frequency is reached. The same occurs when the signal frequency goes above f_{cu}.

The range (band) of frequencies lying between f_{cl} and f_{cu} is defined as the **bandwidth** of the amplifier, as illustrated in Figure 10–42. Only the dominant critical frequencies appear in the response curve because they determine the bandwidth. Also, sometimes the other critical frequencies are far enough away from the dominant frequencies that they play no

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gain (0 dB) is reached. The frequency at which the amplifier's gain is 1 is called the *unity-gain frequency*, f_T. The significance of f_T is that it always equals the midrange voltage gain times the bandwidth and is constant for a given transistor.

Equation 10–28

$$f_T = A_{v(mid)}BW$$

For the case shown in Figure 10–43, $f_T = A_{v(mid)}f_{cu}$. For example, if a transistor data sheet specifies $f_T = 100$ MHz, this means that the transistor is capable of producing a voltage gain of 1 up to 100 MHz, or a gain of 100 up to 1 MHz, or any combination of gain and bandwidth that produces a product of 100 MHz.

EXAMPLE 10–16

A certain transistor has an f_T of 175 MHz. When this transistor is used in an amplifier with a midrange voltage gain of 50, what bandwidth can be achieved ideally?

Solution

$$f_T = A_{v(mid)}BW$$

$$BW = \frac{f_T}{A_{v(mid)}} = \frac{175\text{ MHz}}{50} = \mathbf{3.5\text{ MHz}}$$

SECTION 10–5 REVIEW

1. What is the voltage gain of an amplifier at f_T?
2. What is the bandwidth of an amplifier when $f_{cu} = 25$ kHz and $f_{cl} = 100$ Hz?
3. The f_T of a certain transistor is 130 MHz. What voltage gain can be achieved with a bandwidth of 50 MHz?

10–6 FREQUENCY RESPONSE OF MULTISTAGE AMPLIFIERS

To this point, you have seen how the voltage gain of a single-stage amplifier changes over frequency. When two or more stages are cascaded to form a multistage amplifier, the overall frequency response is determined by the frequency response of each stage depending on the relationships of the critical frequencies.

When amplifier stages are cascaded to form a multistage amplifier, the dominant frequency response is determined by the responses of the individual stages. There are two cases to consider:

1. Each stage has a different lower critical frequency and a different upper critical frequency.
2. Each stage has the same lower critical frequency and the same upper critical frequency.

Different Critical Frequencies

When the lower critical frequency, f_{cl}, of each amplifier stage is different, the dominant lower critical frequency, f'_{cl}, equals the critical frequency of the stage with the highest f_{cl}.

When the upper critical frequency, f_{cu}, of each amplifier stage is different, the dominant upper critical frequency, f'_{cu}, equals the critical frequency of the stage with the lowest f_{cu}.

Overall Bandwidth The bandwidth of a multistage amplifier is the difference between the dominant lower critical frequency and the dominant upper critical frequency.

$$BW = f'_{cu} - f'_{cl}$$

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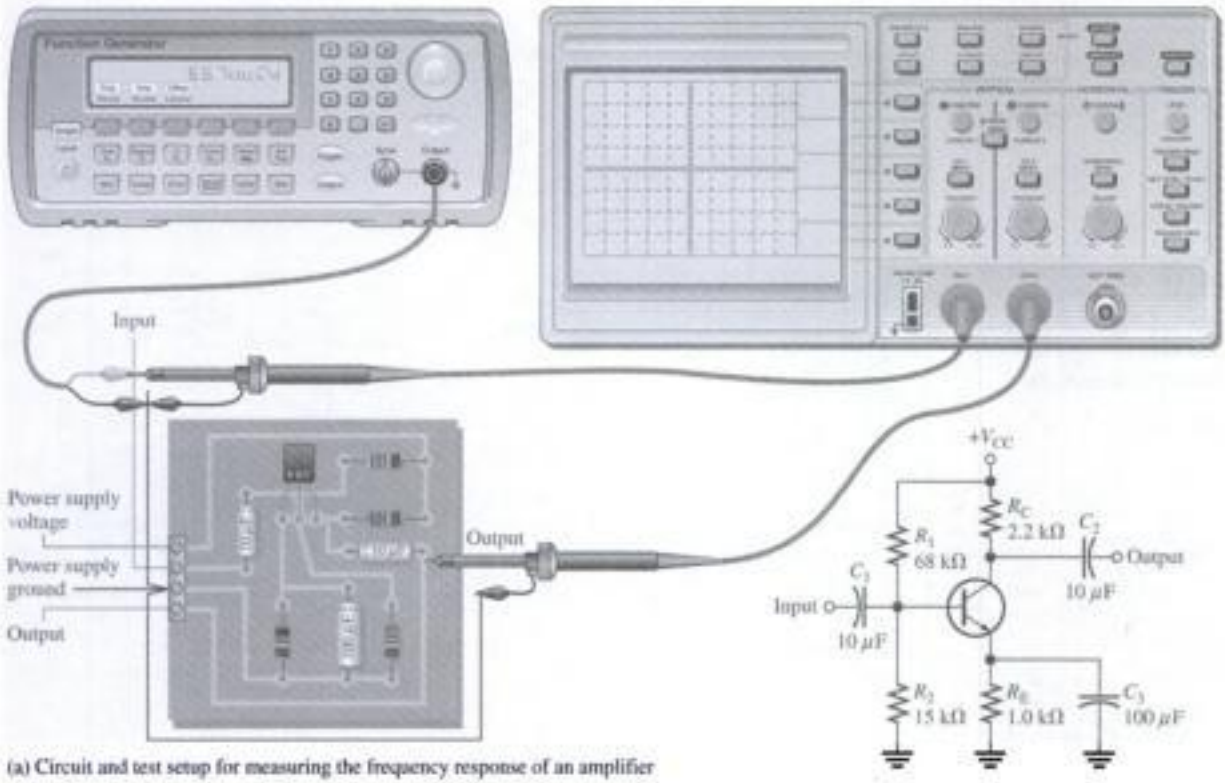
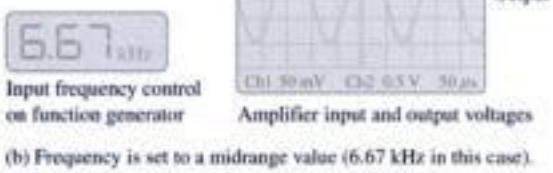


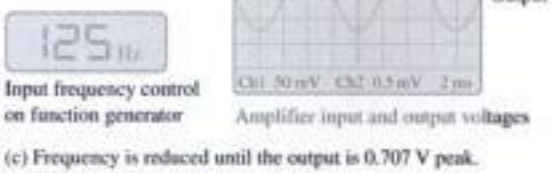
(a) Circuit and test setup for measuring the frequency response of an amplifier



Input frequency control on function generator

Amplifier input and output voltages

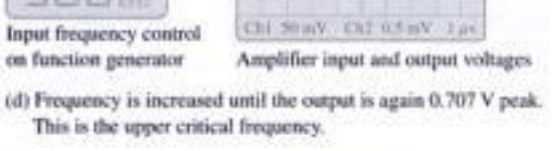
(b) Frequency is set to a midrange value (6.67 kHz in this case). Input voltage adjusted for an output of 1 V peak.



Input frequency control on function generator

Amplifier input and output voltages

(c) Frequency is reduced until the output is 0.707 V peak. This is the lower critical frequency.



Input frequency control on function generator

Amplifier input and output voltages

(d) Frequency is increased until the output is again 0.707 V peak. This is the upper critical frequency.

▲ FIGURE 10–44

A general procedure for measuring an amplifier's frequency response.

time base so the complete interval of the fall time can be observed. Once this measurement is made, f_{cl} can be determined with the following formula.

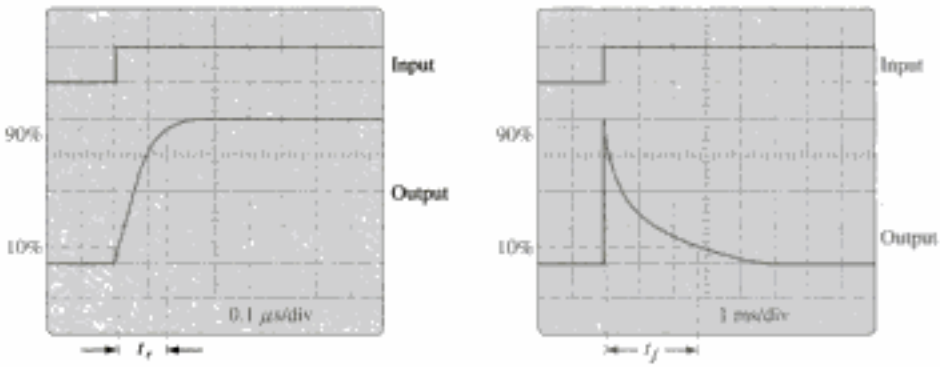
Equation 10–32

$$f_{cl} = \frac{0.35}{t_f}$$

The derivations of Equations 10–31 and 10–32 are in Appendix B.

▶ FIGURE 10–45

Measurement of the rise and fall times associated with the amplifier's step response. The outputs are inverted.



(a) Measurement of output rise time to determine the upper critical frequency

(b) Measurement of output fall time to determine the lower critical frequency

SECTION 10–7 REVIEW

1. In Figure 10–44, what are the lower and upper critical frequencies?
2. The rise time and the fall time of an amplifier's output voltage are measured between what two points on the voltage transition?
3. In Figure 10–45, what is the rise time?
4. In Figure 10–45, what is the fall time?
5. What is the bandwidth of the amplifier whose step response is measured in Figure 10–45?

CHAPTER SUMMARY

- The coupling and bypass capacitors of an amplifier affect the low-frequency response.
- The internal transistor capacitances affect the high-frequency response.
- Critical frequencies are values of frequency at which the *RC* circuits reduce the voltage gain to 70.7% of its midrange value.
- Each *RC* circuit causes the gain to drop at a rate of 20 dB/decade.
- For the low-frequency *RC* circuits, the *highest* critical frequency is the dominant critical frequency.
- For the high-frequency *RC* circuits, the *lowest* critical frequency is the dominant critical frequency.
- A decade of frequency change is a ten-times change (increase or decrease).
- An octave of frequency change is a two-times change (increase or decrease).
- The bandwidth of an amplifier is the range of frequencies between the lower critical frequency and the upper critical frequency.
- The gain-bandwidth product is a transistor parameter that is constant and equal to the unity-gain frequency.

OBJECTIVE TYPE QUESTIONS

Answers are at the end of the chapter.

1. If the value of R_1 in Figure 10–8 is increased, the signal voltage at the base will
   (a) increase **(b)** decrease **(c)** not change
2. If the value of C_1 in Figure 10–26 is decreased, the critical frequency associated with the input circuit will
   (a) increase **(b)** decrease **(c)** not change
3. If the value of R_L in Figure 10–26 is increased, the voltage gain will
   (a) increase **(b)** decrease **(c)** not change
4. If the value of R_C in Figure 10–26 is decreased, the voltage gain will
   (a) increase **(b)** decrease **(c)** not change
5. If V_{CC} in Figure 10–31 is increased, the dc emitter voltage will
   (a) increase **(b)** decrease **(c)** not change
6. If the transistor in Figure 10–31 is replaced with one having a higher β_{ac}, the critical frequency will
   (a) increase **(b)** decrease **(c)** not change
7. If the transistor in Figure 10–31 is replaced with one having a lower β_{ac}, the midrange voltage gain will
   (a) increase **(b)** decrease **(c)** not change
8. If the value of R_D in Figure 10–38 is increased, the voltage gain will
   (a) increase **(b)** decrease **(c)** not change
9. If the value of R_L in Figure 10–38 is increased, the critical frequency will
   (a) increase **(b)** decrease **(c)** not change
10. If the FET in Figure 10–38 is replaced with one having a higher g_m, the critical frequency will
    (a) increase **(b)** decrease **(c)** not change
11. The low-frequency response of an amplifier is determined in part by
    (a) the voltage gain **(b)** the type of transistor
    (c) the supply voltage **(d)** the coupling capacitors
12. The high-frequency response of an amplifier is determined in part by
    (a) the gain-bandwidth product **(b)** the bypass capacitor
    (c) the internal transistor capacitances **(d)** the roll-off
13. The bandwidth of an amplifier is determined by
    (a) the midrange gain **(b)** the critical frequencies
    (c) the roll-off rate **(d)** the input capacitance
14. The gain of a certain amplifier decreases by 6 dB when the frequency is reduced from 1 kHz to 10 Hz. The roll-off is
    (a) −3 dB/decade **(b)** −6 dB/decade **(c)** −3 dB/octave **(d)** −6 dB/octave
15. The gain of a particular amplifier given frequency decreases by 6 dB when the frequency is doubled. The roll-off is
    (a) −12 dB/decade **(b)** −20 dB/decade
    (c) −6 dB/octave **(d)** answers (b) and (c)
16. The Miller input capacitance of an amplifier is dependent, in part, on
    (a) the input coupling capacitor
    (b) the voltage gain
    (c) the bypass capacitor
    (d) none of these

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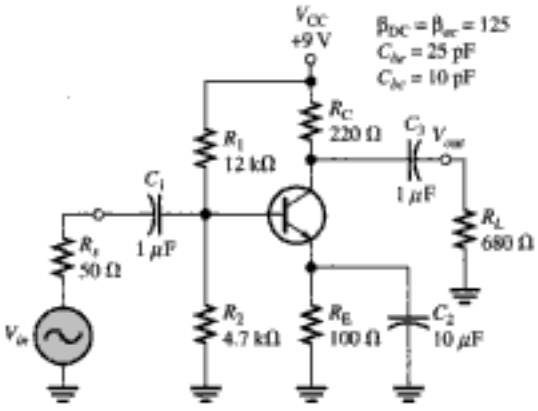
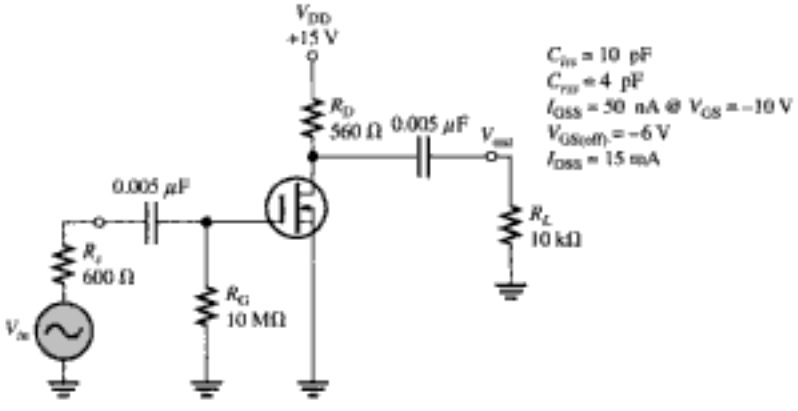
► FIGURE 10–49



15. Determine the voltage gain of the amplifier in Figure 10–49 at one-tenth of the dominant critical frequency, at the dominant critical frequency, and at ten times the dominant critical frequency for the low-frequency response.
16. Determine the phase shift at each of the frequencies used in Problem 15.
17. Determine the critical frequencies associated with the low-frequency response of the FET amplifier in Figure 10–50. Indicate the dominant critical frequency and draw the Bode plot.
18. Find the voltage gain of the amplifier in Figure 10–50 at the following frequencies: f_c, $0.1f_c$, and $10f_c$, where f_c is the dominant critical frequency.

► FIGURE 10–50



SECTION 10–4 High-Frequency Amplifier Response

19. Determine the critical frequencies associated with the high-frequency response of the amplifier in Figure 10–49. Identify the dominant critical frequency and sketch the Bode plot.
20. Determine the voltage gain of the amplifier in Figure 10–49 at the following frequencies: $0.1f_c$, f_c, $10f_c$, and $100f_c$, where f_c is the dominant critical frequency in the high-frequency response.
21. The data sheet for the FET in Figure 10–50 gives $C_{rss} = 4$ pF and $C_{iss} = 10$ pF. Determine the critical frequencies associated with the high-frequency response of the amplifier, and indicate the dominant frequency.
22. Determine the voltage gain in dB and the phase shift at each of the following multiples of the dominant critical frequency in Figure 10–50 for the high-frequency response: $0.1f_c$, f_c, $10f_c$, and $100f_c$.

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3. Coupling and bypass capacitors can be neglected at frequencies for which their reactances are negligible.
4. $C_{in(Miller)} = (5\text{ pF})(51) = 255\text{ pF}$
5. $C_{out(Miller)} = (3\text{ pF})(1.04) = 3.12\text{ pF}$

SECTION 10–2 The Decibel

1. +12 dB corresponds to a voltage gain of approximately 4.
2. $A_p = 10\log(25) = 13.98\text{ dB}$
3. 0 dBm corresponds to 1 mW.

SECTION 10–3 Low-Frequency Amplifier Response

1. $f_{c2} = 167\text{ Hz}$ is dominant.
2. $A_{v(dB)} = 50\text{ dB} - 3\text{ dB} = 47\text{ dB}$
3. −20 dB attenuation at one decade below f_c.
4. $\theta = \tan^{-1}(0.5) = 26.6°$
5. $f_c = 1/(2\pi(6500\ \Omega)(0.0022\ \mu\text{F})) = 11.1\text{ kHz}$

SECTION 10–4 High-Frequency Amplifier Response

1. The internal transistor capacitances determine the high-frequency response.
2. $C_{in(tot)} = C_{in(Miller)} + C_{cc} = (4\text{ pF})(81) + 8\text{ pF} = 342\text{ pF}$
3. The input *RC* circuit dominates.
4. C_{iss} and C_{rss} are usually specified on a FET data sheet.
5. $C_{in(tot)} = (3\text{ pF})(26) + 4\text{ pF} = 82\text{ pF}$

SECTION 10–5 Total Amplifier Frequency Response

1. The gain is 1 at f_T.
2. $BW = 25\text{ kHz} - 100\text{ Hz} = 24.9\text{ kHz}$
3. $A_v = 130\text{ MHz}/50\text{ MHz} = 2.6$

SECTION 10–6 Frequency Response of Multistage Amplifiers

1. $f'_{c1} = 1\text{ kHz}$
2. $f'_{cu} = 49\text{ kHz}$
3. *BW* decreases.

SECTION 10–7 Frequency Response Measurement

1. $f_{c1} = 125\text{ Hz}; f_{cu} = 500\text{ kHz}$
2. Rise time is between the 10% and 90% points and fall time is between the 90% and 10% points.
3. $t_r = 150\text{ ns}$
4. $t_f = 2.8\text{ ms}$
5. Since $f_{cu} >> f_{c1}$, $BW \cong f_{cu} = 2.5\text{ MHz}$.

OBJECTIVE TYPE QUESTIONS

1. (a) **2.** (a) **3.** (a) **4.** (b) **5.** (a) **6.** (b) **7.** (c) **8.** (a) **9.** (b) **10.** (b)
11. (d) **12.** (c) **13.** (b) **14.** (a) **15.** (d) **16.** (b) **17.** (c) **18.** (c) **19.** (a) **20.** (c)
21. (b) **22.** (d) **23.** (c) **24.** (a) **25.** (b)

11

THYRISTORS AND OTHER DEVICES

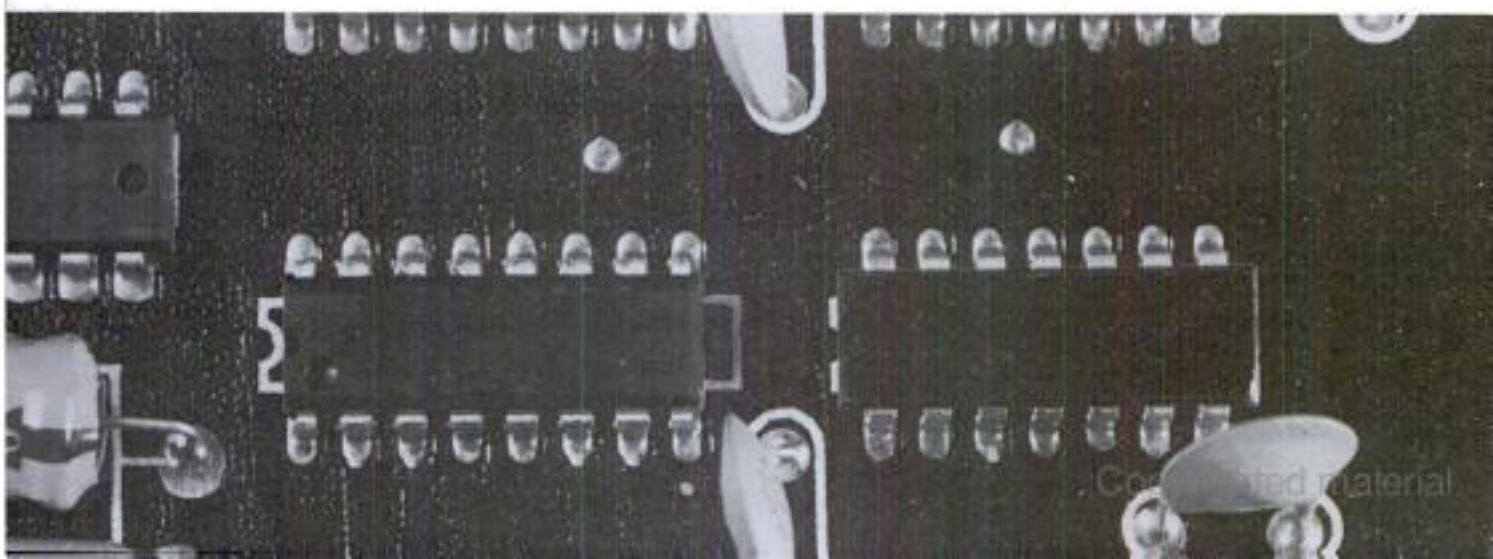
CHAPTER OUTLINE

INTRODUCTION

In this chapter, several types of semiconductor devices are introduced. A family of devices known as thyristors are constructed of four semiconductor layers (*pnpn*). Thyristors include the 4-layer diode, the silicon-controlled rectifier (SCR), the diac, the triac, and the silicon-controlled switch (SCS). These types of thyristors share certain common characteristics in addition to their four-layer construction. They act as open circuits capable of withstanding a certain rated voltage until they are triggered. When triggered, they turn on and become low-resistance current paths and remain so, even after the trigger is removed, until the current is reduced to a certain level or until they are triggered off, depending on the type of device. Thyristors can be used to control the amount of ac power to a load and are used in lamp dimmers, motor speed controls, ignition systems, and charging circuits, to name a few.

Other devices described in this chapter include the unijunction transistor (UJT), the programmable unijunction transistor (PUT), and the insulated-gate bipolar transistor (IGBT). UJTs and PUTs are used as trigger devices for thyristors and also in oscillators and timing circuits. IGBTs are widely used in high-voltage applications.

Optical devices including the phototransistor, light-activated SCR, couplers, fiber-optic cables, and communication links are also discussed.



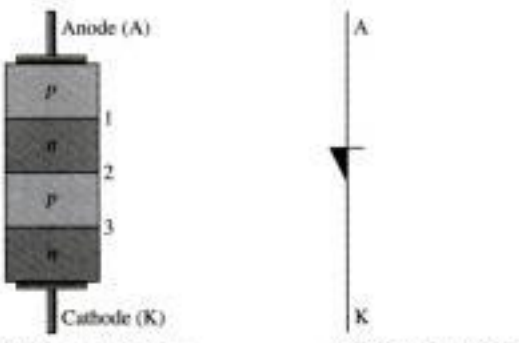
11–1 THE BASIC 4-LAYER DEVICE

The basic thyristor is a 4-layer device with two terminals, the anode and the cathode. It is constructed of four semiconductor layers that form a *pnpn* structure. The device acts as a switch and remains off until the forward voltage reaches a certain value; then it turns on and conducts. Conduction continues until the current is reduced below a specified value. This basic thyristor is also known as a silicon unilateral switch (SUS), Shockley diode, or 4-layer diode.

The **4-layer diode** (also known as Shockley diode and SUS) is a type of **thyristor**, which is a class of devices constructed of four semiconductor layers. The basic construction of a 4-layer diode and its schematic symbol are shown in Figure 11–1.

The *pnpn* structure can be represented by an equivalent circuit consisting of a *pnp* transistor and an *npn* transistor, as shown in Figure 11–2(a). The upper *pnp* layers form Q_1 and the lower *npn* layers form Q_2, with the two middle layers shared by both equivalent transistors. Notice that the base-emitter junction of Q_1 corresponds to *pn* junction 1 in Figure 11–1, the base-emitter junction of Q_2 corresponds to *pn* junction 3, and the base-collector junctions of both Q_1 and Q_2 correspond to *pn* junction 2.

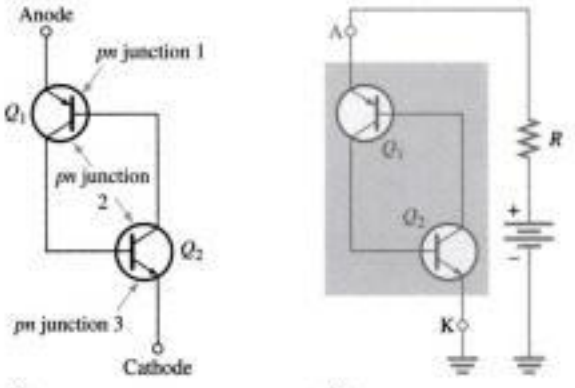
When a positive bias voltage is applied to the anode with respect to the cathode, as shown in Figure 11–2(b), the base-emitter junctions of Q_1 and Q_2 (*pn* junctions 1 and 3 in Figure 11–1(a)) are forward-biased, and the common base-collector junction (*pn* junction 2 in Figure 11–1(a)) is reverse-biased. Therefore, both equivalent transistors are in the linear region.



(a) Basic construction (b) Schematic symbol

▲ FIGURE 11–1

The 4-layer diode.



(a) (b)

▲ FIGURE 11–2

A 4-layer diode equivalent circuit.

The currents in a 4-layer diode are shown in the equivalent circuit in Figure 11–3. At low-bias levels, there is very little anode current, and thus it is in the *off* state or forward-blocking region.

Forward-Breakover Voltage The operation of the 4-layer diode may seem unusual because when it is forward-biased, it can act essentially as an open switch. There is a region of forward bias, called the *forward-blocking region*, in which the device has a very high forward resistance (ideally an open) and is in the *off* state. The forward-blocking region exists from $V_{AK} = 0$ V up to a value of V_{AK} called the **forward-breakover voltage, $V_{BR(F)}$**. This is indicated on the 4-layer diode characteristic curve in Figure 11–4.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SECTION 11–1 REVIEW

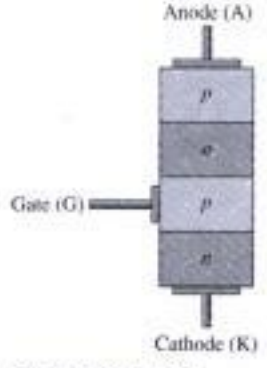
Answers are at the end of the chapter.

1. Why is the 4-layer diode classified as a thyristor?
2. What is the forward-blocking region?
3. What happens when the anode-to-cathode voltage exceeds the forward-breakover voltage?
4. Once it is on, how can the 4-layer diode be turned off?

11–2 THE SILICON-CONTROLLED RECTIFIER (SCR)

Like the 4-layer diode, the SCR has two possible states of operation. In the *off* state, it acts ideally as an open circuit between the anode and the cathode; actually, rather than an open, there is a very high resistance. In the *on* state, the SCR acts ideally as a short from the anode to the cathode; actually, there is a small *on* (forward) resistance. The SCR is used in many applications, including motor controls, time-delay circuits, heater controls, phase controls, and relay controls, to name a few.

An SCR (silicon-controlled rectifier) is a 4-layer *pnpn* device similar to the 4-layer diode except with three terminals: anode, cathode, and gate. The basic structure of an SCR is shown in Figure 11–7(a), and the schematic symbol is shown in Figure 11–7(b). Typical SCR packages are shown in Figure 11–7(c). Other types of thyristors are found in the same or similar packages.



(a) Basic construction

(b) Schematic symbol

(c) Typical packages

▲ FIGURE 11–7

The silicon-controlled rectifier (SCR).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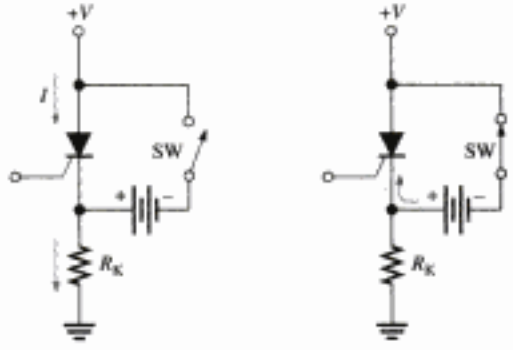
The **forced commutation** method basically requires momentarily forcing current through the SCR in the direction opposite to the forward conduction so that the net forward current is reduced below the holding value. The basic circuit, as shown in Figure 11–12, consists of a switch (normally a transistor switch) and a battery in parallel with the SCR. While the SCR is conducting, the switch is open, as shown in part (a). To turn off the SCR, the switch is closed, placing the battery across the SCR and forcing current through it opposite to the forward current, as shown in part (b). Typically, turn-off times for SCRs range from a few microseconds up to about 30 μs.

▶ **FIGURE 11–12**

SCR turn-off by forced commutation.



SCR Characteristics and Ratings

Several of the most important SCR characteristics and ratings are defined as follows. Use the curve in Figure 11–10(a) for reference where appropriate.

Forward-breakover voltage, $V_{BR(F)}$ This is the voltage at which the SCR enters the forward-conduction region. The value of $V_{BR(F)}$ is maximum when $I_G = 0$ and is designated $V_{BR(F0)}$. When the gate current in increased, $V_{BR(F)}$ decreases and is designated $V_{BR(F1)}$, $V_{BR(F2)}$, and so on, for increasing steps in gate current (I_{G1}, I_{G2}, and so on).

Holding current, I_H This is the value of anode current below which the SCR switches from the forward-conduction region to the forward-blocking region. The value increases with decreasing values of I_G and is maximum for $I_G = 0$.

Gate trigger current, I_{GT} This is the value of gate current necessary to switch the SCR from the forward-blocking region to the forward-conduction region under specified conditions.

Average forward current, $I_{F(avg)}$ This is the maximum continuous anode current (dc) that the device can withstand in the conduction state under specified conditions.

Forward-conduction region This region corresponds to the *on* condition of the SCR where there is forward current from anode to cathode through the very low resistance (approximate short) of the SCR.

Forward-blocking and reverse-blocking regions These regions correspond to the *off* condition of the SCR where the forward current from anode to cathode is blocked by the effective open circuit of the SCR.

Reverse-breakdown voltage, $V_{BR(R)}$ This parameter specifies the value of reverse voltage from cathode to anode at which the device breaks into the avalanche region and begins to conduct heavily (the same as in a *pn* junction diode).

SECTION 11–2 REVIEW

1. What is an SCR?
2. Name the SCR terminals.
3. How can an SCR be turned on (made to conduct)?
4. How can an SCR be turned off?

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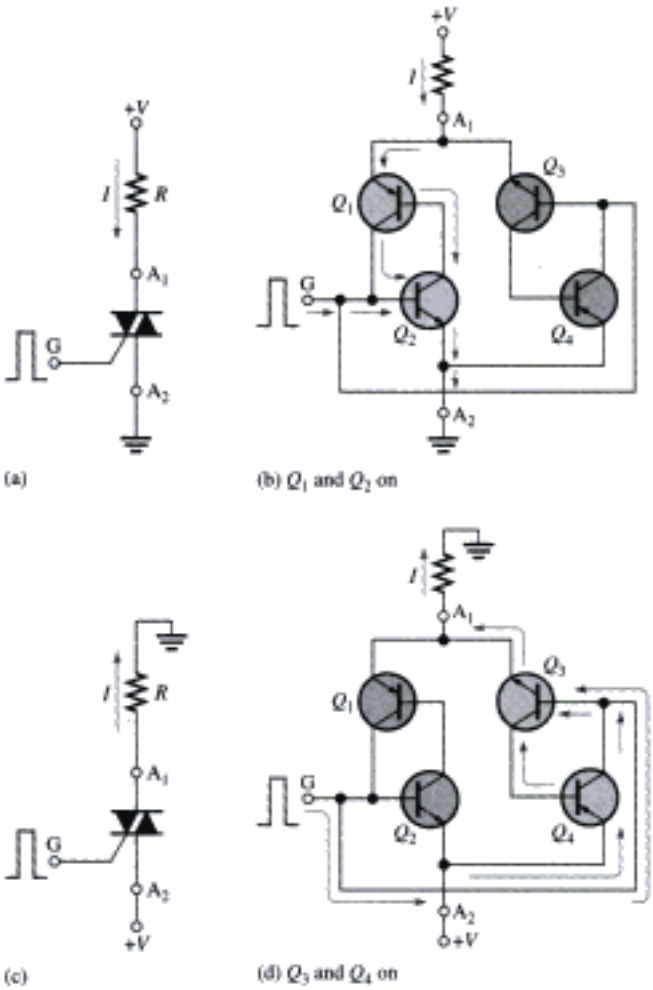
Figure 11–18 shows the triac being triggered into both directions of conduction. In part (a), terminal A_1 is biased positive with respect to A_2, so the triac conducts as shown when triggered by a positive pulse at the gate terminal. The transistor equivalent circuit in part (b) shows that Q_1 and Q_2 conduct when a positive trigger pulse is applied. In part (c), terminal A_2 is biased positive with respect to A_1, so the triac conducts as shown. In this case, Q_3 and Q_4 conduct as indicated in part (d) upon application of a positive trigger pulse.



◀ FIGURE 11–18

Bilateral operation of a triac.

SECTION 11–3 REVIEW

1. Compare the diac to the 4-layer diode in terms of basic operation.
2. Compare the triac with the SCR in terms of basic operation.
3. How does a triac differ from a diac?

11–4 THE SILICON-CONTROLLED SWITCH (SCS)

The silicon-controlled switch (SCS) is similar in construction to the SCR. The SCS, however, has two gate terminals, the cathode gate and the anode gate. The SCS can be turned on and off using either gate terminal. Remember that the SCR can be only turned on using its gate terminal. Normally, the SCS is available in power ratings lower than those of the SCR.

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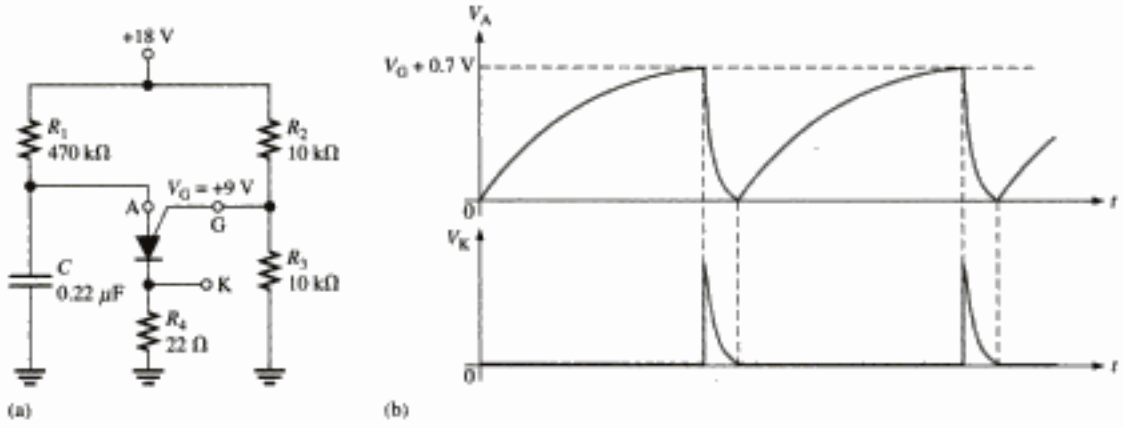


▲ FIGURE 11–30

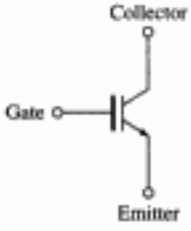
PUT relaxation oscillator.

SECTION 11–6 REVIEW

1. What does the term *programmable* mean as used in programmable unijunction transistor (PUT)?
2. Compare the structure and the operation of a PUT to those of other devices such as the UJT and SCR.

11–7 THE IGBT

The IGBT (insulated-gate bipolar transistor) combines features from both the MOSFET and the BJT that make it useful in high-voltage and high-current switching applications. The IGBT has largely replaced the MOSFET and the BJT in many of these applications.



▲ FIGURE 11–31

A symbol for the IGBT (insulated-gate bipolar transistor).

The **IGBT** is a device that has the output conduction characteristics of a BJT but is voltage controlled like a MOSFET; it is an excellent choice for many high-voltage switching applications. The IGBT has three terminals: gate, collector, and emitter. One common circuit symbol is shown in Figure 11–31. As you can see, it is similar to the BJT symbol except there is an extra bar representing the gate structure of a MOSFET rather than a base.

The IGBT has MOSFET input characteristics and BJT output characteristics. BJTs are capable of higher currents than FETs, but MOSFETs have no gate current because of the insulated gate structure. IGBTs exhibit a lower saturation voltage than MOSFETs and have about the same saturation voltage as BJTs. IGBTs are superior to MOSFETs in some applications because they can handle high collector-to-emitter voltages exceeding 200 V and exhibit less saturation voltage when they are in the *on* state. IGBTs are superior to BJTs in some applications because they can switch faster. In terms of switching speed, MOSFETs switch fastest, then IGBTs, followed by BJTs, which are slowest. A general comparison of IGBTs, MOSFETs, and BJTs is given in Table 11–1.

▶ TABLE 11–1

Comparison of several device features for switching applications.

FEATURES	IGBT	MOSFET	BJT
Type of input drive	Voltage	Voltage	Current
Input resistance	High	High	Low
Operating frequency	Medium	High	Low
Switching speed	Medium	Fast (ns)	Slow (μs)
Saturation voltage	Low	High	Low

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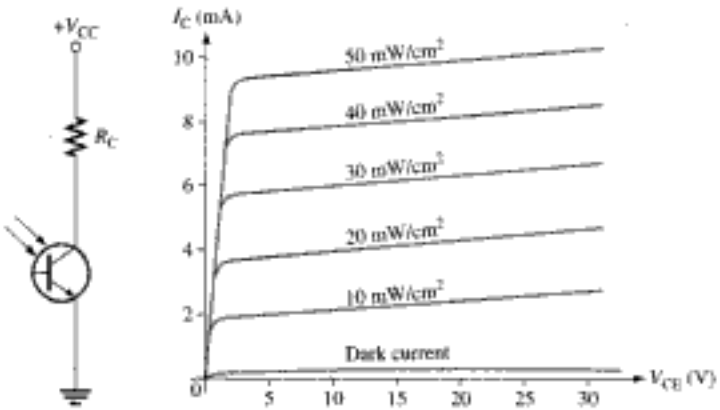
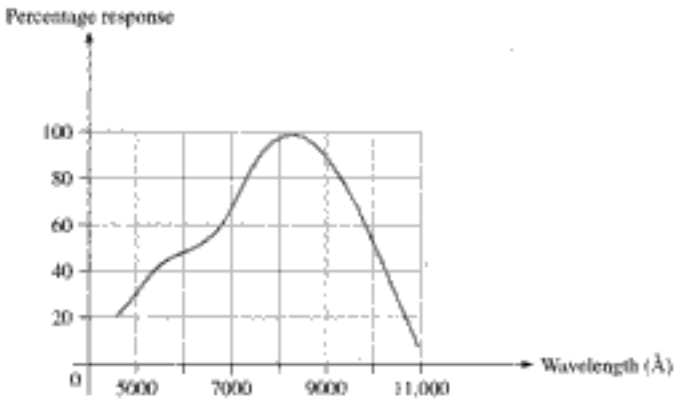


◀ **FIGURE 11–36**

Phototransistor bias circuit and typical collector characteristic curves.

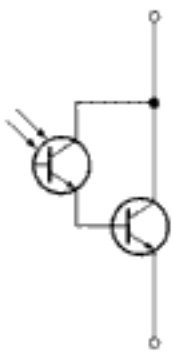


◀ **FIGURE 11–37**

Typical phototransistor spectral response.

Photodarlington

The photodarlington consists of a phototransistor connected in a darlington arrangement with a conventional BJT, as shown in Figure 11–38. Because of the higher current gain, this device has a much higher collector current and exhibits a greater light sensitivity than does a regular phototransistor.

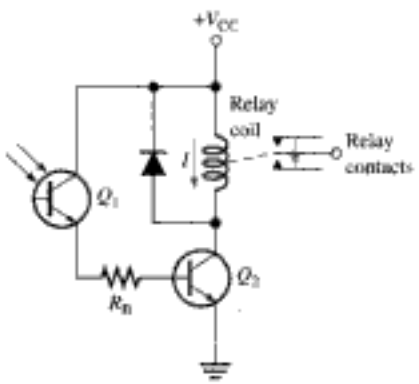


▲ **FIGURE 11–38**

Photodarlington.

Applications

Phototransistors are used in a wide variety of applications. A light-operated relay circuit is shown in Figure 11–39. The phototransistor Q_1 drives the BJT Q_2. When there is sufficient incident light on Q_1, transistor Q_2 is driven into saturation, and collector current through the relay coil energizes the relay. The diode across the relay coil prevents, by its limiting action, a large voltage transient from occurring at the collector of Q_2 when the transistor turns off.



◀ **FIGURE 11–39**

Light-operated relay circuit.

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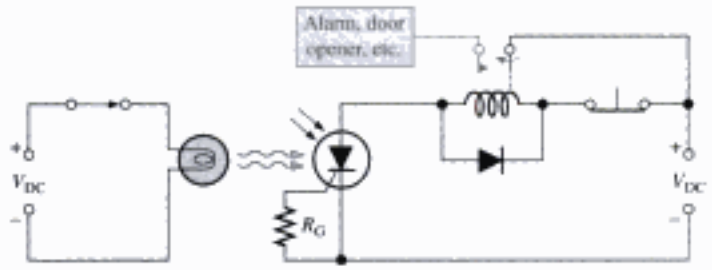
A **LASCR** (light-activated silicon-controlled rectifier) is a four-layer semiconductor device (thyristor) that conducts current in one direction when activated by a sufficient amount of light and continues to conduct until the current falls below a specified value. Figure 11–42 shows a LASCR schematic symbol and typical packages.

(a) Symbol (b) Typical packages

◄ FIGURE 11–42
LASCRs.

The LASCR is most sensitive to light when the gate terminal is open. If necessary, a resistor from the gate to the cathode can be used to reduce the sensitivity.

Figure 11–43 shows a LASCR used to energize a latching relay. The input source turns on the lamp; the resulting incident light triggers the LASCR. The anode current energizes the relay and closes the contact. Notice that the input source is electrically isolated from the rest of the circuit.



◄ FIGURE 11–43
A LASCR circuit.

SECTION 11–9 REVIEW

1. Can most LASCRs be operated as conventional SCRs?
2. What is required in Figure 11–54 to turn off the LASCR and de-energize the relay?

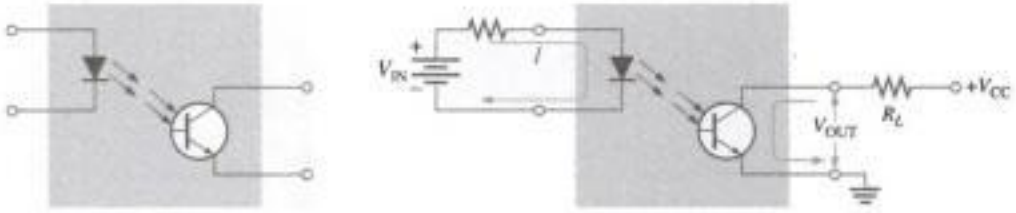
11–10 OPTICAL COUPLERS

Optical couplers use various optical devices such as LEDs and laser diodes. They are designed to provide complete electrical isolation between an input circuit and an output circuit. The usual purpose of isolation is to provide protection from high-voltage transients, surge voltage, or low-level noise that could possibly result in an erroneous output or damage to the device. Optical couplers also allow interfacing circuits with different voltage levels, different grounds, and so on. Optical diodes were covered in Chapter 3.

The input circuit of an optical coupler is typically an LED, but the output circuit can take several forms, such as the phototransistor shown in Figure 11–44(a). When the input voltage forward-biases the LED, light transmitted to the phototransistor turns it on, producing current through the external load, as shown in Figure 11–44(b). Typical optical couplers are shown in Figure 11–44(c).

Several other types of optical couplers are shown in Figure 11–45. The darlington transistor coupler in Figure 11–45(a) can be used when increased output current capability is needed beyond that provided by the phototransistor output. The disadvantage is that the photodarlington has a switching speed less than that of the phototransistor.

A LASCR output coupler is shown in Figure 11–45(b). This device can be used in applications where, for example, a low-level input voltage is required to latch a high-voltage relay for the purpose of activating some type of electromechanical device.

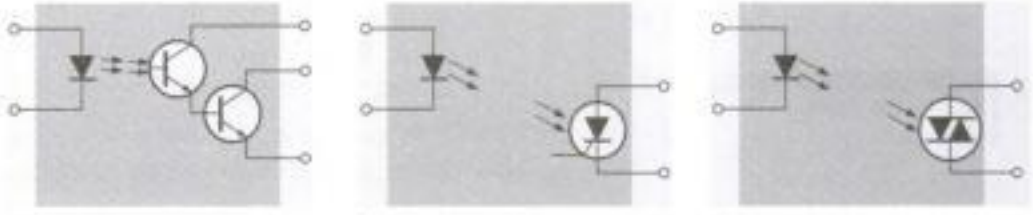


(a) Basic device (b) Device with external connections

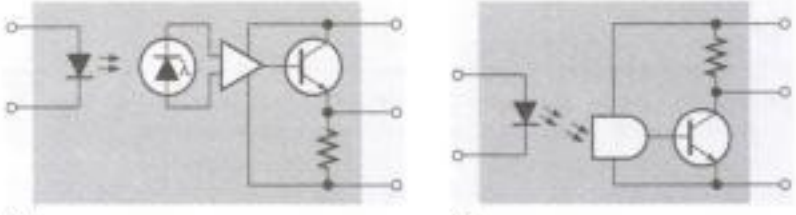
(c) Typical devices

▲ FIGURE 11–44

Optical couplers using phototransistors.



(a) (b) (c)



(d) (e)

▲ FIGURE 11–45

Common types of optical-coupling devices.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cladding so that it can move around bends in the fiber with essentially no loss. A fiber-optic cable consists of the core, which is the glass fiber itself, the cladding that surrounds the fiber and provides the reflective surface, and the outer coating or jacket that provides protection. Other layers may be added for strengthening. The basic structure of a single fiber-optic cable is illustrated in Figure 11–46(a), and the propagation of light along a fiber with a bend is shown in part (b). It doesn't matter whether the fiber is straight or bent; the light still travels through it.

► FIGURE 11–46

Simplified structure and operation of a fiber-optic cable.

(a) Basic construction (b) Propagation of a light ray

When a light ray enters the fiber-optic cable, it strikes the reflective surface of the cladding at an angle called the **angle of incidence**, θ_i. If the angle of incidence is greater than a parameter known as the **critical angle**, θ_c, the light ray is then reflected back into the core at an angle called the **angle of reflection**, as shown in Figure 11–47(a). The angle of incidence is always equal to the angle of reflection. If the angle of incidence is less than the critical angle, the light ray is refracted and passes into the cladding, causing energy to be lost, as shown in Figure 11–47(b). This is called *scattering*, and any refracted light represents a loss or attenuation as a light ray is propagated through the fiber-optic cable. Another cause of attenuation of light in a fiber-optic cable is called *absorption*, which is caused by the interactions of the light photons and the molecules of the core.

► FIGURE 11–47

Critical angle in a fiber-optic cable.

(a) Reflection of a light ray ($\theta_i > \theta_c$) (b) Refraction of a light ray ($\theta_i < \theta_c$)

The core material and the cladding material each have a parameter known as the **index of refraction**, which determines the critical angle. The critical angle is defined by the formula

Equation 11–4

$$\theta_c = \cos^{-1}\left(\frac{n_2}{n_1}\right)$$

where n_1 is the index of refraction of the core and n_2 is the index of refraction of the cladding.

EXAMPLE 11–5

A certain fiber-optic cable has a core index of refraction of 1.35 and a cladding index of refraction of 1.30. Determine the critical angle.

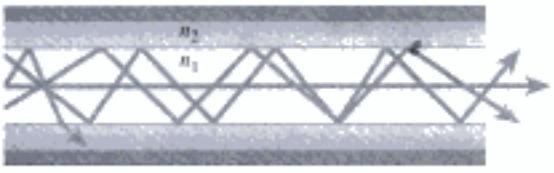
Solution

$$\theta_c = \cos^{-1}\left(\frac{n_2}{n_1}\right) = \cos^{-1}\left(\frac{1.30}{1.35}\right) = \mathbf{15.6°}$$

Modes of Light Propagation

Three basic modes of light propagation in fiber-optic cables are multimode step index, single-mode step index, and multimode graded index.

Multimode Step Index Figure 11–48 shows a fiber-optic cable in which the diameter of the core is fairly large relative to the diameter of the cladding. As shown, there is a sharp transition in the index of refraction going from the core to the cladding, thus the term *step*. Light entering the cable will tend to propagate through the core in multiple rays or modes, as indicated. Some of the rays will go straight down the core while others will bounce back and forth as they propagate. Still others will scatter due to their small angle of incidence, causing attenuation in the light energy. As a result of the multiple modes, the light will encounter time dispersion; that is, all the light rays will not arrive at the end of the cable at exactly the same time.



◀ FIGURE 11–48

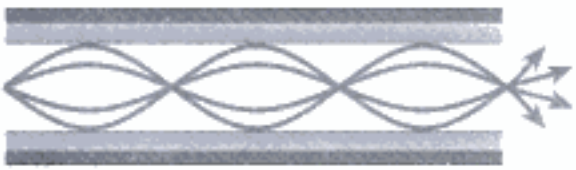
Multimode step index fiber-optic cable.

Single-Mode Step Index Figure 11–49 shows a fiber-optic cable in which the diameter core is very small relative to the diameter of the cladding. There is a sharp transition in the index of refraction going from the core to the cladding. Light entering the cable tends to propagate through the core in a single ray or mode. This results in much less attenuation and, ideally, no time dispersion compared to the multimode cable.

◀ FIGURE 11–49

Single-mode step index fiber-optic cable.

Multimode Graded Index Figure 11–50 shows a fiber-optic cable in which the diameter of the core is fairly large relative to the diameter of the cladding. There is a gradual or graded transition in the index of refraction going from the center of the core into the cladding. Light rays will be more curved as they bounce through the gradually changing indices of refraction resulting in less attenuation and time dispersion than in the multimode step index cable.



◀ FIGURE 11–50

Multimode graded index fiber-optic cable.

A Fiber-Optic Data Communications Link

A simplified block diagram of a fiber-optic data communications link is shown in Figure 11–51. The source provides the electrical signal that is to be transmitted. This electrical signal is converted to a light signal and coupled to the fiber-optic cable by the transmitter. At the receiving end, the light signal is coupled out of the cable into the receiver, which converts it to an electrical signal. This signal is then processed and connected to the end user.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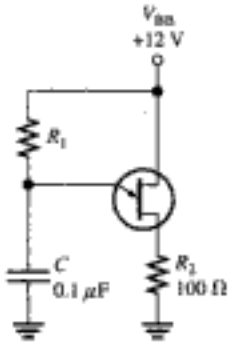
SECTION 11–4 The Silicon-Controlled Switch (SCS)

7. Explain the turn-on and turn-off operation of an SCS in terms of its transistor equivalent.
8. Name the terminals of an SCS.

SECTION 11–5 The Unijunction Transistor (UJT)

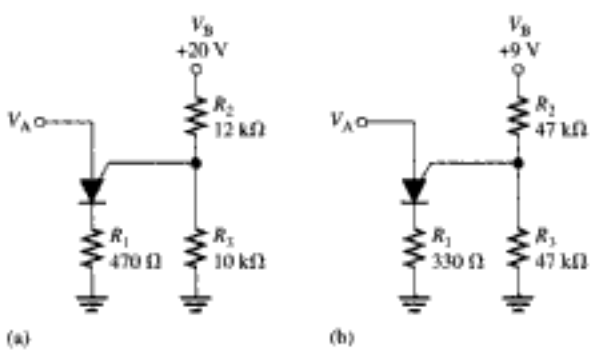
9. In a certain UJT, $r'_{B1} = 2.5\ \text{k}\Omega$ and $r'_{B2} = 4\ \text{k}\Omega$. What is the intrinsic standoff ratio?
10. Determine the peak-point voltage for the UJT in Problem 12 if $V_{BB} = 15$ V.
11. Find the range of values of R_1 in Figure 11–57 that will ensure proper turn-on and turn-off of the UJT. $\eta = 0.68$, $V_v = 0.8$ V, $I_V = 15$ mA, $I_P = 10\ \mu\text{A}$, and $V_P = 10$ V.

► FIGURE 11–57

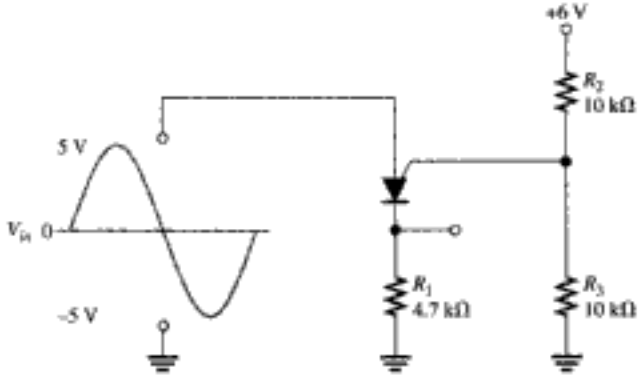


SECTION 11–6 The Programmable Unijunction Transistor (PUT)

12. At what anode voltage (V_A) will each PUT in Figure 11–58 begin to conduct?
13. Draw the current waveform for each circuit in Figure 11–58 when there is a 10 V peak sinusoidal voltage at the anode. Neglect the forward voltage of the PUT.
14. Sketch the voltage waveform across R_1 in Figure 11–59 in relation to the input voltage waveform.



▲ FIGURE 11–58



▲ FIGURE 11–59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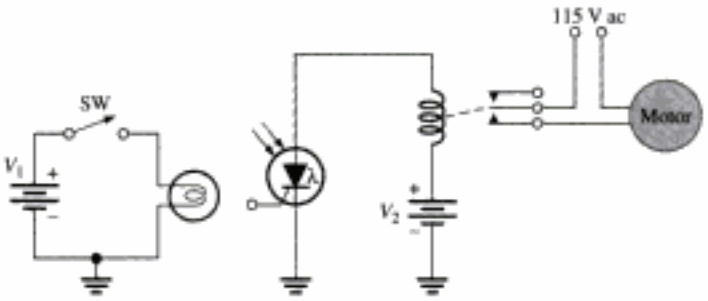
▶ FIGURE 11–62

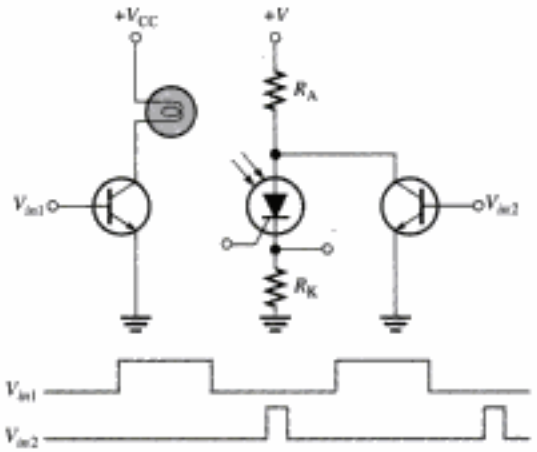


SECTION 11–10 Optical Couplers

22. A particular optical coupler has a current transfer ratio of 30 percent. If the input current is 100 mA, what is the output current?

23. The optical coupler shown in Figure 11–64 is required to deliver at least 10 mA to the external load. If the current transfer ratio is 60 percent, how much current must be supplied to the input?

▶ FIGURE 11–63

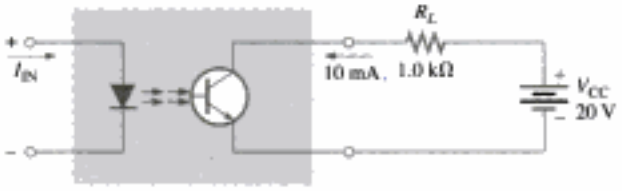


SECTION 11–11 Fiber Optics

24. A light ray strikes the core of a fiber-optic cable at 30° angle of incidence. If the critical angle of the core is 15°, will the light ray be reflected or refracted?

25. Determine the critical angle of a fiber-optic cable if the core has an index of refraction of 1.55 and the cladding has an index of refraction of 1.25.

▶ FIGURE 11–64



ANSWERS

SECTION REVIEWS

SECTION 11–1 The Basic 4-Layer Device

1. The 4-layer diode is a thyristor because it has four semiconductor layers in a *pnpn* configuration.

2. A region of 4-layer diode operation in which the device is nonconducting

3. The device turns on and conducts when V_{AK} exceeds the forward-breakover voltage.
4. When the anode current is reduced below the holding current value, the device turns off.

SECTION 11–2 The Silicon-Controlled Rectifier (SCR)

1. An SCR (silicon-controlled rectifier) is a three-terminal thyristor.
2. The SCR terminals are anode, cathode, and gate.
3. A positive gate pulse turns the SCR on.
4. Reduce the anode current below I_H (holding current) to turn a conducting SCR off.

SECTION 11–3 The Diac and Triac

1. The diac is like two parallel 4-layer diodes connected in opposite directions.
2. A triac is like two parallel SCRs having a common gate and connected in opposite directions.
3. A triac has a gate terminal, but a diac does not.

SECTION 11–4 The Silicon-Controlled Switch (SCS)

1. An SCS can be turned off with the application of a gate pulse, but an SCR cannot.
2. A positive pulse on the cathode gate or a negative pulse on the anode gate turns the SCS on.
3. An SCS can be turned off by any of the following:
   (a) positive pulse on anode gate
   (b) negative pulse on cathode gate
   (c) reduce anode current below holding value
   (d) completely interrupt anode current

SECTION 11–5 The Unijunction Transistor (UJT)

1. The UJT terminals are base 1, base 2, and emitter.
2. $\eta = r'_{B1}/r'_{BB}$
3. R, C, and η determine the period.

SECTION 11–6 The Programmable Unijunction Transistor (PUT)

1. *Programmable* means that the turn-on voltage can be adjusted to a desired value.
2. The PUT is a thyristor, similar in structure to an SCR, but it is turned on by the anode-to-gate voltage. It has a negative resistance characteristic like the UJT.

SECTION 11–7 The IGBT

1. IGBT stands for insulated-gate bipolar transistor.
2. High-voltage switching applications
3. The IGBT has a lower output saturation voltage than the MOSFET.
4. The IGBT has a very high input resistance compared to a BJT.
5. Latch-up is a condition in which the IGBT is in the *on* state and cannot be turned off by the gate voltage.

SECTION 11–8 The Phototransistor

1. The base current of a phototransistor is light induced.
2. Base
3. The collector current depends on β_{DC} and I_λ.

SECTION 11–9 The Light-Activated SCR (LASCR)

1. Most LASCRs can be operated as conventional SCRs.
2. A series switch to shut off the anode current is required.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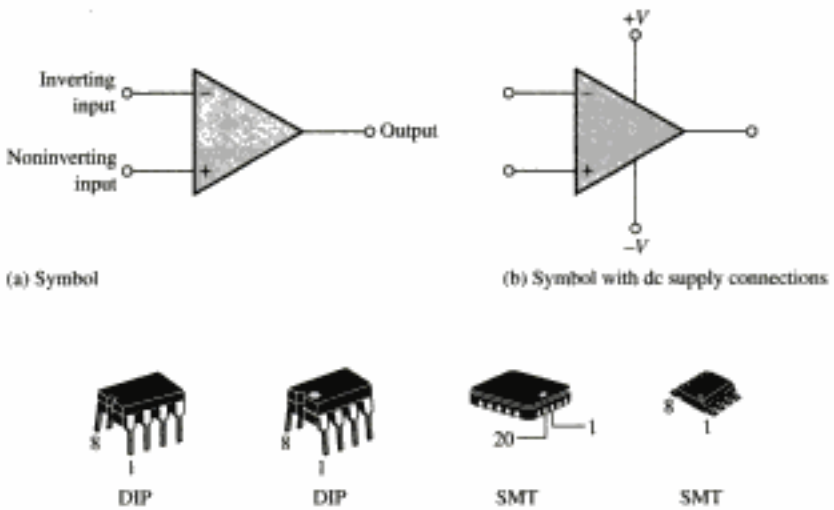
12–1 INTRODUCTION TO OPERATIONAL AMPLIFIERS

Early operational amplifiers (op-amps) were used primarily to perform mathematical operations such as addition, subtraction, integration, and differentiation—thus the term *operational*. These early devices were constructed with vacuum tubes and worked with high voltages. Today's op-amps are linear integrated circuits (ICs) that use relatively low dc supply voltages and are reliable and inexpensive.

Symbol and Terminals

The standard **operational amplifier (op-amp)** symbol is shown in Figure 12–1(a). It has two input terminals, the inverting (−) input and the noninverting (+) input, and one output terminal. The typical op-amp operates with two dc supply voltages, one positive and the other negative, as shown in Figure 12–1(b). Usually these dc voltage terminals are left off the schematic symbol for simplicity but are understood to be there. Some typical op-amp IC packages are shown in Figure 12–1(c).

► **FIGURE 12–1**
Op-amp symbols and packages.



(a) Symbol

(b) Symbol with dc supply connections

(c) Typical packages. Pin 1 is indicated by a notch or dot on dual in-line (DIP) and surface-mount technology (SMT) packages, as shown.

The Ideal Op-Amp

To illustrate what an op-amp is, let's consider its ideal characteristics. A practical op-amp, of course, falls short of these ideal standards, but it is much easier to understand and analyze the device from an ideal point of view.

First, the ideal op-amp has *infinite voltage gain* and *infinite bandwidth*. Also, it has an *infinite input impedance* (open) so that it does not load the driving source. Finally, it has a *zero output impedance*. These characteristics are illustrated in Figure 12–2(a). The input voltage, V_{in}, appears between the two input terminals, and the output voltage is $A_v V_{in}$, as indicated by the internal voltage source symbol. The concept of infinite input impedance is a particularly valuable analysis tool for the various op-amp configurations, which will be discussed in Section 12–4.

The Practical Op-Amp

Although **integrated circuit (IC)** op-amps approach parameter values that can be treated as ideal in many cases, the ideal device can never be made. Any device has limitations, and the IC op-amp is no exception. Op-amps have both voltage and current limitations. Peak-to-peak output voltage, for example, is usually limited to slightly less than the two supply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A CMRR of 100,000, for example, means that the desired input signal (differential) is amplified 100,000 times more than the unwanted noise (common-mode). If the amplitudes of the differential input signal and the common-mode noise are equal, the desired signal will appear on the output 100,000 times greater in amplitude than the noise. Thus, the noise or interference has been essentially eliminated.

Common-Mode Input Voltage Range

All op-amps have limitations on the range of voltages over which they will operate. The *common-mode input voltage range* is the range of input voltages which, when applied to both inputs, will not cause clipping or other output distortion. Many op-amps have common-mode input voltage ranges of ±10 V with dc supply voltages of ±15 V.

Input Offset Voltage

The ideal op-amp produces zero volts out for zero volts in. In a practical op-amp, however, a small dc voltage, $V_{OUT(error)}$, appears at the output when no differential input voltage is applied. Its primary cause is a slight mismatch of the base-emitter voltages of the differential amplifier input stage of an op-amp.

As specified on an op-amp data sheet, the *input offset voltage*, V_{OS}, is the differential dc voltage required between the inputs to force the output to zero volts. Typical values of input offset voltage are in the range of 2 mV or less. In the ideal case, it is 0 V.

The *input offset voltage drift* is a parameter related to V_{OS} that specifies how much change occurs in the input offset voltage for each degree change in temperature. Typical values range anywhere from about 5 μV per degree centigrade to about 50 μV per degree centigrade. Usually, an op-amp with a higher nominal value of input offset voltage exhibits a higher drift.

Input Bias Current

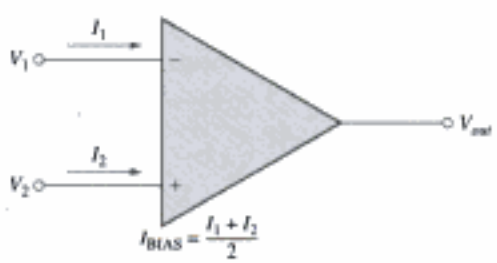
The input terminals of a bipolar differential amplifier are the transistor bases and, therefore, the input currents are the base currents.

The *input bias current* is the dc current required by the inputs of the amplifier to properly operate the first stage. By definition, the input bias current is the *average* of both input currents and is calculated as follows:

$$I_{BIAS} = \frac{I_1 + I_2}{2}$$

Equation 12–3

The concept of input bias current is illustrated in Figure 12–9.



◀ FIGURE 12–9

Input bias current is the average of the two op-amp input currents.

Input Impedance

Two basic ways of specifying the input impedance of an op-amp are the differential and the common mode. The *differential input impedance* is the total resistance between the inverting and the noninverting inputs, as illustrated in Figure 12–10(a). Differential impedance is measured by determining the change in bias current for a given change in differential input voltage. The *common-mode input impedance* is the resistance between each input and ground and is measured by determining the change in bias current for a given change in common-mode input voltage. It is depicted in Figure 12–10(b).

▶ FIGURE 12–10

Op-amp input impedance.

(a) Differential input impedance (b) Common-mode input impedance

Input Offset Current

Ideally, the two input bias currents are equal, and thus their difference is zero. In a practical op-amp, however, the bias currents are not exactly equal.

The *input offset current*, I_{OS}, is the difference of the input bias currents, expressed as an absolute value.

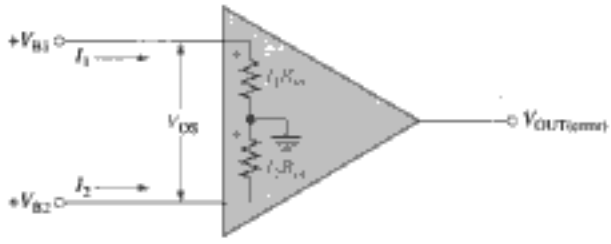
Equation 12–4

$$I_{OS} = |I_1 - I_2|$$

Actual magnitudes of offset current are usually at least an order of magnitude (ten times) less than the bias current. In many applications, the offset current can be neglected. However, high-gain, high-input impedance amplifiers should have as little I_{OS} as possible because the difference in currents through large input resistances develops a substantial offset voltage, as shown in Figure 12–11.

▶ FIGURE 12–11

Effect of input offset current.



The offset voltage developed by the input offset current is

$$V_{OS} = I_1 R_{in} - I_2 R_{in} = (I_1 - I_2) R_{in}$$

Equation 12–5

$$V_{OS} = I_{OS} R_{in}$$

The error created by I_{OS} is amplified by the gain A_v of the op-amp and appears in the output as

Equation 12–6

$$V_{OUT(error)} = A_v I_{OS} R_{in}$$

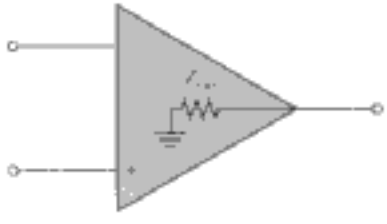
A change in offset current with temperature affects the error voltage. Values of temperature coefficient for the offset current in the range of 0.5 nA per degree centigrade are common.

Output Impedance

The *output impedance* is the resistance viewed from the output terminal of the op-amp, as indicated in Figure 12–12.

▶ FIGURE 12–12

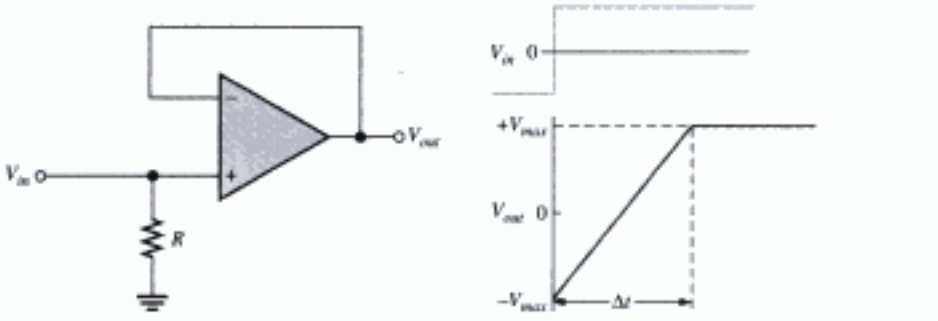
Op-amp output impedance.



Slew Rate

The maximum rate of change of the output voltage in response to a step input voltage is the **slew rate** of an op-amp. The slew rate is dependent upon the high-frequency response of the amplifier stages within the op-amp.

Slew rate is measured with an op-amp connected as shown in Figure 12–13(a). This particular op-amp connection is a unity-gain, noninverting configuration that will be discussed in Section 12–4. It gives a worst-case (slowest) slew rate. Recall that the high-frequency components of a voltage step are contained in the rising edge and that the upper critical frequency of an amplifier limits its response to a step input. For a step input, the slope on the output is inversely proportional to the upper critical frequency. Slope increases as upper critical frequency decreases.



(a) Test circuit

(b) Step input voltage and the resulting output voltage

◀ **FIGURE 12–13**
Slew-rate measurement.

A pulse is applied to the input and the resulting ideal output voltage is indicated in Figure 12–13(b). The width of the input pulse must be sufficient to allow the output to "slew" from its lower limit to its upper limit. A certain time interval, Δt, is required for the output voltage to go from its lower limit $-V_{max}$ to its upper limit $+V_{max}$, once the input step is applied. The slew rate is expressed as

$$\text{Slew rate} = \frac{\Delta V_{out}}{\Delta t}$$

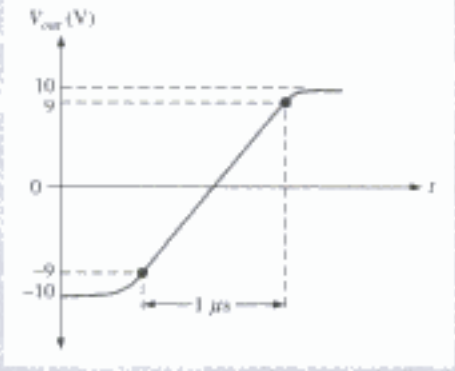
Equation 12–7

where $\Delta V_{out} = +V_{max} - (-V_{max})$. The unit of slew rate is volts per microsecond (V/μs).

EXAMPLE 12–2

The output voltage of a certain op-amp appears as shown in Figure 12–14 in response to a step input. Determine the slew rate.

▶ **FIGURE 12–14**

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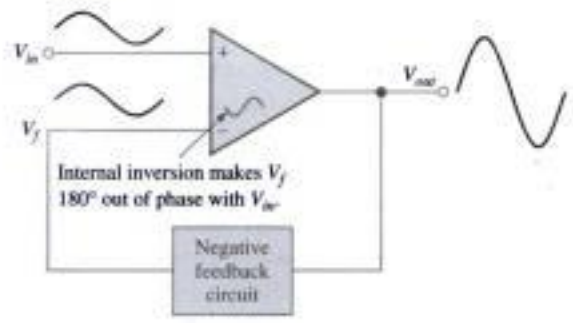
SECTION 12–2 REVIEW

1. Distinguish between differential and single-ended inputs.
2. Define *common-mode rejection*.
3. For a given value of open-loop gain, does a higher CMRR result in a higher or lower common-mode gain?
4. List at least ten op-amp parameters.
5. Which two parameters, not including the frequency response, are frequency dependent?

12–3 NEGATIVE FEEDBACK

Negative feedback is one of the most useful concepts in electronics, particularly in op-amp applications. **Negative feedback** is the process whereby a portion of the output voltage of an amplifier is returned to the input with a phase angle that opposes (or subtracts from) the input signal.

Negative feedback is illustrated in Figure 12–15. The inverting (−) input effectively makes the feedback signal 180° out of phase with the input signal.



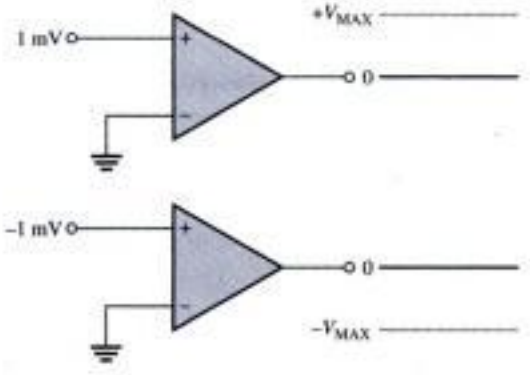
◄ FIGURE 12–15
Illustration of negative feedback.

Why Use Negative Feedback?

As you have seen, the inherent open-loop voltage gain of a typical op-amp is very high (usually greater than 100,000). Therefore, an extremely small input voltage drives the op-amp into its saturated output states. In fact, even the input offset voltage of the op-amp can drive it into saturation. For example, assume $V_{IN} = 1$ mV and $A_{ol} = 100{,}000$. Then,

$$V_{IN}A_{ol} = (1\text{ mV})(100{,}000) = 100\text{ V}$$

Since the output level of an op-amp can never reach 100 V, it is driven deep into saturation and the output is limited to its maximum output levels, as illustrated in Figure 12–16 for both a positive and a negative input voltage of 1 mV.



◄ FIGURE 12–16
Without negative feedback, a small input voltage drives the op-amp to its output limits and it becomes nonlinear.

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Since the output impedance of the noninverting amplifier configuration is $Z_{out(NI)} = V_{out}/I_{out}$, you can substitute $I_{out}Z_{out(NI)}$ for V_{out}; therefore,

$$A_{cl}V_{in} = (1 + A_{ol}B)I_{out}Z_{out(NI)}$$

Dividing both sides of the above expression by I_{out},

$$\frac{A_{cl}V_{in}}{I_{out}} = (1 + A_{ol}B)Z_{out(NI)}$$

The term on the left is the internal output impedance of the op-amp (Z_{out}) because, without feedback, $A_{cl}V_{in} = V_{out}$. Therefore,

$$Z_{out} = (1 + A_{ol}B)Z_{out(NI)}$$

Thus,

Equation 12–12

$$Z_{out(NI)} = \frac{Z_{out}}{1 + A_{ol}B}$$

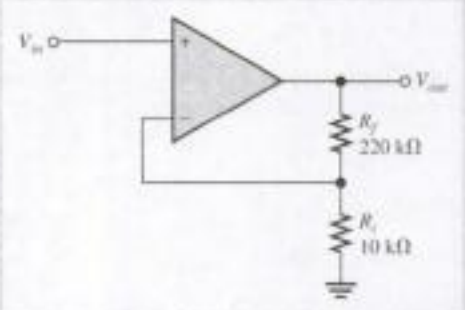
This equation shows that the output impedance of the noninverting amplifier configuration with negative feedback is much less than the internal output impedance, Z_{out}, of the op-amp itself (without feedback) because Z_{out} is divided by the factor $1 + A_{ol}B$.

EXAMPLE 12–5

(a) Determine the input and output impedances of the amplifier in Figure 12–26. The op-amp data sheet gives $Z_{in} = 2\ \text{M}\Omega$, $Z_{out} = 75\ \Omega$, and $A_{ol} = 200{,}000$.

(b) Find the closed-loop voltage gain.

► **FIGURE 12–26**



Solution (a) The attenuation, B, of the feedback circuit is

$$B = \frac{R_i}{R_i + R_f} = \frac{10\ \text{k}\Omega}{230\ \text{k}\Omega} = 0.0435$$

$$Z_{in(NI)} = (1 + A_{ol}B)Z_{in} = [1 + (200{,}000)(0.0435)](2\ \text{M}\Omega)$$

$$= (1 + 8700)(2\ \text{M}\Omega) = \mathbf{17.4\ G\Omega}$$

$$Z_{out(NI)} = \frac{Z_{out}}{1 + A_{ol}B} = \frac{75\ \Omega}{1 + 8700} = \mathbf{8.6\ m\Omega}$$

(b) $$A_{cl(NI)} = 1 + \frac{R_f}{R_i} = 1 + \frac{220\ \text{k}\Omega}{10\ \text{k}\Omega} = \mathbf{23.0}$$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Output Impedance As with a noninverting amplifier, the output impedance of an inverting amplifier is decreased by the negative feedback. In fact, the expression is the same as for the noninverting case.

Equation 12–16

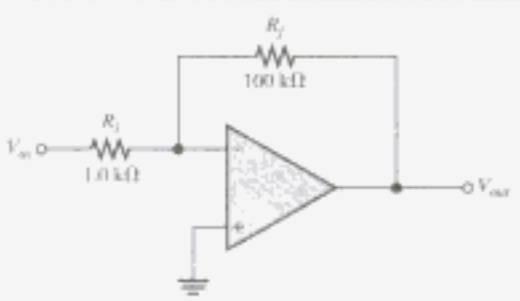
$$Z_{out(f)} = \frac{Z_{out}}{1 + A_{vd}B}$$

The output impedance of both the noninverting and the inverting amplifier configurations is very low; in fact, it is almost zero in practical cases. Because of this near zero output impedance, any load impedance connected to the op-amp output can vary greatly and not change the output voltage at all.

EXAMPLE 12–7

Find the values of the input and output impedances in Figure 12–29. Also, determine the closed-loop voltage gain. The op-amp has the following parameters: $A_{vd} = 50{,}000$; $Z_{in} = 4\ \text{M}\Omega$; and $Z_{out} = 50\ \Omega$.

► **FIGURE 12–29**



Solution

$$Z_{in(f)} = R_i = \mathbf{1.0\ k\Omega}$$

The feedback attenuation, B, is

$$B = \frac{R_i}{R_i + R_f} = \frac{1.0\ \text{k}\Omega}{101\ \text{k}\Omega} = 0.001$$

Then

$$Z_{out(f)} = \frac{Z_{out}}{1 + A_{vd}B} = \frac{50\ \Omega}{1 + (50{,}000)(0.001)}$$
$$= \mathbf{980\ m\Omega}\ \text{(zero for all practical purposes)}$$

The closed-loop voltage gain is

$$A_{v(f)} = -\frac{R_f}{R_i} = -\frac{100\ \text{k}\Omega}{1.0\ \text{k}\Omega} = \mathbf{-100}$$

SECTION 12–5 REVIEW

1. How does the input impedance of a noninverting amplifier configuration compare to the input impedance of the op-amp itself?
2. When an op-amp is connected in a voltage-follower configuration, does the input impedance increase or decrease?
3. Given that $R_f = 100\ \text{k}\Omega$; $R_i = 2\ \text{k}\Omega$; $A_{vd} = 120{,}000$; $Z_{in} = 2\ \text{M}\Omega$; and $Z_{out} = 60\ \Omega$, what are $Z_{in(f)}$ and $Z_{out(f)}$ for an inverting amplifier configuration?

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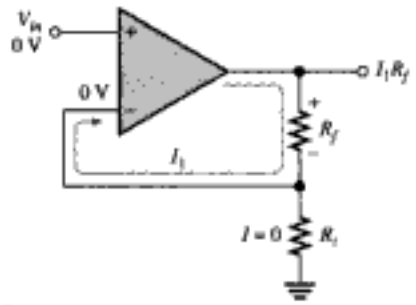
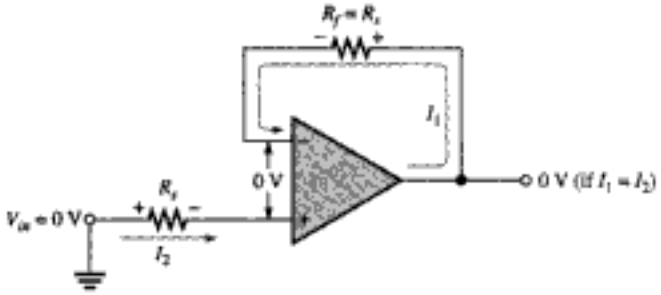
▶ **FIGURE 12–32**

Input bias current creates output error voltage in noninverting amplifier.



▶ **FIGURE 12–33**

Bias current compensation in a voltage-follower.



output error voltage. If $I_1 = I_2$, then the output voltage is zero. Usually I_1 does not quite equal I_2; but even in this case, the output error voltage is reduced as follows because I_{OS} is less than I_2.

$$V_{OUT(error)} = |I_1 - I_2| R_s \approx I_{OS} R_s$$

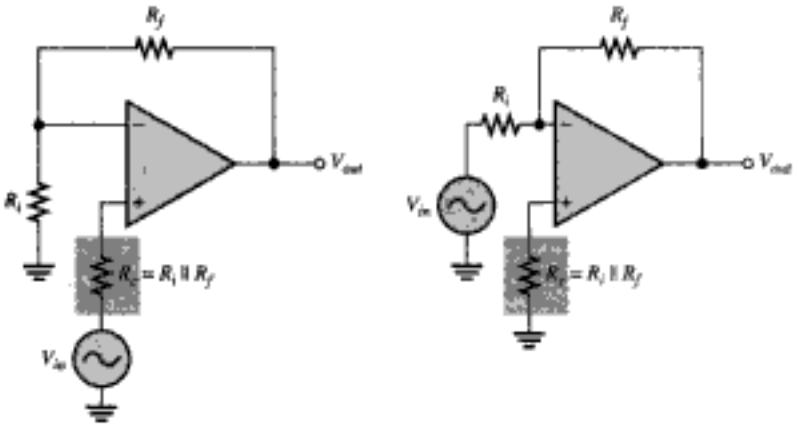
where I_{OS} is the input offset current.

Bias Current Compensation in Other Op-Amp Configurations

To compensate for the effect of bias current in the noninverting amplifier, a resistor R_c is added, as shown in Figure 12–34(a). The compensating resistor value equals the parallel combination of R_i and R_f. The input current creates a voltage drop across R_c that offsets the voltage across the combination of R_i and R_f, thus sufficiently reducing the output error voltage. The inverting amplifier is similarly compensated, as shown in Figure 12–34(b).

▶ **FIGURE 12–34**

Bias current compensation in the noninverting and inverting amplifier configurations.



(a) Noninverting amplifier (b) Inverting amplifier

Effect of Input Offset Voltage

The output voltage of an op-amp should be zero when the differential input is zero. However, there is always a small output error voltage present whose value typically ranges from microvolts to millivolts. This is due to unavoidable imbalances within the internal op-amp transistors aside from the bias currents. In a negative feedback configuration, the input offset voltage V_{IO} can be visualized as an equivalent small dc voltage source, as illustrated in Figure 12–35 for a voltage-follower. Generally, the output error voltage due to the input offset voltage is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If an op-amp is represented by a voltage gain element with a gain of $A_{ol(mid)}$ plus a single *RC* lag circuit, as shown in Figure 12–40, then the total open-loop gain of the op-amp is the product of the midrange open-loop gain, $A_{ol(mid)}$, and the attenuation of the *RC* circuit.

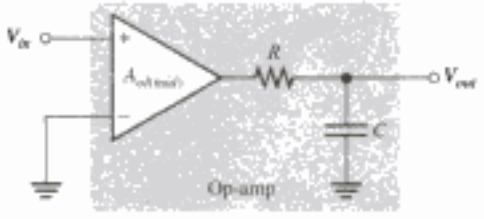
Equation 12–19

$$A_{ol} = \frac{A_{ol(mid)}}{\sqrt{1 + f^2/f_c^2}}$$

As you can see from Equation 12–19, the open-loop gain equals the midrange gain when the signal frequency f is much less than the critical frequency f_c and drops off as the frequency increases. Since f_c is part of the open-loop response of an op-amp, we will refer to it as $f_{c(ol)}$.

▶ FIGURE 12–40

Op-amp represented by a gain element and an internal *RC* circuit.



The following example demonstrates how the open-loop gain decreases as the frequency increases above $f_{c(ol)}$.

EXAMPLE 12–8

Determine A_{ol} for the following values of f. Assume $f_{c(ol)} = 100$ Hz and $A_{ol(mid)} = 100{,}000$.

(a) $f = 0$ Hz **(b)** $f = 10$ Hz **(c)** $f = 100$ Hz **(d)** $f = 1000$ Hz

Solution

(a) $A_{ol} = \dfrac{A_{ol(mid)}}{\sqrt{1 + f^2/f_{c(ol)}^2}} = \dfrac{100{,}000}{\sqrt{1 + 0}} = \mathbf{100{,}000}$

(b) $A_{ol} = \dfrac{100{,}000}{\sqrt{1 + (0.1)^2}} = \mathbf{99{,}503}$

(c) $A_{ol} = \dfrac{100{,}000}{\sqrt{1 + (1)^2}} = \dfrac{100{,}000}{\sqrt{2}} = \mathbf{70{,}710}$

(d) $A_{ol} = \dfrac{100{,}000}{\sqrt{1 + (10)^2}} = \mathbf{9950}$

Phase Shift

An *RC* circuit causes a propagation delay from input to output, thus creating a **phase shift** between the input signal and the output signal. An *RC* lag circuit such as found in an op-amp stage causes the output signal voltage to lag the input, as shown in Figure 12–41. From basic ac circuit theory, the phase shift, θ, is

$$\theta = -\tan^{-1}\left(\frac{R}{X_C}\right)$$

Since $R/X_C = f/f_c$,

Equation 12–20

$$\theta = -\tan^{-1}\left(\frac{f}{f_c}\right)$$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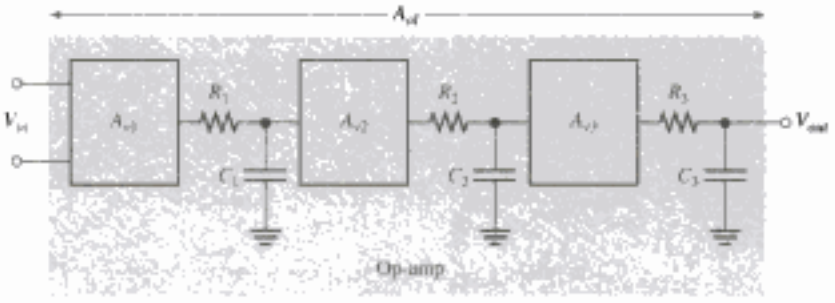
Complete Frequency Response

Previously, an op-amp was assumed to have a constant roll-off of −20 dB/decade above its critical frequency. For most op-amps this is the case; for some, however, the situation is more complex. The more complex IC operational amplifier may consist of two or more cascaded amplifier stages. The gain of each stage is frequency dependent and rolls off at −20 dB/decade above its critical frequency. Therefore, the total response of an op-amp is a composite of the individual responses of the internal stages. As an example, a three-stage op-amp is represented in Figure 12–43(a), and the frequency response of each stage is shown in Figure 12–43(b). As you know, dB gains are added so that the total op-amp frequency response is as shown in Figure 12–43(c). Since the roll-off rates are additive, the total roll-off rate increases by −20 dB/decade (−6 dB/octave) as each critical frequency is reached.

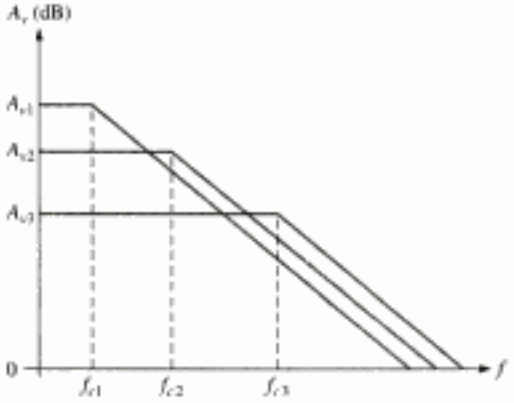
Complete Phase Response

In a multistage amplifier, each stage contributes to the total phase lag. As you have seen, each *RC* lag circuit can produce up to a −90° phase shift. Since each stage in an op-amp includes an *RC* lag circuit, a three-stage op-amp, for example, can have a maximum phase lag of −270°. Also, the phase lag of each stage is less than −45° when the frequency is below the critical frequency, equal to −45° at the critical frequency, and greater than −45° when the frequency is above the critical frequency. The phase lags of the stages of an op-amp are added to produce a total phase lag, according to the following formula for three stages:

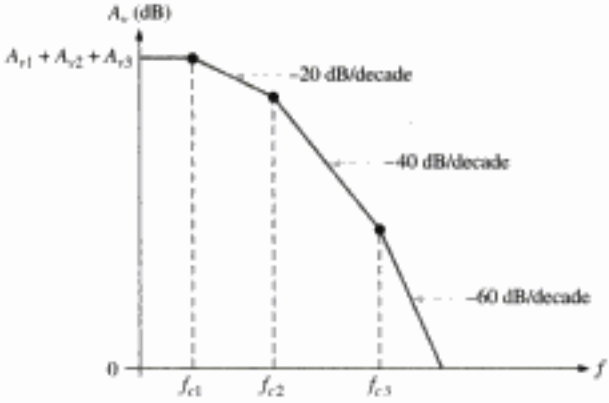
$$\theta_{tot} = -\tan^{-1}\left(\frac{f}{f_{c1}}\right) - \tan^{-1}\left(\frac{f}{f_{c2}}\right) - \tan^{-1}\left(\frac{f}{f_{c3}}\right)$$



(a) Representation of an op-amp with three internal stages



(b) Individual responses



(c) Composite response

▲ FIGURE 12–43

Op-amp open-loop frequency response.

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Effect of Negative Feedback on Bandwidth

You know how negative feedback affects the gain; now you will learn how it affects the amplifier's bandwidth. The closed-loop critical frequency of an op-amp is

Equation 12–21

$$f_{c(cl)} = f_{c(ol)}(1 + BA_{ol(mid)})$$

This expression shows that the closed-loop critical frequency, $f_{c(cl)}$, is higher than the open-loop critical frequency $f_{c(ol)}$ by the factor $1 + BA_{ol(mid)}$.

Since $f_{c(cl)}$ equals the bandwidth for the closed-loop amplifier, the closed-loop bandwidth (BW_{cl}) is also increased by the same factor.

Equation 12–22

$$BW_{cl} = BW_{ol}(1 + BA_{ol(mid)})$$

EXAMPLE 12–11

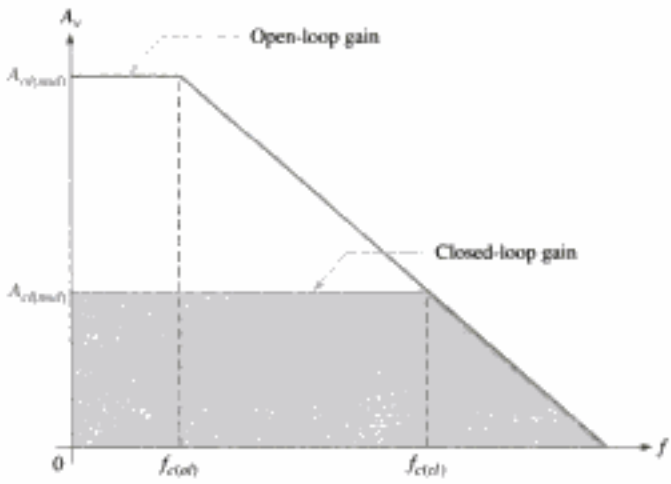
A certain amplifier has an open-loop midrange gain of 150,000 and an open-loop 3 dB bandwidth of 200 Hz. The attenuation of the feedback loop is 0.002. What is the closed-loop bandwidth?

Solution $BW_{cl} = BW_{ol}(1 + BA_{ol(mid)}) = 200\text{ Hz}[1 + (0.002)(150{,}000)] = \mathbf{60.2\text{ kHz}}$

Figure 12–44 graphically illustrates the concept of closed-loop response. When the open-loop gain of an op-amp is reduced by negative feedback, the bandwidth is increased. The closed-loop gain is independent of the open-loop gain up to the point of intersection of the two gain curves. This point of intersection is the critical frequency, $f_{c(cl)}$, for the closed-loop response. Notice that the closed-loop gain has the same roll-off rate as the open-loop gain, beyond the closed-loop critical frequency.

▶ **FIGURE 12–44**

Closed-loop gain compared to open-loop gain.



Gain-Bandwidth Product

An increase in closed-loop gain causes a decrease in the bandwidth and vice versa, such that the product of gain and bandwidth is a constant. This is true as long as the roll-off rate is fixed. If you let A_{cl} represent the gain of any of the closed-loop configurations and $f_{c(cl)}$ represent the closed-loop critical frequency (same as the bandwidth), then

$$A_{cl}f_{c(cl)} = A_{ol}f_{c(ol)}$$

The **gain-bandwidth product** is always equal to the frequency at which the op-amp's open-loop gain is unity or 0 dB (unity-gain bandwidth).

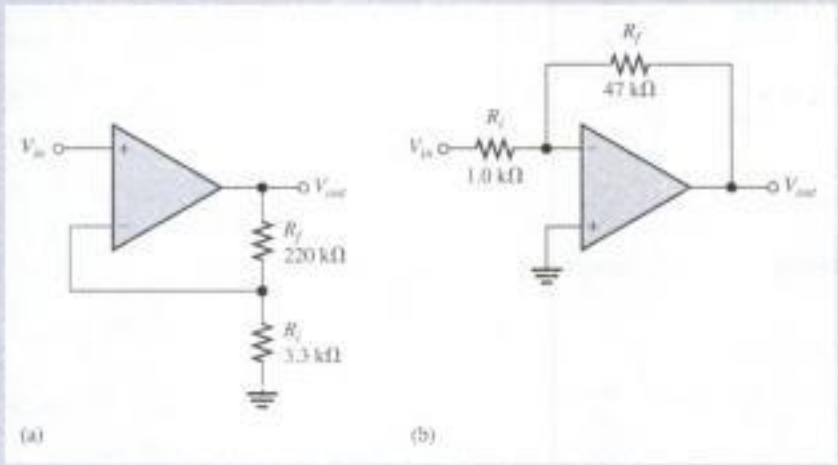
Equation 12–23

$$\text{Unity-gain bandwidth} = A_{cl}f_{c(cl)}$$

EXAMPLE 12–12

Determine the bandwidth of each of the amplifiers in Figure 12–45. Both op-amps have an open-loop gain of 100 dB and a unity-gain bandwidth of 3 MHz.

▶ **FIGURE 12–45**



Solution **(a)** For the noninverting amplifier in Figure 12–45(a), the closed-loop gain is

$$A_{cl} = 1 + \frac{R_f}{R_i} = 1 + \frac{220\ \text{k}\Omega}{3.3\ \text{k}\Omega} = 67.7$$

Use Equation 12–23 and solve for $f_{c(cl)}$ (where $f_{c(cl)} = BW_{cl}$).

$$f_{c(cl)} = BW_{cl} = \frac{\text{unity-gain } BW}{A_{cl}}$$

$$BW_{cl} = \frac{3\ \text{MHz}}{67.7} = \mathbf{44.3\ kHz}$$

(b) For the inverting amplifier in Figure 12–45(b), the closed-loop gain is

$$A_{cl} = -\frac{R_f}{R_i} = -\frac{47\ \text{k}\Omega}{1.0\ \text{k}\Omega} = -47$$

Using the absolute value of A_{cl}, the closed-loop bandwidth is

$$BW_{cl} = \frac{3\ \text{MHz}}{47} = \mathbf{63.8\ kHz}$$

SECTION 12–8 REVIEW

1. Is the closed-loop gain always less than the open-loop gain?
2. A certain op-amp is used in a feedback configuration having a gain of 30 and a bandwidth of 100 kHz. If the external resistor values are changed to increase the gain to 60, what is the new bandwidth?
3. What is the unity-gain bandwidth of the op-amp in Question 2?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OBJECTIVE TYPE QUESTIONS

Answers are at the end of the chapter.

1. If the voltage applied to Input 1 in Figure 12–4 is increased with respect to the voltage at Input 2, the voltage at Output 2 will
   (a) increase (b) decrease (c) not change
2. If $V_{in} = 1$ mV and R_f opens in the circuit of Figure 12–19, the output voltage will
   (a) increase (b) decrease (c) not change
3. If R_i is increased in the circuit of Figure 12–19, the voltage gain will
   (a) increase (b) decrease (c) not change
4. If 10 mV are applied to the input to the op-amp circuit of Figure 12–23 and R_f is increased, the output voltage will
   (a) increase (b) decrease (c) not change
5. In Figure 12–29, if R_f is changed from 100 kΩ to 68 kΩ, the feedback attenuation will
   (a) increase (b) decrease (c) not change
6. If the closed-loop gain in Figure 12–45(a) is increased by increasing the value of R_f, the closed-loop bandwidth will
   (a) increase (b) decrease (c) not change
7. If R_f is changed to 470 kΩ and R_i is changed to 10 kΩ in Figure 12–45(b), the closed-loop bandwidth will
   (a) increase (b) decrease (c) not change
8. If R_i in Figure 12–45(b) opens, the output voltage will
   (a) increase (b) decrease (c) not change
9. An integrated circuit (IC) op-amp has
   (a) two inputs and two outputs (b) one input and one output
   (c) two inputs and one output
10. Which of the following characteristics does not necessarily apply to an op-amp?
    (a) High gain (b) Low power
    (c) High input impedance (d) Low output impedance
11. A differential amplifier
    (a) is part of an op-amp (b) has one input and one output
    (c) has two outputs (d) answers (a) and (c)
12. When an op-amp is operated in the single-ended mode,
    (a) the output is grounded
    (b) one input is grounded and a signal is applied to the other
    (c) both inputs are connected together
    (d) the output is not inverted
13. In the differential mode,
    (a) opposite polarity signals are applied to the inputs
    (b) the gain is 1
    (c) the outputs are different amplitudes
    (d) only one supply voltage is used
14. In the common mode,
    (a) both inputs are grounded (b) the outputs are connected together
    (c) an identical signal appears on both inputs (d) the output signals are in-phase
15. Common-mode gain is
    (a) very high (b) very low (c) always unity (d) unpredictable
16. If $A_{v(d)} = 3500$ and $A_{cm} = 0.35$, the CMRR is
    (a) 1225 (b) 10,000 (c) 80 dB (d) answers (b) and (c)

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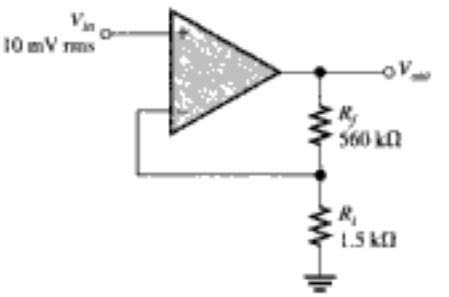
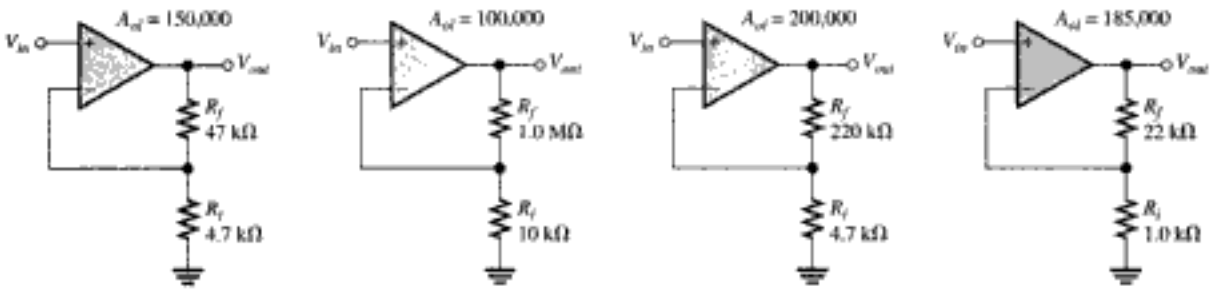
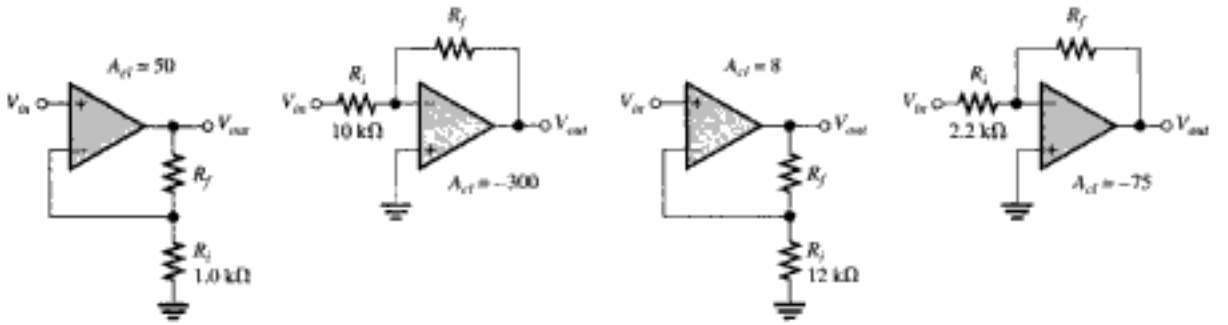
► FIGURE 12–49





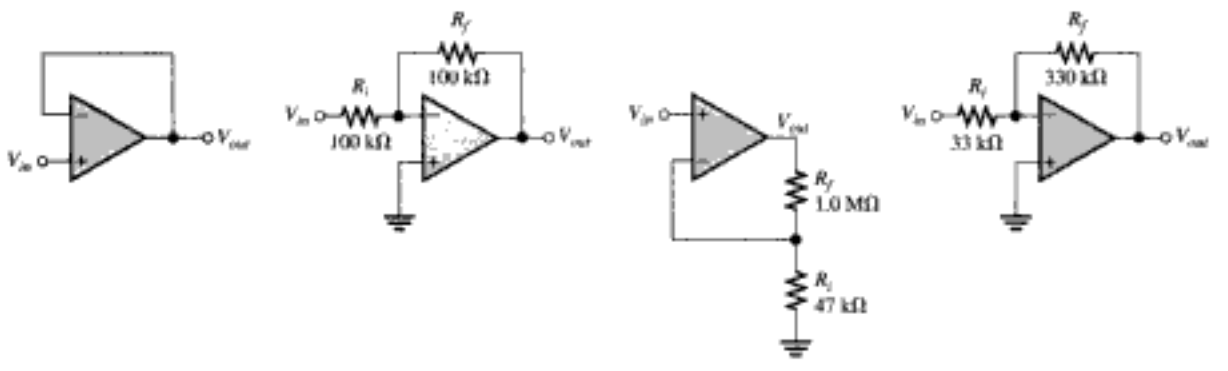
▲ FIGURE 12–50



▲ FIGURE 12–51

16. Find the gain of each amplifier in Figure 12–52.

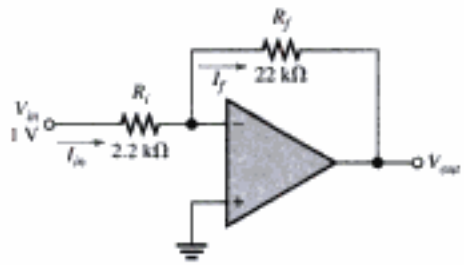
17. If a signal voltage of 10 mV rms is applied to each amplifier in Figure 12–52, what are the output voltages and what is their phase relationship with inputs?



▲ FIGURE 12–52

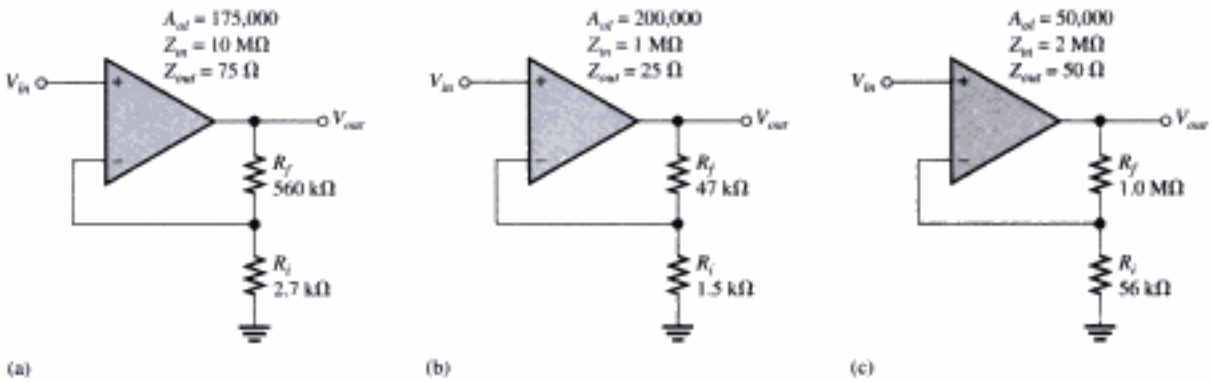
18. Determine the approximate values for each of the following quantities in Figure 12–53.
(a) I_{in} **(b)** I_f **(c)** V_{out} **(d)** closed-loop gain

▶ FIGURE 12–53



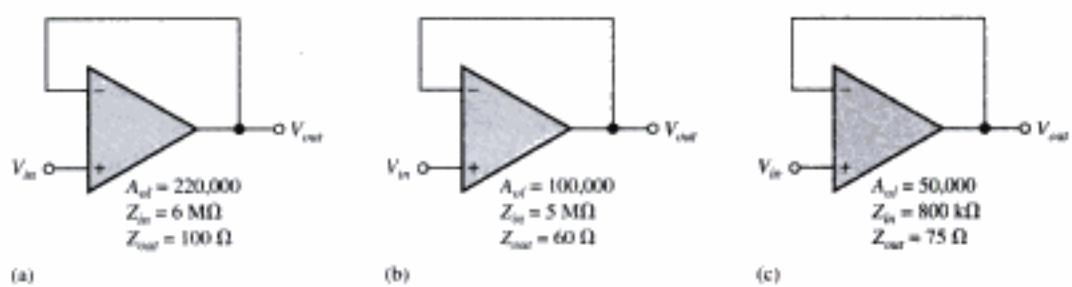
SECTION 12–5 Effects of Negative Feedback on Op-Amp Impedances

19. Determine the input and output impedances for each amplifier configuration in Figure 12–54.



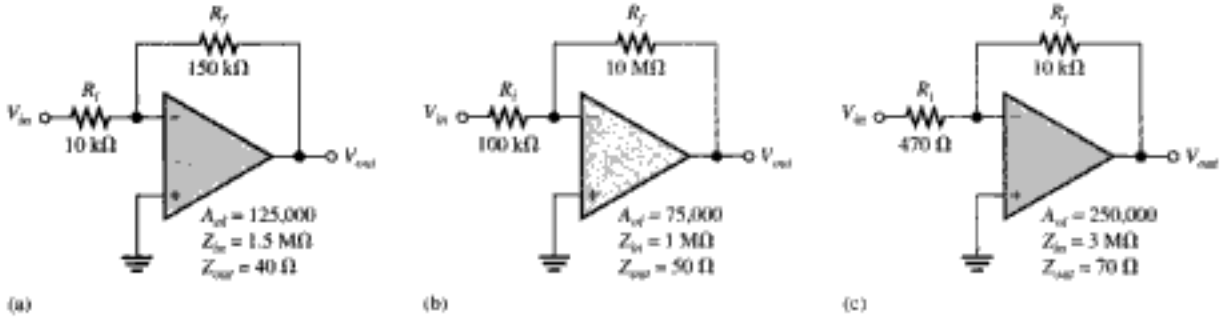
▲ FIGURE 12–54

20. Repeat Problem 19 for each circuit in Figure 12–55.



▲ FIGURE 12–55

21. Repeat Problem 19 for each circuit in Figure 12–56.



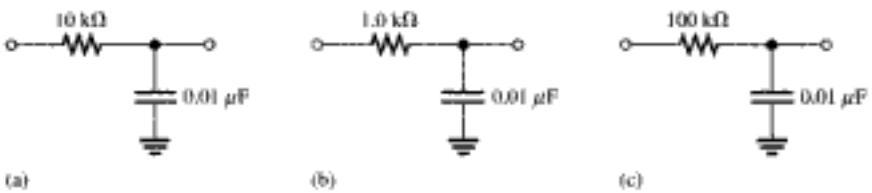
▲ FIGURE 12–56

SECTION 12–6 Bias Current and Offset Voltage Compensation

22. A voltage-follower is driven by a voltage source with a source resistance of 75 Ω.
    (a) What value of compensating resistor is required for bias current, and where should the resistor be placed?
    (b) If the two input currents after compensation are 42 μA and 40 μA, what is the output error voltage?
23. Determine the compensating resistor value for each amplifier configuration in Figure 12–54, and indicate the placement of the resistor.
24. A particular op-amp voltage-follower has an input offset voltage of 2 nV. What is the output error voltage?
25. What is the input offset voltage of an op-amp if a dc output voltage of 35 mV is measured when the input voltage is zero? The op-amp's open-loop gain is specified to be 200,000.

SECTION 12–7 Open-Loop Response

26. The midrange open-loop gain of a certain op-amp is 120 dB. Negative feedback reduces this gain by 50 dB. What is the closed-loop gain?
27. The upper critical frequency of an op-amp's open-loop response is 200 Hz. If the midrange gain is 175,000, what is the ideal gain at 200 Hz? What is the actual gain? What is the op-amp's open-loop bandwidth?
28. An *RC* lag circuit has a critical frequency of 5 kHz. If the resistance value is 1.0 kΩ, what is X_C when $f = 3$ kHz?
29. Determine the attenuation of an *RC* lag circuit with $f_c = 12$ kHz for each of the following frequencies.
    (a) 1 kHz (b) 5 kHz (c) 12 kHz (d) 20 kHz (e) 100 kHz
30. The midrange open-loop gain of a certain op-amp is 80,000. If the open-loop critical frequency is 1 kHz, what is the open-loop gain at each of the following frequencies?
    (a) 100 Hz (b) 1 kHz (c) 10 kHz (d) 1 MHz
31. Determine the phase shift through each circuit in Figure 12–57 at a frequency of 2 kHz.



▲ FIGURE 12–57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3. A higher CMRR results in a lower common-mode gain.
4. Input bias current, input offset voltage, drift, input offset current, input impedance, output impedance, common-mode input voltage range, CMRR, open-loop voltage gain, slew rate, frequency response.
5. Slew rate and voltage gain are both frequency dependent.

SECTION 12–3 Negative Feedback

1. Negative feedback provides a stable controlled voltage gain, control of impedances, and wider bandwidth.
2. The open-loop gain is so high that a very small signal on the input will drive the op-amp into saturation.

SECTION 12–4 Op-Amps with Negative Feedback

1. The main purpose of negative feedback is to stabilize the gain.
2. False
3. $A_{cl} = 1/0.02 = 50$

SECTION 12–5 Effects of Negative Feedback on Op-Amp Impedances

1. The noninverting configuration has a higher Z_{in} than the op-amp alone.
2. Z_{in} increases in a voltage-follower.
3. $Z_{in(cl)} = R_i = 2\ \text{k}\Omega$, $Z_{out(cl)} = Z_{out}/(1 + A_{ol}B) = 25\ \text{m}\Omega$

SECTION 12–6 Bias Current and Offset Voltage Compensation

1. Input bias current and input offset voltage are sources of output error.
2. Add a resistor in the feedback path equal to the input source resistance.

SECTION 12–7 Open-Loop Response

1. Open-loop voltage gain is without feedback, and closed-loop voltage gain is with negative feedback. Open-loop voltage gain is larger.
2. $BW = 100\ \text{Hz}$
3. A_{ol} decreases.
4. $A_{v(ol)} = 20\ \text{dB} + 30\ \text{dB} = 50\ \text{dB}$
5. $\theta_{tot} = -49° + (-5.2°) = -54.2°$

SECTION 12–8 Closed-Loop Response

1. Yes, A_{cl} is always less than A_{ol}.
2. $BW = 3{,}000\ \text{kHz}/60 = 50\ \text{kHz}$
3. unity-gain $BW = 3{,}000\ \text{kHz}/1 = 3\ \text{MHz}$

OBJECTIVE TYPE QUESTIONS

1. (a)	**2.** (a)	**3.** (b)	**4.** (a)	**5.** (a)	**6.** (b)	**7.** (c)	**8.** (b)	**9.** (c)	**10.** (b)
11. (d)	**12.** (b)	**13.** (a)	**14.** (c)	**15.** (b)	**16.** (d)	**17.** (c)	**18.** (d)	**19.** (a)	**20.** (b)
21. (c)	**22.** (c)	**23.** (d)	**24.** (b)	**25.** (c)	**26.** (a)	**27.** (c)	**28.** (d)	**29.** (b)	**30.** (a)
31. (b)	**32.** (d)	**33.** (a)	**34.** (d)	**35.** (c)	**36.** (b)	**37.** (d)			

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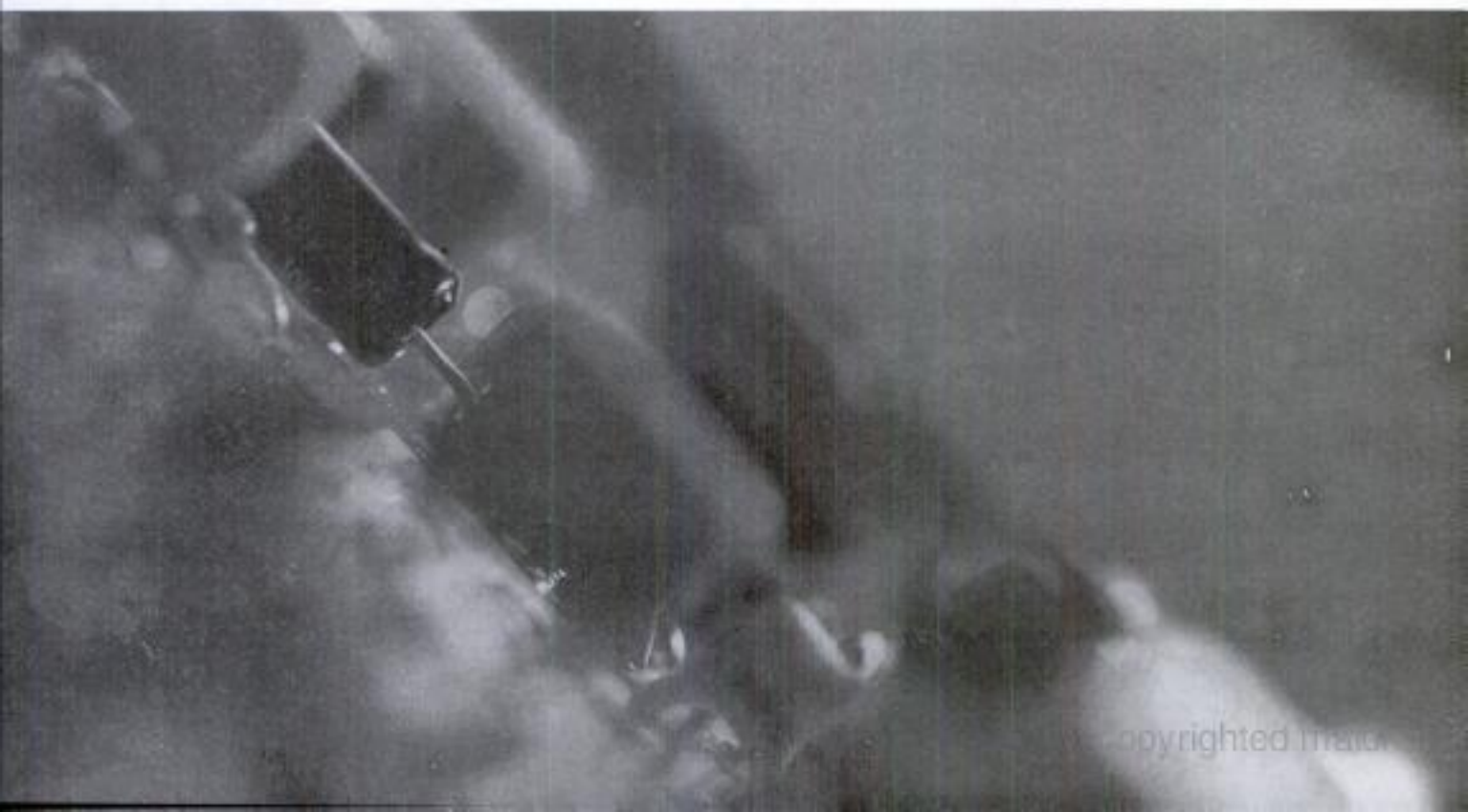
13

BASIC OP-AMP CIRCUITS

CHAPTER OUTLINE

INTRODUCTION

Op-amps are used in such a wide variety of circuits and applications that it is impossible to cover all of them in one chapter, or even in one book. Therefore, in this chapter, four fundamentally important circuits are covered to give you a foundation in op-amp circuits.

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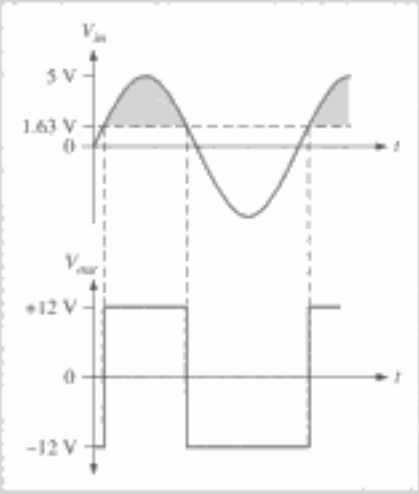
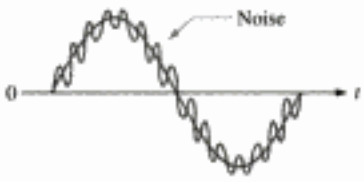
As shown in Figure 13–4, each time the input exceeds +1.63 V, the output voltage switches to its +12 V level, and each time the input goes below +1.63 V, the output switches back to its −12 V level, neglecting hysteresis.

▶ **FIGURE 13–4**



Effects of Input Noise on Comparator Operation

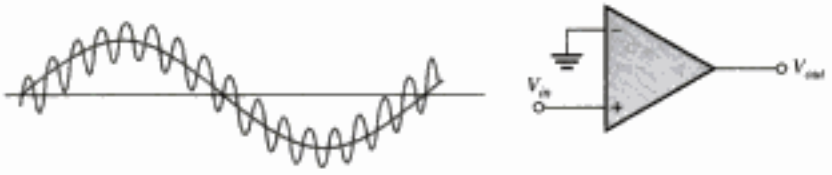


▲ **FIGURE 13–5**

Sine wave with superimposed noise.

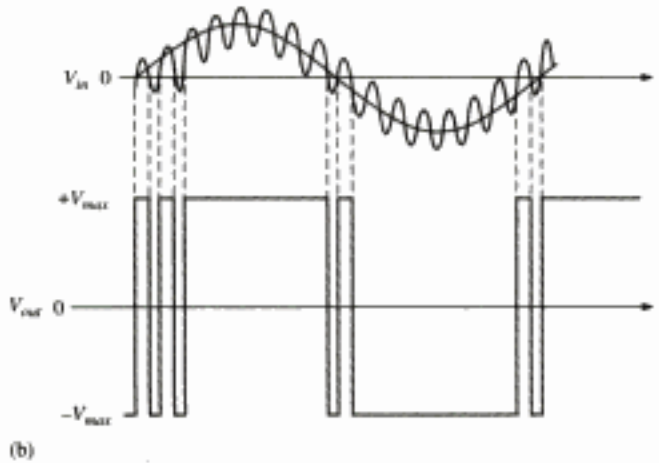
In many practical situations, **noise** (unwanted voltage fluctuations) appears on the input line. This noise voltage becomes superimposed on the input voltage, as shown in Figure 13–5 for the case of a sine wave, and can cause a comparator to erratically switch output states.

In order to understand the potential effects of noise voltage, consider a low-frequency sinusoidal voltage applied to the noninverting (+) input of an op-amp comparator used as a zero-level detector, as shown in Figure 13–6(a). Part (b) of the figure shows the input sine wave plus noise and the resulting output. As you can see, when the sine wave approaches 0, the fluctuations due to noise cause the total input to vary above and below 0 several times, thus producing an erratic output voltage.



◀ **FIGURE 13–6**

Effects of noise on comparator circuit.

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When V_{in} exceeds V_{UTP}, the output voltage drops to its negative maximum, $-V_{out(max)}$, as shown in part (a). Now the voltage fed back to the noninverting input is V_{LTP} and is expressed as

Equation 13–2

$$V_{LTP} = \frac{R_2}{R_1 + R_2}(-V_{out(max)})$$

The input voltage must now fall below V_{LTP}, as shown in part (b), before the device will switch from the maximum negative voltage back to the maximum positive voltage. This means that a small amount of noise voltage has no effect on the output, as illustrated by Figure 13–8(c).

A comparator with hysteresis is sometimes known as a **Schmitt trigger**. The amount of hysteresis is defined by the difference of the two trigger levels.

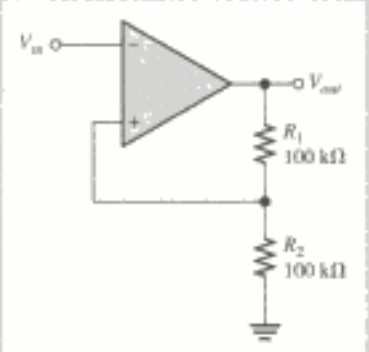
Equation 13–3

$$V_{HYS} = V_{UTP} - V_{LTP}$$

EXAMPLE 13–2

Determine the upper and lower trigger points for the comparator circuit in Figure 13–9. Assume that $+V_{out(max)} = +5\text{ V}$ and $-V_{out(max)} = -5\text{ V}$.

▶ **FIGURE 13–9**



Solution

$$V_{UTP} = \frac{R_2}{R_1 + R_2}(+V_{out(max)}) = 0.5(5\text{ V}) = \mathbf{+2.5\text{ V}}$$

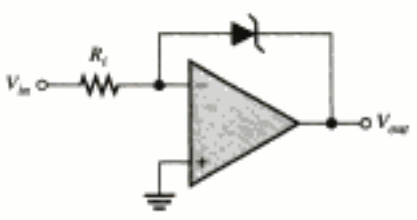
$$V_{LTP} = \frac{R_2}{R_1 + R_2}(-V_{out(max)}) = 0.5(-5\text{ V}) = \mathbf{-2.5\text{ V}}$$

Output Bounding

In some applications, it is necessary to limit the output voltage levels of a comparator to a value less than that provided by the saturated op-amp. A single zener diode can be used, as shown in Figure 13–10, to limit the output voltage to the zener voltage in one direction and to the forward diode drop in the other. This process of limiting the output range is called **bounding**.

▶ **FIGURE 13–10**

Comparator with output bounding.



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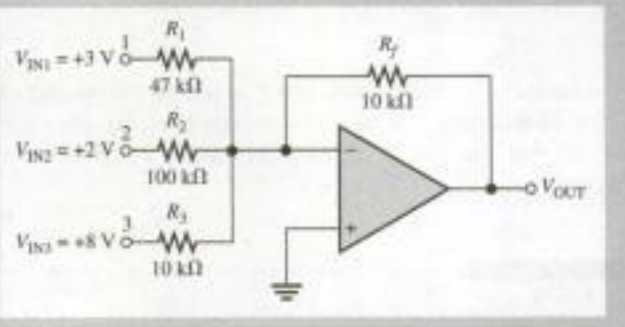
EXAMPLE 13–7

Determine the weight of each input voltage for the scaling adder in Figure 13–20 and find the output voltage.

► FIGURE 13–20



Solution

$$\text{Weight of input 1: } \frac{R_f}{R_1} = \frac{10\,\text{k}\Omega}{47\,\text{k}\Omega} = \mathbf{0.213}$$

$$\text{Weight of input 2: } \frac{R_f}{R_2} = \frac{10\,\text{k}\Omega}{100\,\text{k}\Omega} = \mathbf{0.100}$$

$$\text{Weight of input 3: } \frac{R_f}{R_3} = \frac{10\,\text{k}\Omega}{10\,\text{k}\Omega} = \mathbf{1.00}$$

The output voltage is

$$\begin{aligned} V_{OUT} &= -\left(\frac{R_f}{R_1}V_{IN1} + \frac{R_f}{R_2}V_{IN2} + \frac{R_f}{R_3}V_{IN3}\right) \\ &= -[0.213(3\text{ V}) + 0.100(2\text{ V}) + 1.00(8\text{ V})] \\ &= -(0.639\text{ V} + 0.2\text{ V} + 8\text{ V}) = \mathbf{-8.84\text{ V}} \end{aligned}$$

SECTION 13–2 REVIEW

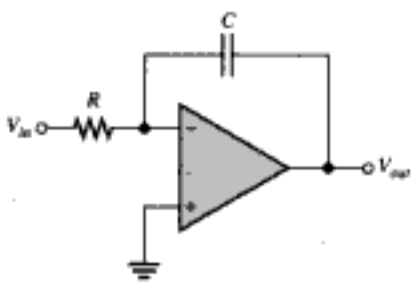
1. Define *summing point*.
2. What is the value of R_f/R for a five-input averaging amplifier?
3. A certain scaling adder has two inputs, one having twice the weight of the other. If the resistor value for the lower-weighted input is 10 kΩ, what is the value of the other input resistor?

13–3 INTEGRATORS AND DIFFERENTIATORS

An op-amp integrator simulates mathematical integration, which is basically a summing process that determines the total area under the curve of a function. An op-amp differentiator simulates mathematical differentiation, which is a process of determining the instantaneous rate of change of a function. It is not necessary for you to understand mathematical integration or differentiation, at this point, in order to learn how an integrator and differentiator work. The integrators and differentiators shown in this section are idealized to show basic principles. Practical integrators often have an additional resistor or other circuitry in parallel with the feedback capacitor to prevent saturation. Practical differentiators may include a series resistor to reduce high frequency noise.

The Op-Amp Integrator

An ideal **integrator** is shown in Figure 13–21. Notice that the feedback element is a capacitor that forms an *RC* circuit with the input resistor. Although a large-value resistor is normally used in parallel with the capacitor to limit the gain, it does not affect the basic operation and is not shown for purposes of this analysis.



◀ **FIGURE 13–21**
An op-amp integrator.

How a Capacitor Charges To understand how the integrator works, it is important to review how a capacitor charges. Recall that the charge Q on a capacitor is proportional to the charging current (I_C) and the time (t).

$$Q = I_C t$$

Also, in terms of the voltage, the charge on a capacitor is

$$Q = CV_C$$

From these two relationships, the capacitor voltage can be expressed as

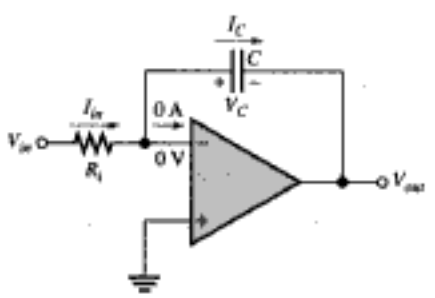
$$V_C = \left(\frac{I_C}{C}\right)t$$

This expression has the form of an equation for a straight line that begins at zero with a constant slope of I_C/C. Remember from algebra that the general formula for a straight line is $y = mx + b$. In this case, $y = V_C$, $m = I_C/C$, $x = t$, and $b = 0$.

Recall that the capacitor voltage in a simple *RC* circuit is not linear but is exponential. This is because the charging current continuously decreases as the capacitor charges and causes the rate of change of the voltage to continuously decrease. The key thing about using an op-amp with an *RC* circuit to form an integrator is that the capacitor's charging current is made constant, thus producing a straight-line (linear) voltage rather than an exponential voltage. Now let's see why this is true.

In Figure 13–22, the inverting input of the op-amp is at virtual ground (0 V), so the voltage across R_i equals V_{in}. Therefore, the input current is

$$I_{in} = \frac{V_{in}}{R_i}$$



◀ **FIGURE 13–22**
Currents in an integrator.

If V_{in} is a constant voltage, then I_{in} is also a constant because the inverting input always remains at 0 V, keeping a constant voltage across R_i. Because of the very high input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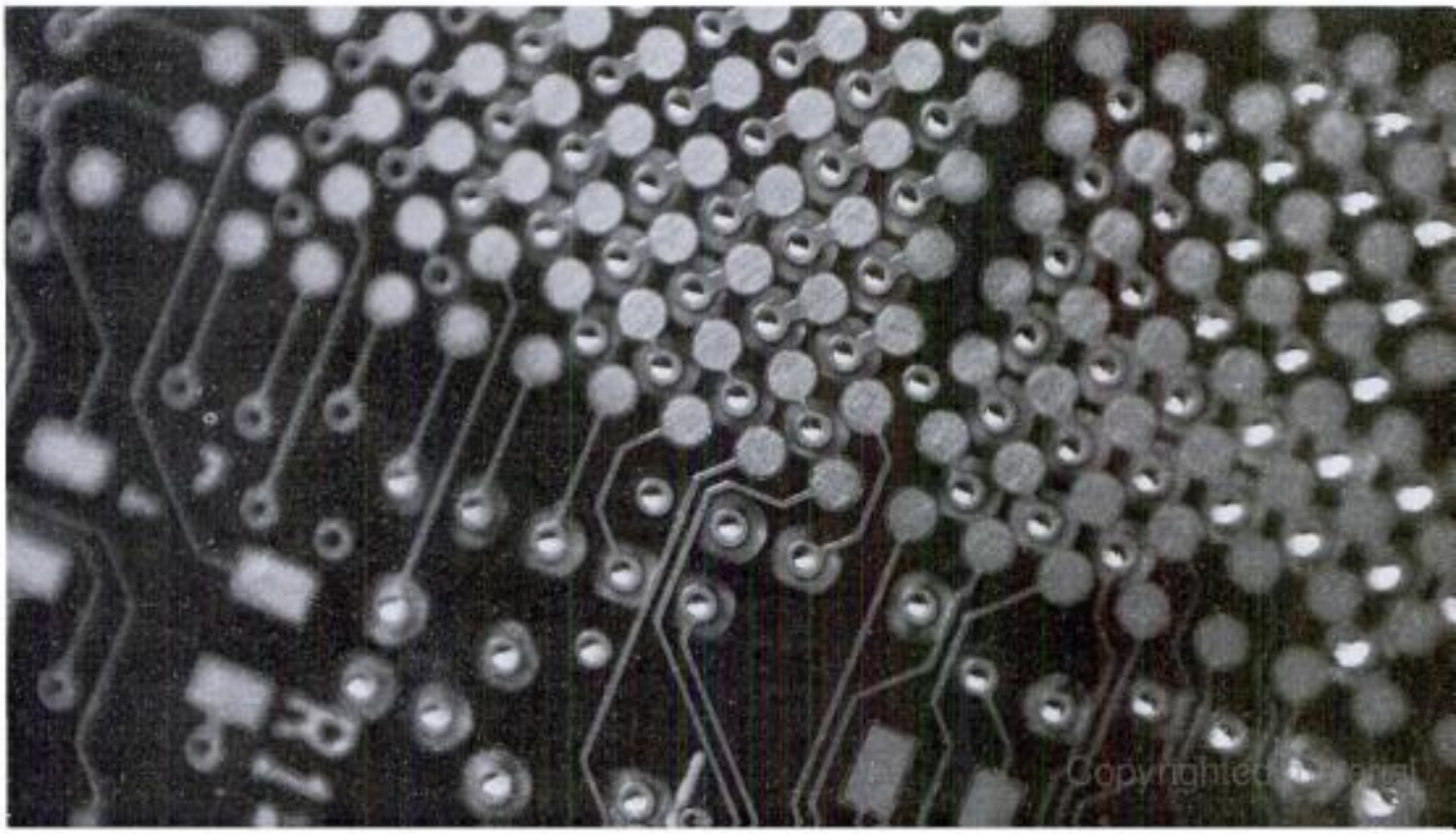
14

SPECIAL-PURPOSE OP-AMP CIRCUITS

CHAPTER OUTLINE

INTRODUCTION

A general-purpose op-amp, such as the 741, is a versatile and widely used device. However, some specialized IC amplifiers are available that have certain features or characteristics oriented to special applications. Most of these devices are actually derived from the basic op-amp. These special circuits include the instrumentation amplifier that is used in high-noise environments, the isolation amplifier that is used in high-voltage and medical applications, the operational transconductance amplifier (OTA) that is used as a voltage-to-current amplifier, and the logarithmic amplifiers that are used for linearizing certain types of inputs and for mathematical operations.



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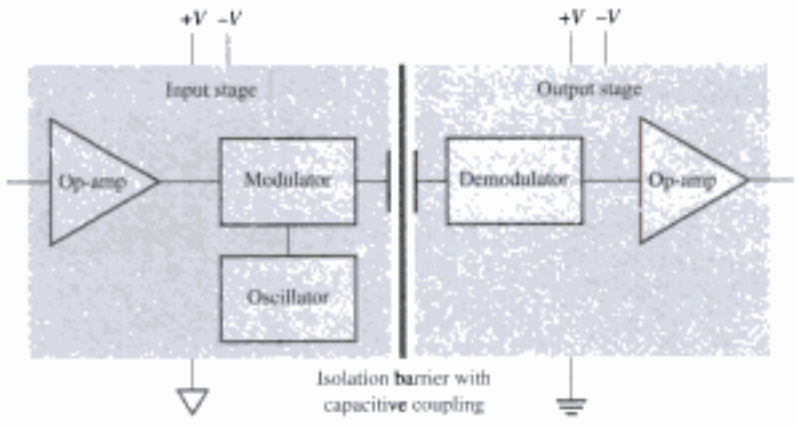
A Basic Capacitor-Coupled Isolation Amplifier

An **isolation amplifier** is a device that consists of two electrically isolated stages. The input stage and the output stage are separated from each other by an isolation barrier so that a signal must be processed in order to be coupled across the isolation barrier. Some isolation amplifiers use optical coupling or transformer coupling to provide isolation between the stages. However, most modern isolation amplifiers use capacitive coupling for isolation. Each stage has separate supply voltages and grounds so that there are no common electrical paths between them. A simplified block diagram for a typical isolation amplifier is shown in Figure 14–8. Notice two different ground symbols are used to reinforce the concept of stage separation.



◄ FIGURE 14–8
Simplified block diagram of a typical isolation amplifier.

The input stage consists of an amplifier, an oscillator, and a modulator. **Modulation** is the process of allowing a signal containing information to modify a characteristic of another signal, such as amplitude, frequency, or pulse width, so that the information in the first signal is also contained in the second. In this case, the modulator uses a high-frequency square-wave oscillator to modify the original signal. A small-value capacitor in the isolation barrier is used to couple the lower-frequency modulated signal or dc voltage from the input to the output. Without modulation, prohibitively high-value capacitors would be necessary with a resulting degradation in the isolation between the stages. The output stage consists of a demodulator that extracts the original input signal from the modulated signal so that the original signal from the input stage is back to its original form.

The high-frequency oscillator output in Figure 14–8 can be either amplitude or pulse-width modulated by the signal from the input amplifier (oscillators are covered in Chapter 16). In amplitude modulation, the amplitude of the oscillator output is varied corresponding to the variations of the input signal, as indicated in Figure 14–9(a), which uses one cycle of a sine wave for illustration. In pulse-width modulation, the duty cycle of the oscillator output is varied by changing the pulse width corresponding to the variations of the input signal. An isolation amplifier using pulse-width modulation is represented in Figure 14–9(b).

Although it uses a relatively complex process internally, the isolation amplifier is still just an amplifier and is simple to use. When dc supply voltages and an input signal are applied, an amplified output signal is the result. The isolation function itself is an unseen process.

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Solution The voltage gain of the input stage is

$$A_{v1} = \frac{R_{f1}}{R_{i1}} + 1 = \frac{22\,\text{k}\Omega}{2.2\,\text{k}\Omega} + 1 = 10 + 1 = 11$$

The voltage gain of the output stage is

$$A_{v2} = \frac{R_{f2}}{R_{i2}} + 1 = \frac{47\,\text{k}\Omega}{10\,\text{k}\Omega} + 1 = 4.7 + 1 = 5.7$$

The total voltage gain of the isolation amplifier is

$$A_{v(\text{tot})} = A_{v1}A_{v2} = (11)(5.7) = \mathbf{62.7}$$

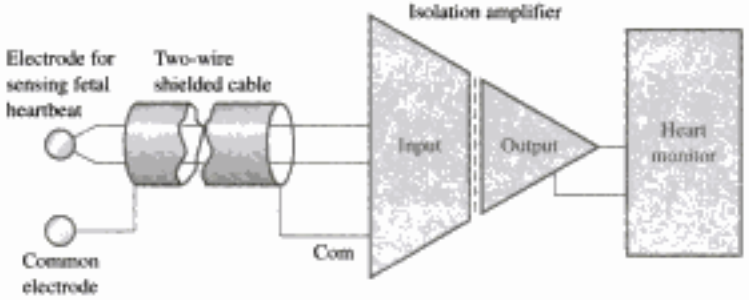
Applications

As previously mentioned, the isolation amplifier is used in applications that require no common grounds between a transducer and the processing circuits where interfacing to sensitive equipment is required. In chemical, nuclear, and metal-processing industries, for example, millivolt signals typically exist in the presence of large common-mode voltages that can be in the kilovolt range. In this type of environment, the isolation amplifier can amplify small signals from very noisy equipment and provide a safe output to sensitive equipment such as computers.

Another important application is in various types of medical equipment. In medical applications where body functions such as heart rate and blood pressure are monitored, the very small monitored signals are combined with large common-mode signals, such as 60 Hz power-line pickup from the skin. In these situations, without isolation, dc leakage or equipment failure could be fatal. Figure 14–13 shows a simplified diagram of an isolation amplifier in a cardiac-monitoring application. In this situation, heart signals, which are very small, are combined with much larger common-mode signals caused by muscle noise, electrochemical noise, residual electrode voltage, and 60 Hz power-line pickup from the skin.

▶ FIGURE 14–13

Fetal heartbeat monitoring using an isolation amplifier.



The monitoring of fetal heartbeat, as illustrated, is the most demanding type of cardiac monitoring because in addition to the fetal heartbeat that typically generates 50 μV, there is also the mother's heartbeat that typically generates 1 mV. The common-mode voltages can run from about 1 mV to about 100 mV. The CMR (common-mode rejection) of the isolation amplifier separates the signal of the fetal heartbeat from that of the mother's heartbeat and from those common-mode signals. Therefore, the signal from the fetal heartbeat is essentially all that the amplifier sends to the monitoring equipment.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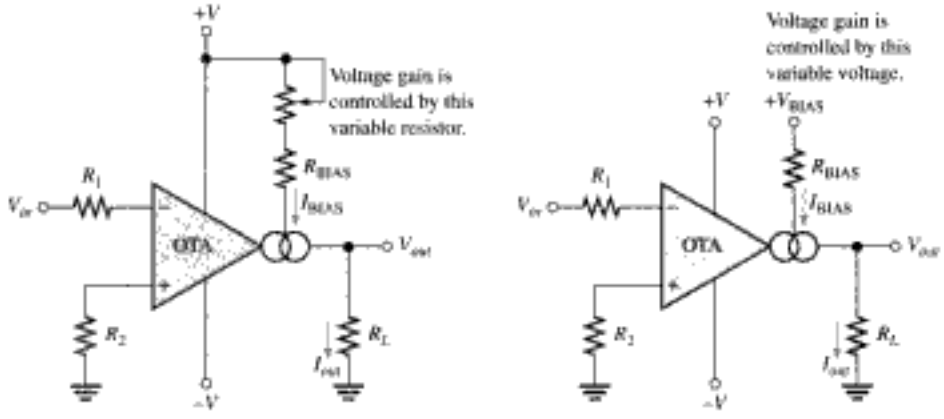
variable resistor in series with R_{BIAS} in the circuit of Figure 14–16. By changing the resistance, you can produce a change in I_{BIAS}, which changes the transconductance. A change in the transconductance changes the voltage gain. The voltage gain can also be controlled with an externally applied variable voltage, as shown in Figure 14–17(b). A variation in the applied bias voltage causes a change in the bias current.

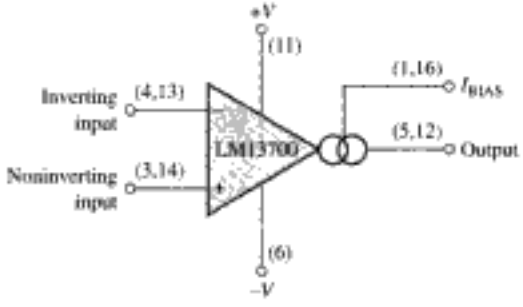


(a) Amplifier with resistance-controlled gain

(b) Amplifier with voltage-controlled gain

◄ FIGURE 14–17

An OTA as an inverting amplifier with a variable-voltage gain.



◄ FIGURE 14–18

An LM13700 OTA. There are two in an IC package. The buffer transistors are not shown. Pin numbers for both OTAs are given in parentheses.

A Specific OTA

The LM13700 is a typical OTA and serves as a representative device. The LM13700 is a dual-device package containing two OTAs and buffer circuits. Figure 14–18 shows the pin configuration using a single OTA in the package. The maximum dc supply voltages are ±18 V, and its transconductance characteristic happens to be the same as indicated by the graph in Figure 14–15. For an LM13700, the bias current is determined by the following formula:

$$I_{BIAS} = \frac{+V_{BIAS} - (-V) - 1.4\text{ V}}{R_{BIAS}}$$

The 1.4 V is due to the internal circuit where a base-emitter junction and a diode connect the external R_{BIAS} with the negative supply voltage ($-V$). The positive bias voltage, $+V_{BIAS}$, may be obtained from the positive supply voltage, $+V$.

Not only does the transconductance of an OTA vary with bias current, but so do the input and output resistances. Both the input and output resistances decrease as the bias current increases, as shown in Figure 14–19.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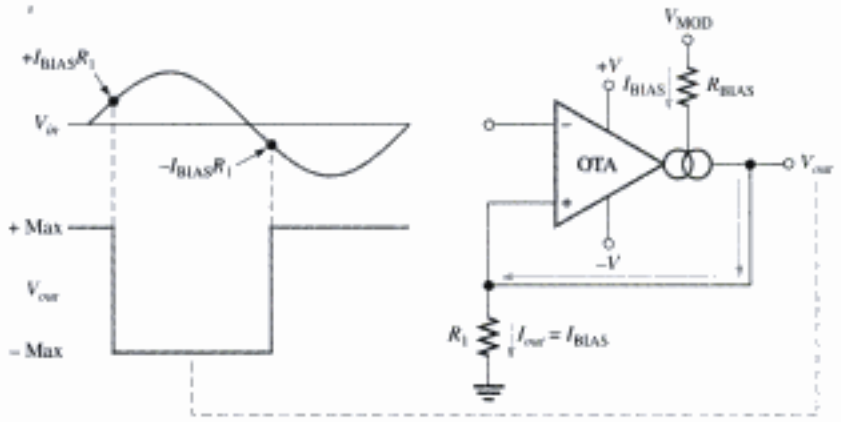


◀ FIGURE 14–25

Basic operation of the OTA Schmitt trigger.

SECTION 14–3 REVIEW

1. What does OTA stand for?
2. If the bias current in an OTA is increased, does the transconductance increase or decrease?
3. What happens to the voltage gain if the OTA is connected as a fixed-voltage amplifier and the supply voltages are increased?
4. What happens to the voltage gain if the OTA is connected as a variable-gain voltage amplifier and the voltage at the bias terminal is decreased?

14–4 LOG AND ANTILOG AMPLIFIERS

Log and antilog amplifiers are used in applications that require compression of analog input data, linearization of transducers that have exponential outputs, and analog multiplication and division. In this section, we will discuss the principles of logarithmic amplifiers.

The **logarithm** of a number is the power to which the base must be raised to get that number. A logarithmic (log) amplifier produces an output that is proportional to the logarithm of the input, and antilogarithmic (antilog) amplifiers take the antilog or inverse log of the input.

The Basic Logarithmic Amplifier

The key element in a log amplifier is a device that exhibits a logarithmic characteristic that, when placed in the feedback loop of an op-amp, produces a logarithmic response. This means that the output voltage is a function of the logarithm of the input voltage, as expressed by the following general equation:

$$V_{out} = -K \ln(V_{in}) \qquad \textbf{Equation 14–8}$$

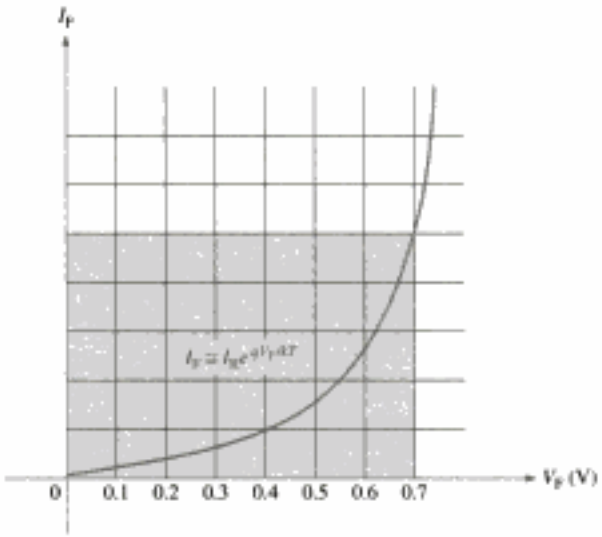
where K is a constant and ln is the natural logarithm to the base e. A **natural logarithm** is the exponent to which the base e must be raised in order to equal a given quantity. Although we will use natural logarithms in the formulas in this section, each expression can be converted to a logarithm to the base 10 ($\log_{10}$) using the relationship $\ln x = 2.3 \log_{10} x$.

The semiconductor *pn* junction in the form of either a diode or the base-emitter junction of a BJT provides a logarithmic characteristic. You may recall that a diode has a

nonlinear characteristic up to a forward voltage of approximately 0.7 V. Figure 14–26 shows the characteristic curve, where V_F is the forward diode voltage and I_F is the forward diode current.

▶ FIGURE 14–26

A portion of a diode (*pn* junction) characteristic curve (V_F versus I_F).



As you can see on the graph, the diode curve is nonlinear. Not only is the characteristic curve nonlinear, it is logarithmic and is specifically defined by the following formula:

$$I_F \cong I_R e^{qV_F/kT}$$

where I_R is the reverse leakage current, q is the charge on an electron, k is Boltzmann's constant, and T is the absolute temperature in Kelvin. From the previous equation, the diode forward voltage, V_F, can be determined as follows. Take the natural logarithm (*ln* is the logarithm to the base e) of both sides.

$$\ln I_F = \ln I_R e^{qV_F/kT}$$

The ln of a product of two terms equals the sum of the ln of each term.

$$\ln I_F = \ln I_R + \ln e^{qV_F/kT} = \ln I_R + \frac{qV_F}{kT}$$

$$\ln I_F - \ln I_R = \frac{qV_F}{kT}$$

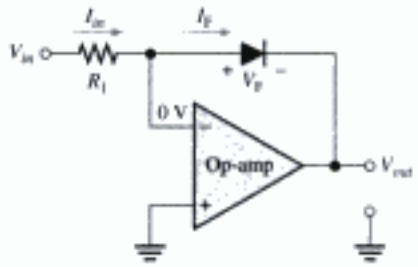
The difference of two ln terms equals the ln of the quotient of the terms.

$$\ln\left(\frac{I_F}{I_R}\right) = \frac{qV_F}{kT}$$

Solving for V_F,

$$V_F = \left(\frac{kT}{q}\right)\ln\left(\frac{I_F}{I_R}\right)$$

Log Amplifier with a Diode When you place a diode in the feedback loop of an op-amp circuit, as shown in Figure 14–27, you have a basic log amplifier. Since the inverting input is at virtual ground (0 V), the output is at $-V_F$ when the input is positive. Since V_F is logarithmic, so is V_{out}. The output is limited to a maximum value of approximately -0.7 V because the diode's logarithmic characteristic is restricted to voltages below 0.7 V. Also, the input must be positive when the diode is connected in the direction shown in the figure. To handle negative inputs, you must turn the diode around.



◄ FIGURE 14–27

A basic log amplifier using a diode as the feedback element.

An analysis of the circuit in Figure 14–27 is as follows, beginning with the facts that $V_{out} = -V_F$ and $I_F = I_{in}$ because there is no current at the inverting input.

$$V_{out} = -V_F$$

$$I_F = I_{in} = \frac{V_{in}}{R_1}$$

Substituting into the formula for V_F,

$$V_{out} = -\left(\frac{kT}{q}\right)\ln\left(\frac{V_{in}}{I_R R_1}\right)$$

The term kT/q is a constant equal to approximately 25 mV at 25°C. Therefore, the output voltage can be expressed as

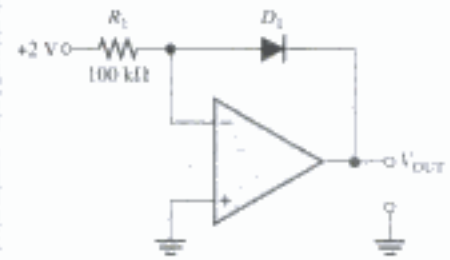
$$V_{out} \cong -(0.025\text{ V})\ln\left(\frac{V_{in}}{I_R R_1}\right) \qquad \textbf{Equation 14–9}$$

From Equation 14–9, u can see that the output voltage is the negative of a logarithmic function of the input voltage. The value of the output is controlled by the value of the input voltage and the value of the resistor R_1. The other factor, I_R, is a constant for a given diode.

EXAMPLE 14–8

Determine the output voltage for the log amplifier in Figure 14–28. Assume $I_R = 50$ nA.

► FIGURE 14–28



Solution The input voltage and the resistor value are given in Figure 14–28.

$$V_{OUT} = -(0.025\text{ V})\ln\left(\frac{V_{in}}{I_R R_1}\right) = -(0.025\text{ V})\ln\left(\frac{2\text{ V}}{50\text{ nA} \times 100\text{ k}\Omega}\right)$$

$$= -(0.025\text{ V})\ln(400) = -(0.025\text{ V})(5.99) = \mathbf{-0.150\text{ V}}$$

Log Amplifier with a BJT The base-emitter junction of a bipolar junction transistor exhibits the same type of logarithmic characteristic as a diode because it is also a *pn* junction. A log amplifier with a BJT connected in a common-base form in the feedback loop is shown in Figure 14–29. Notice that V_{out} with respect to ground is equal to $-V_{BE}$.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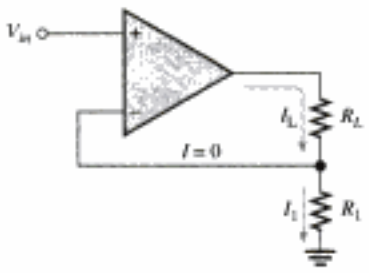
▶ **FIGURE 14–35**

Voltage-to-current converter.



Neglecting the input offset voltage, both inverting and noninverting input terminals of the op-amp are at the same voltage, V_{in}. Therefore, the voltage across R_1 equals V_{in}. Since there is negligible current at the inverting input, the current through R_1 is the same as the current through R_L; thus

Equation 14–14

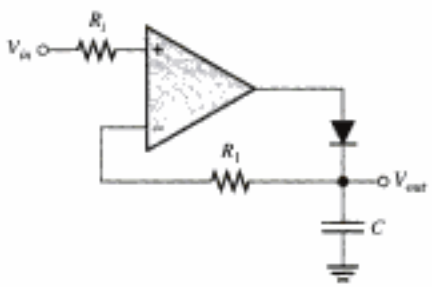
$$I_L = \frac{V_{in}}{R_1}$$

Peak Detector

An interesting application of the op-amp is in a peak detector circuit such as the one shown in Figure 14–36. In this case the op-amp is used as a comparator. This circuit is used to detect the peak of the input voltage and store that peak voltage on a capacitor. For example, this circuit can be used to detect and store the maximum value of a voltage surge; this value can then be measured at the output with a voltmeter or recording device. The basic operation is as follows. When a positive voltage is applied to the noninverting input of the op-amp through R_i, the high-level output voltage of the op-amp forward-biases the diode and charges the capacitor. The capacitor continues to charge until its voltage reaches a value equal to the input voltage and thus both op-amp inputs are at the same voltage. At this point, the op-amp comparator switches, and its output goes to the low level. The diode is now reverse-biased, and the capacitor stops charging. It has reached a voltage equal to the peak of V_{in} and will hold this voltage until the charge eventually leaks off. If a greater input peak occurs, the capacitor charges to the new peak.

▶ **FIGURE 14–36**

A basic peak detector.



SECTION 14–5 REVIEW

1. For the constant-current source in Figure 14–33, the input reference voltage is 6.8 V and R_i is 10 kΩ. What value of constant current does the circuit supply to a 1.0 kΩ load? To a 5 kΩ load?
2. What element determines the constant of proportionality that relates input current to output voltage in the current-to-voltage converter?

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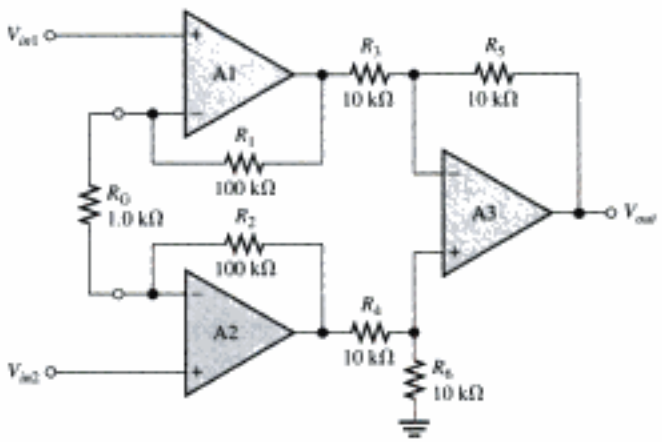
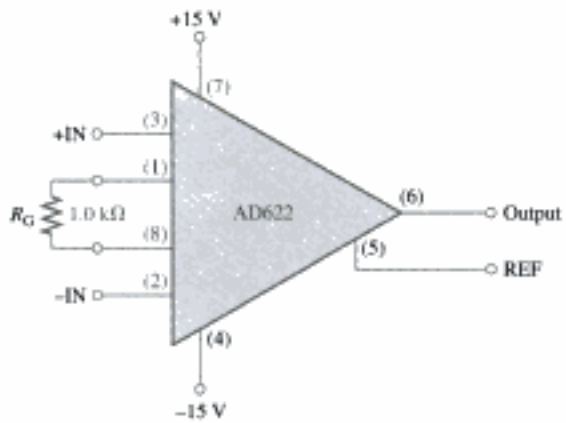
► FIGURE 14–37



2. Find the overall voltage gain of the instrumentation amplifier in Figure 14–37.
3. The following voltages are applied to the instrumentation amplifier in Figure 14–37: $V_{in1} = 5$ mV, $V_{in2} = 10$ mV, and $V_{cm} = 225$ mV. Determine the final output voltage.
4. What value of R_G must be used to change the gain of the instrumentation amplifier in Figure 14–37 to 1000?
5. What is the voltage gain of the AD622 instrumentation amplifier in Figure 14–38?

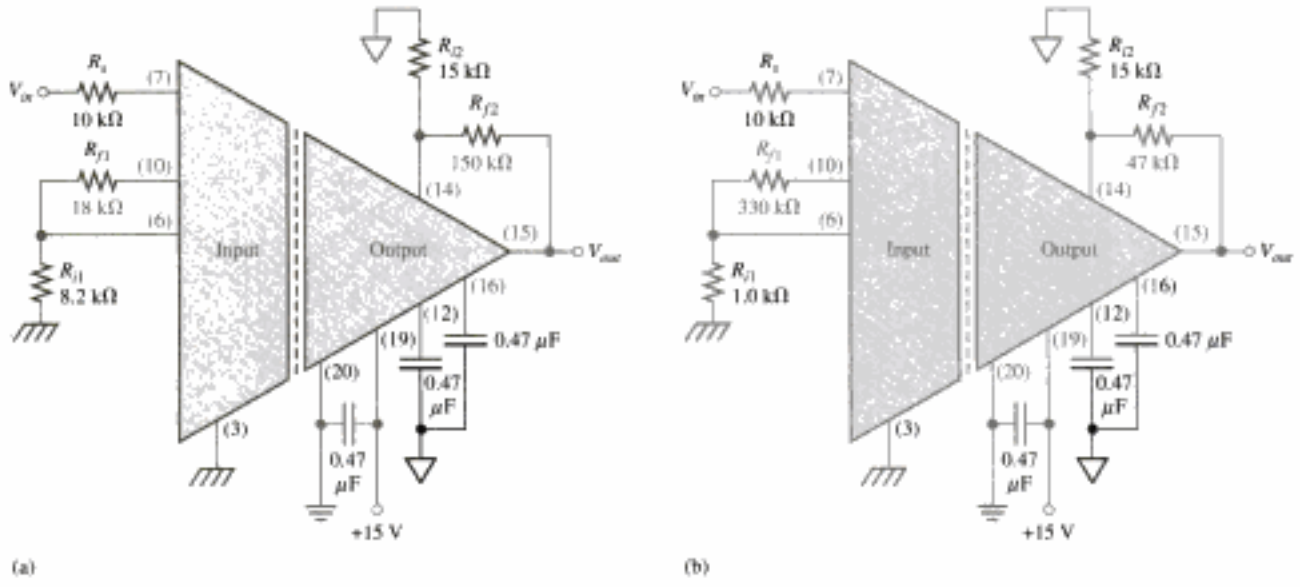
► FIGURE 14–38



6. Determine the approximate bandwidth of the amplifier in Figure 14–38 if the voltage gain is set to 10. Use the graph in Figure 14–6.
7. Specify what you must do to change the gain of the amplifier in Figure 14–38 to approximately 24.
8. Determine the value of R_G in Figure 14–38 for a voltage gain of 20.

SECTION 14–2 Isolation Amplifiers

9. The op-amp in the input stage of a certain isolation amplifier has a voltage gain of 30. The output stage is set for a gain of 10. What is the total voltage gain of this device?
10. Determine the total voltage gain of each 3656 KG in Figure 14–39.



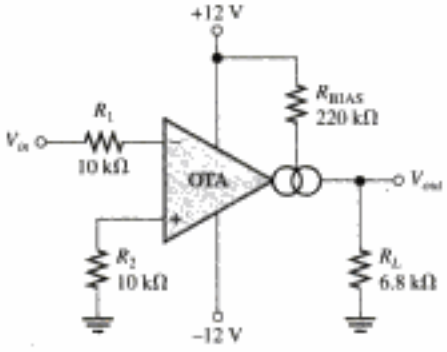
▲ FIGURE 14–39

11. Specify how you would change the total gain of the amplifier in Figure 14–39(a) to approximately 100 by changing only the gain of the input stage.
12. Specify how you would change the total gain in Figure 14–39(b) to approximately 440 by changing only the gain of the output stage.
13. Specify how you would connect each amplifier in Figure 14–39 for unity gain.

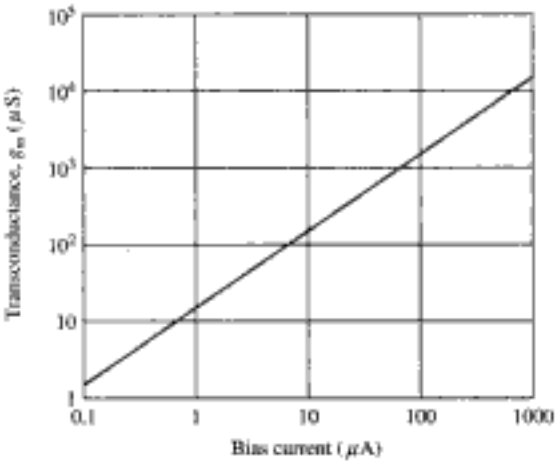
SECTION 14–3 Operational Transconductance Amplifiers (OTAs)

14. A certain OTA has an input voltage of 10 mV and an output current of 10 μA. What is the transconductance?
15. A certain OTA with a transconductance of 5000 μS has a load resistance of 10 kΩ. If the input voltage is 100 mV, what is the output current? What is the output voltage?
16. The output voltage of a certain OTA with a load resistance is determined to be 3.5 V. If its transconductance is 4000 μS and the input voltage is 100 mV, what is the value of the load resistance?
17. Determine the voltage gain of the OTA in Figure 14–40. Assume $K = 16\ \mu S/\mu A$ for the graph in Figure 14–41.

▶ FIGURE 14–40



► FIGURE 14–41



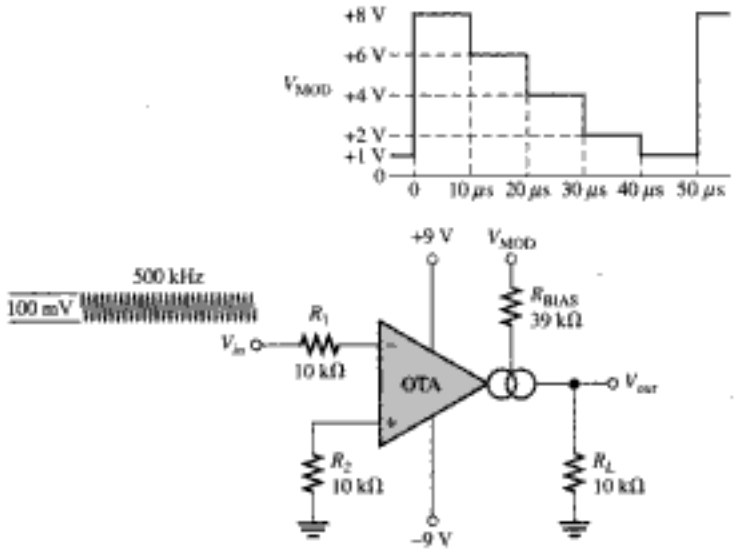
18. If a 10 kΩ rheostat is added in series with the bias resistor in Figure 14–40, what are the minimum and maximum voltage gains?

19. The OTA in Figure 14–42 functions as an amplitude modulation circuit. Determine the output voltage waveform for the given input waveforms assuming $K = 16\ \mu S/\mu A$.

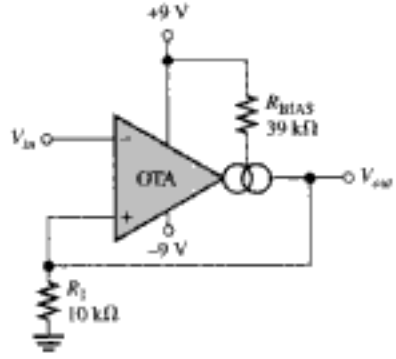
20. Determine the trigger points for the Schmitt trigger in Figure 14–43.

21. Determine the output voltage waveform for the Schmitt trigger in Figure 14–43 in relation to a 1 kHz sine wave with peak values of ±10 V.

► FIGURE 14–42



► FIGURE 14–43



SECTION 14–4 Log and Antilog Amplifiers

22. Using your calculator, find the natural logarithm (ln) of each of the following numbers:
(a) 0.5 **(b)** 2 **(c)** 50 **(d)** 130

23. Repeat Problem 22 for $\log_{10}$.

24. What is the antilog of 1.6?

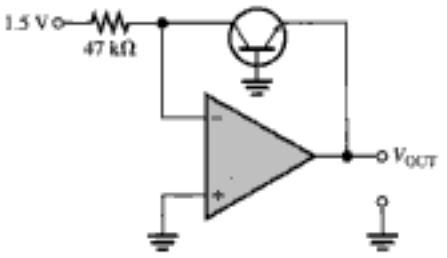
25. Explain why the output of a log amplifier is limited to approximately 0.7 V.

26. What is the output voltage of a certain log amplifier with a diode in the feedback path when the input voltage is 3 V? The input resistor is 82 kΩ and the reverse leakage current is 100 nA.

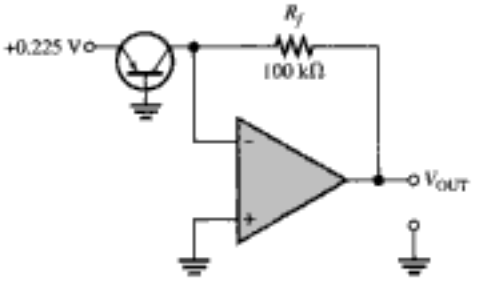
27. Determine the output voltage for the log amplifier in Figure 14–44. Assume $I_{RBO} = 60$ nA.

28. Determine the output voltage for the antilog amplifier in Figure 14–45. Assume $I_{RBO} = 60$ nA.

► **FIGURE 14–44**



► **FIGURE 14–45**

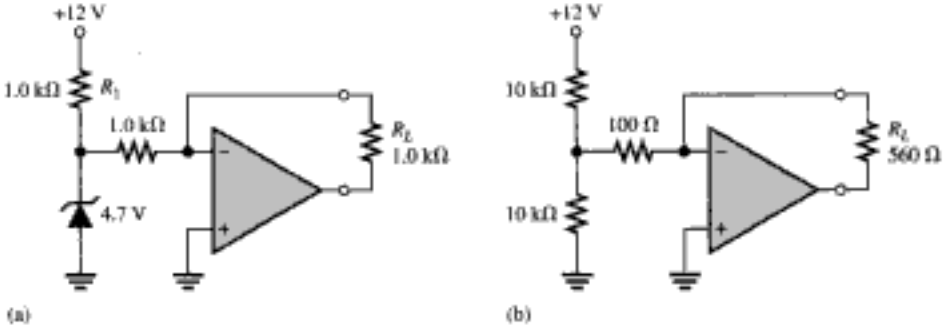


29. Signal compression is one application of logarithmic amplifiers. Suppose an audio signal with a maximum voltage of 1 V and a minimum voltage of 100 mV is applied to the log amplifier in Figure 14–44. What will be the maximum and minimum output voltages? What conclusion can you draw from this result?

SECTION 14–5 Converters and Other Op-Amp Circuits

30. Determine the load current in each circuit of Figure 14–46.

31. Devise a circuit for remotely sensing temperature and producing a proportional voltage that can then be converted to digital form for display. A thermistor can be used as the temperature-sensing element.



▲ **FIGURE 14–46**

ANSWERS

SECTION REVIEWS

SECTION 14–1 Instrumentation Amplifiers

1. The main purpose of an instrumentation amplifier is to amplify small signals that occur on large common-mode voltages. The key characteristics are high input impedance, high CMRR, low output impedance, and low output offset.
2. Three op-amps and seven resistors including the gain resistor are required to construct a basic instrumentation amplifier (see Figure 14–2).
3. The gain is set by the external resistor R_G.
4. The gain is approximately 6.

SECTION 14–2 Isolation Amplifiers

1. Isolation amplifiers are used in medical equipment, power plant instrumentation, industrial processing, and automated testing.
2. The two stages of an isolation amplifier are input and output and their purpose is isolation.
3. The stages are connected by capacitive, optical, or transformer coupling.
4. The oscillator is used for modulation.

SECTION 14–3 Operational Transconductance Amplifiers (OTAs)

1. OTA stands for Operational Transconductance Amplifier.
2. Transconductance increases with bias current.
3. Assuming that the bias input is connected to the supply voltage, the voltage gain increases when the supply voltage is increased because this increases the bias current.
4. The voltage gain decreases as the bias voltage decreases.

SECTION 14–4 Log and Antilog Amplifiers

1. A diode or transistor in the feedback loop provides the exponential (nonlinear) characteristic.
2. The output of a log amplifier is limited to the barrier potential of the *pn* junction (about 0.7 V).
3. The output voltage is determined by the input voltage, the input resistor, and the emitter-to-base leakage current.
4. The transistor in an antilog amplifier is in series with the input rather than in the feedback loop.

SECTION 14–5 Converters and Other Op-Amp Circuits

1. $I_L = 6.8\text{ V}/10\text{ k}\Omega = 0.68\text{ mA}$; same value to 5 kΩ load.
2. The feedback resistor is the constant of proportionality.

OBJECTIVE TYPE QUESTIONS

1. (b) **2.** (c) **3.** (b) **4.** (a) **5.** (c) **6.** (b) **7.** (a) **8.** (a) **9.** (d) **10.** (b)
11. (a) **12.** (e) **13.** (c) **14.** (b) **15.** (a) **16.** (c) **17.** (d) **18.** (c) **19.** (a) **20.** (b)
21. (f) **22.** (b)

15

ACTIVE FILTERS

CHAPTER OUTLINE

INTRODUCTION

Power supply filters were introduced in Chapter 2. In this chapter, active filters that are used for signal processing are introduced. Filters are circuits that are capable of passing signals with certain selected frequencies while rejecting signals with other frequencies. This property is called *selectivity*.

Active filters use transistors or op-amps combined with passive *RC*, *RL*, or *RLC* circuits. The active devices provide voltage gain, and the passive circuits provide frequency selectivity. In terms of general response, the four basic categories of active filters are low-pass, high-pass, band-pass, and band-stop. In this chapter, you will study active filters using op-amps and *RC* circuits.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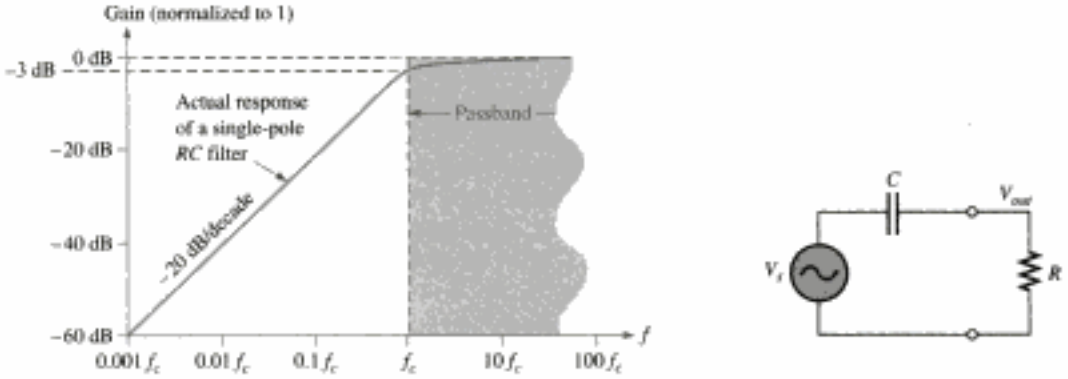
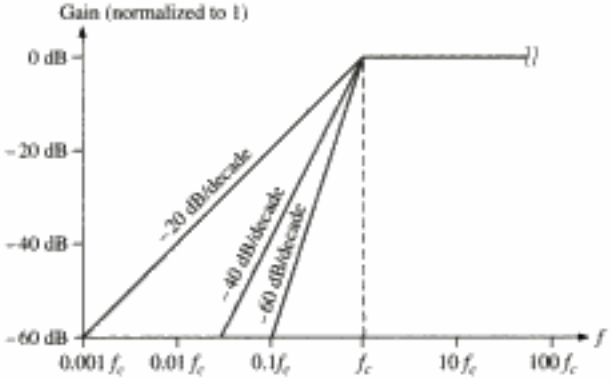


(a) Comparison of an ideal high-pass filter response (gray area) with actual response

(b) Basic high-pass circuit



(c) Idealized high-pass filter responses

▲ FIGURE 15–2

High-pass filter responses.

Band-Pass Filter Response

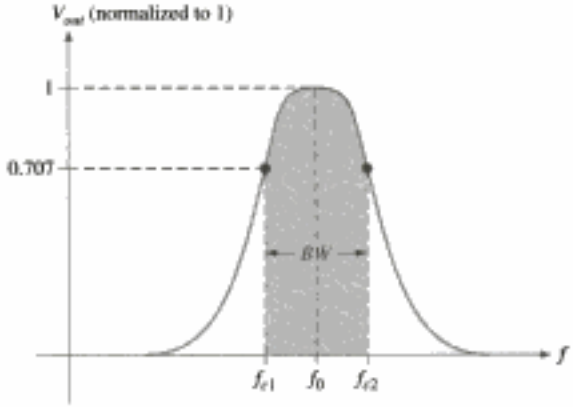
A **band-pass filter** passes all signals lying within a band between a lower-frequency limit and an upper-frequency limit and essentially rejects all other frequencies that are outside this specified band. A generalized band-pass response curve is shown in Figure 15–3. The bandwidth (BW) is defined as the difference between the upper critical frequency (f_{c2}) and the lower critical frequency (f_{c1}).

Equation 15–2

$$BW = f_{c2} - f_{c1}$$

▶ FIGURE 15–3

General band-pass response curve.



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EXAMPLE 15–2

If resistor R_2 in the feedback circuit of an active two-pole filter of the type in Figure 15–6 is 10 kΩ, what value must R_1 be to obtain a maximally flat Butterworth response?

Solution

$$\frac{R_1}{R_2} = 0.586$$

$$R_1 = 0.586R_2 = 0.586(10\,\text{k}\Omega) = \mathbf{5.86\ k\Omega}$$

Using the nearest standard 5 percent value of 5.6 kΩ will get very close to the ideal Butterworth response.

Critical Frequency and Roll-Off Rate

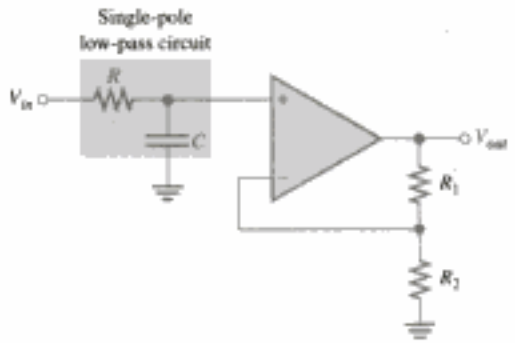
The critical frequency is determined by the values of the resistors and capacitors in the frequency-selective *RC* circuit shown in Figure 15–6. For a single-pole (first-order) filter, as shown in Figure 15–7, the critical frequency is

$$f_c = \frac{1}{2\pi RC}$$

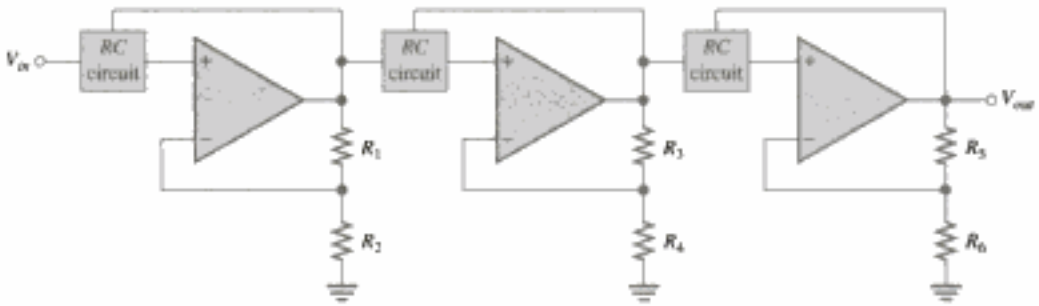
Although we show a low-pass configuration, the same formula is used for the f_c of a single-pole high-pass filter. The number of poles determines the roll-off rate of the filter. A Butterworth response produces −20 dB/decade/pole. So, a first-order (one-pole) filter has a roll-off of −20 dB/decade; a second-order (two-pole) filter has a roll-off rate of −40 dB/decade; a third-order (three-pole) filter has a roll-off rate of −60 dB/decade; and so on.

▶ FIGURE 15–7

First-order (one-pole) low-pass filter.



Generally, to obtain a filter with three poles or more, one-pole or two-pole filters are cascaded, as shown in Figure 15–8. To obtain a third-order filter, for example, cascade a second-order and a first-order filter; to obtain a fourth-order filter, cascade two second-order filters; and so on. Each filter in a cascaded arrangement is called a *stage* or *section*.



▲ FIGURE 15–8

The number of filter poles can be increased by cascading.

Because of its maximally flat response, the Butterworth characteristic is the most widely used. Therefore, we will limit our coverage to the Butterworth response to illustrate basic filter concepts. Table 15–1 lists the roll-off rates, damping factors, and feedback resistor ratios for up to sixth-order Butterworth filters. Resistor designations correspond to the gain-setting resistors in Figure 15–8 and may be different on other circuit diagrams.

▼ TABLE 15–1

Values for the Butterworth response.

ORDER	ROLL-OFF DB/DECADE	1ST STAGE			2ND STAGE			3RD STAGE		
		POLES	*DF*	R_1/R_2	POLES	*DF*	R_3/R_4	POLES	*DF*	R_5/R_6
1	−20	1	Optional							
2	−40	2	1.414	0.586						
3	−60	2	1.00	1	1	1.00	1			
4	−80	2	1.848	0.152	2	0.765	1.235			
5	−100	2	1.00	1	2	1.618	0.382	1	0.618	1.382
6	−120	2	1.932	0.068	2	1.414	0.586	2	0.518	1.482

SECTION 15–2 REVIEW

1. Explain how Butterworth, Chebyshev, and Bessel responses differ.
2. What determines the response characteristic of a filter?
3. Name the basic parts of an active filter.

15–3 ACTIVE LOW-PASS FILTERS

Filters that use op-amps as the active element provide several advantages over passive filters (*R*, *L*, and *C* elements only). The op-amp provides gain, so the signal is not attenuated as it passes through the filter. The high input impedance of the op-amp prevents excessive loading of the driving source, and the low output impedance of the op-amp prevents the filter from being affected by the load that it is driving. Active filters are also easy to adjust over a wide frequency range without altering the desired response.

A Single-Pole Filter

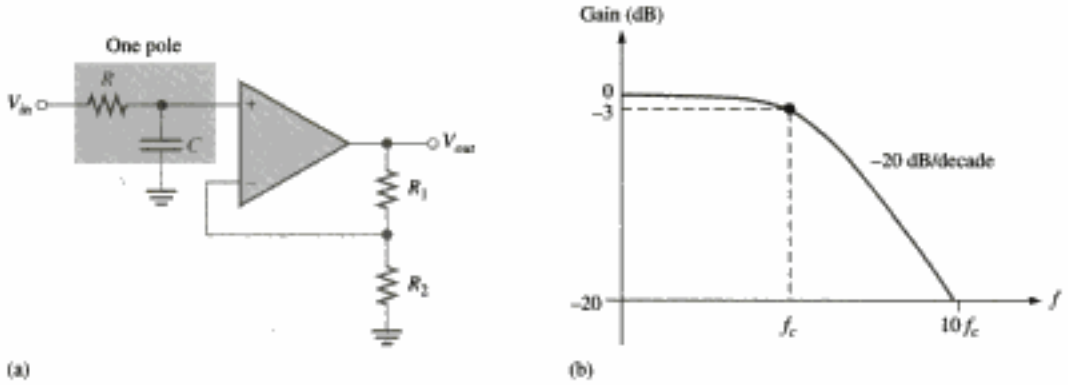
Figure 15–9(a) shows an active filter with a single low-pass *RC* frequency-selective circuit that provides a roll-off of −20 dB/decade above the critical frequency, as indicated by the response curve in Figure 15–9(b). The critical frequency of the single-pole filter is $f_c = 1/(2\pi RC)$. The op-amp in this filter is connected as a noninverting amplifier with the closed-loop voltage gain in the passband set by the values of R_1 and R_2.

$$A_{cl(NI)} = \frac{R_1}{R_2} + 1$$

Equation 15–6

The Sallen-Key Low-Pass Filter

The Sallen-Key is one of the most common configurations for a second-order (two-pole) filter. It is also known as a VCVS (voltage-controlled voltage source) filter. A low-pass



▲ FIGURE 15–9

Single-pole active low-pass filter and response curve.

version of the Sallen-Key filter is shown in Figure 15–10. Notice that there are two low-pass *RC* circuits that provide a roll-off of −40 dB/decade above the critical frequency (assuming a Butterworth characteristic). One *RC* circuit consists of R_A and C_A, and the second circuit consists of R_B and C_B. A unique feature of the Sallen-Key low-pass filter is the capacitor C_A that provides feedback for shaping the response near the edge of the passband. The critical frequency for the Sallen-Key filter is

$$f_c = \frac{1}{2\pi\sqrt{R_A R_B C_A C_B}}$$

The component values can be made equal so that $R_A = R_B = R$ and $C_A = C_B = C$. In this case, the expression for the critical frequency simplifies to

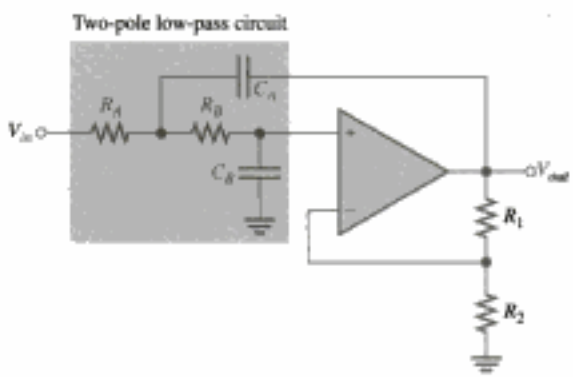
Equation 15–7

$$f_c = \frac{1}{2\pi RC}$$

As in the single-pole filter, the op-amp in the second-order Sallen-Key filter acts as a non inverting amplifier with the negative feedback provided by resistors R_1 and R_2. As you have learned, the damping factor is set by the values of R_1 and R_2, thus making the filter response either Butterworth, Chebyshev, or Bessel. For example, from Table 15–1, the R_1/R_2 ratio must be 0.586 to produce the damping factor of 1.414 required for a second-order Butterworth response.

► FIGURE 15–10

Basic Sallen-Key low-pass filter.



EXAMPLE 15–3

Determine the critical frequency of the Sallen-Key low-pass filter in Figure 15–11, and set the value of R_1 for an approximate Butterworth response.

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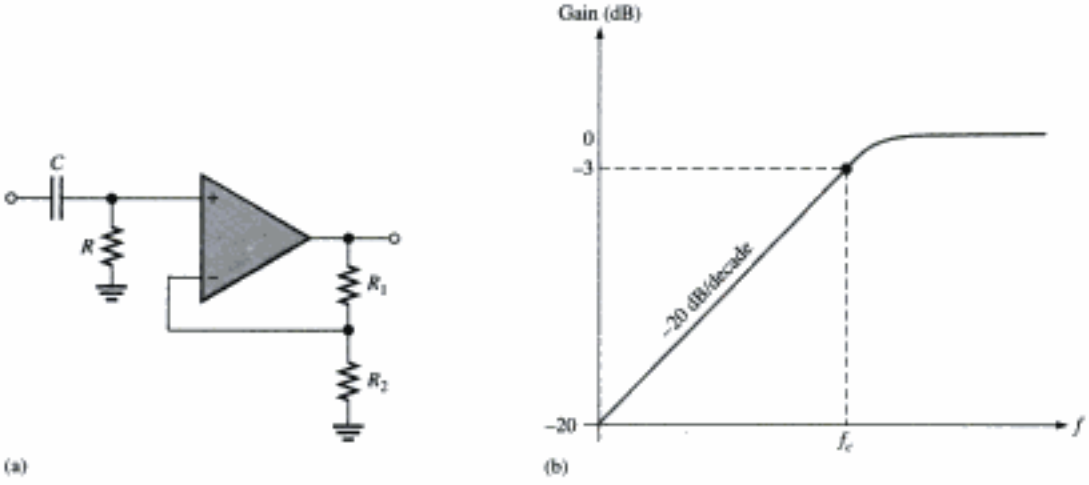
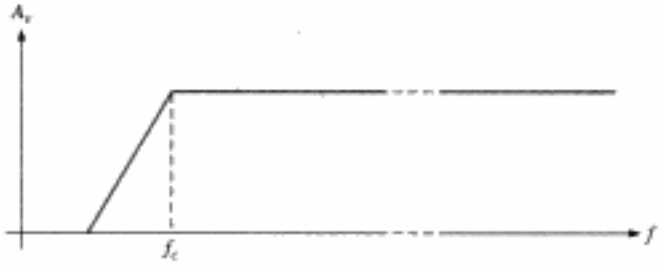
low-pass configuration. As with the other filters, the response characteristic can be optimized by proper selection of the feedback resistors, R_1 and R_2.



▲ FIGURE 15–13

Single-pole active high-pass filter and response curve.

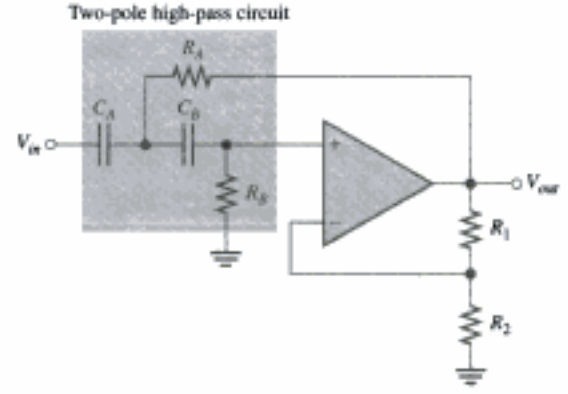


(a) Ideal

(b) Nonideal

◀ FIGURE 15–14

High-pass filter response.



◀ FIGURE 15–15

Basic Sallen-Key high-pass filter.

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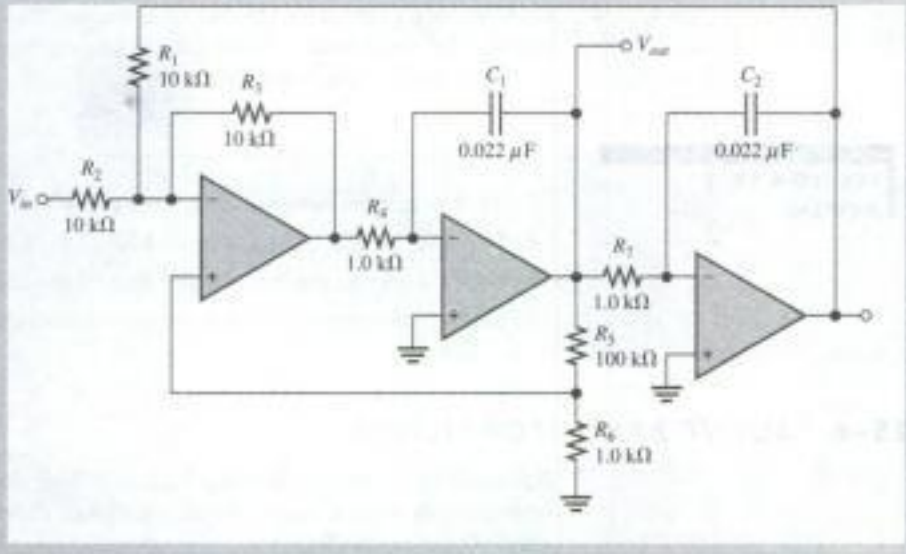
► FIGURE 15–22



Solution For each integrator,

$$f_c = \frac{1}{2\pi R_4 C_1} = \frac{1}{2\pi R_7 C_2} = \frac{1}{2\pi(1.0\text{ k}\Omega)(0.022\ \mu\text{F})} = 7.23\text{ kHz}$$

The center frequency is approximately equal to the critical frequencies of the integrators.

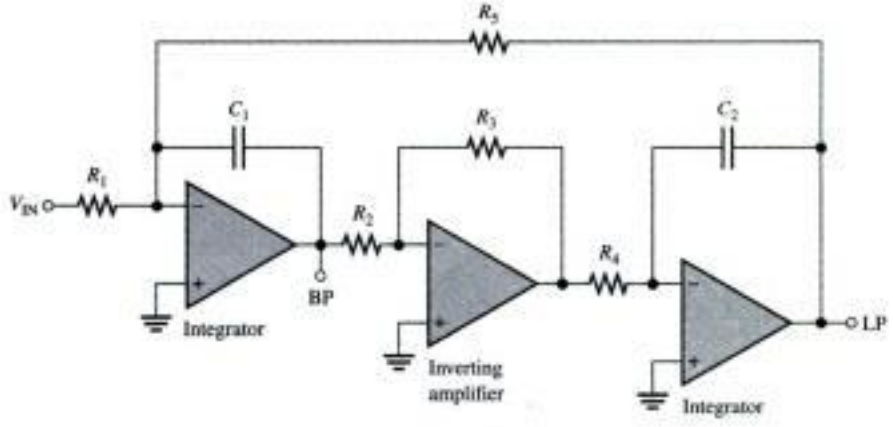
$$f_0 = f_c = \mathbf{7.23\ kHz}$$

$$Q = \frac{1}{3}\left(\frac{R_5}{R_6} + 1\right) = \frac{1}{3}\left(\frac{100\text{ k}\Omega}{1.0\text{ k}\Omega} + 1\right) = \mathbf{33.7}$$

$$BW = \frac{f_0}{Q} = \frac{7.23\text{ kHz}}{33.7} = \mathbf{215\ Hz}$$

The Biquad Filter

The biquad filter is similar to the state-variable filter except that it consists of an integrator, followed by an inverting amplifier, and then another integrator, as shown in Figure 15–23. These differences in the configuration between a biquad and a state-variable filter result in some operational differences although both allow a very high Q value. The major difference



◄ FIGURE 15–23

A biquad filter.

is that, in a biquad filter, the bandwidth is independent and the Q is dependent on the critical frequency. In the state-variable filter it is just the opposite: the bandwidth is dependent and the Q is independent on the critical frequency. Also, the biquad filter provides only band-pass and low-pass outputs.

SECTION 15–5 REVIEW

1. What determines selectivity in a band-pass filter?
2. One filter has a $Q = 5$ and another has a $Q = 25$. Which has the narrower bandwidth?
3. List the active elements that make up a state-variable filter.
4. List the active elements that make up a biquad filter.

15–6 ACTIVE BAND-STOP FILTERS

Band-stop filters reject a specified band of frequencies and pass all others. The response is opposite to that of a band-pass filter. Band-stop filters are sometimes referred to as notch filters.

Multiple-Feedback Band-Stop Filter

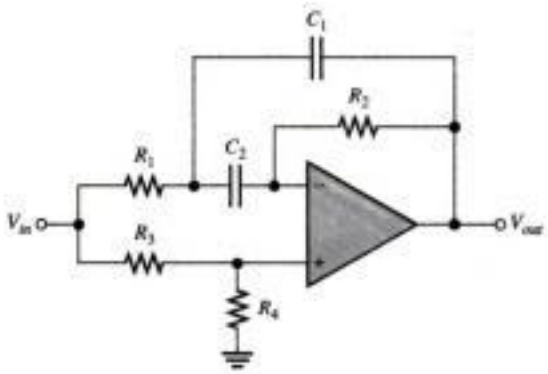
Figure 15–24 shows a multiple-feedback band-stop filter. Notice that this configuration is similar to the band-pass version in Figure 15–18 except that R_3 has been moved and R_4 has been added.

State-Variable Band-Stop Filter

Summing the low-pass and the high-pass responses of the state-variable filter covered in Section 15–5 with a summing amplifier creates a band-stop filter, as shown in Figure 15–25. One important application of this filter is minimizing the 60 Hz "hum" in audio systems by setting the center frequency to 60 Hz.

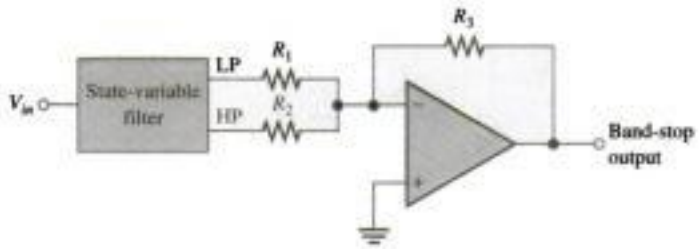
▶ FIGURE 15–24

Multiple-feedback band-stop filter.



▶ FIGURE 15–25

State-variable band-stop filter.

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15–7 FILTER RESPONSE MEASUREMENTS

In this section, we discuss two methods of determining a filter's response by measurement—discrete point measurement and swept frequency measurement.

- **Discuss two methods for measuring frequency response**
- Explain the discrete point measurement method
- Explain the swept frequency measurement method

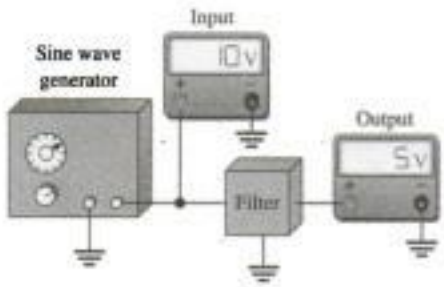
Discrete Point Measurement

Figure 15–27 shows an arrangement for taking filter output voltage measurements at discrete values of input frequency using common laboratory instruments. The general procedure is as follows:

1. Set the amplitude of the sine wave generator to a desired voltage level.
2. Set the frequency of the sine wave generator to a value well below the expected critical frequency of the filter under test. For a low-pass filter, set the frequency as near as possible to 0 Hz. For a band-pass filter, set the frequency well below the expected lower critical frequency.
3. Increase the frequency in predetermined steps sufficient to allow enough data points for an accurate response curve.
4. Maintain a constant input voltage amplitude while varying the frequency.

▶ FIGURE 15–27

Test setup for discrete point measurement of the filter response. (Readings are arbitrary and for display only.)

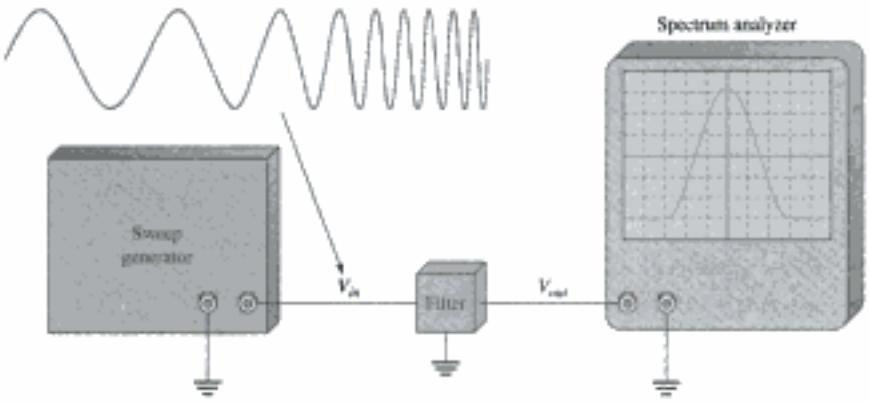


5. Record the output voltage at each value of frequency.
6. After recording a sufficient number of points, plot a graph of output voltage versus frequency.

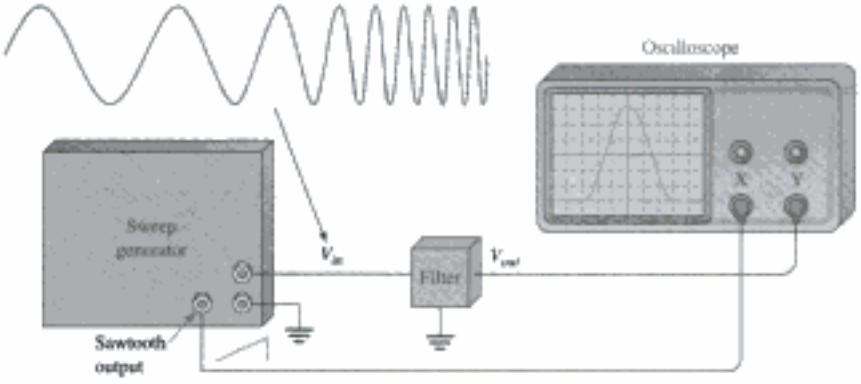
If the frequencies to be measured exceed the frequency response of the DMM, an oscilloscope may have to be used instead.

Swept Frequency Measurement

The swept frequency method requires more elaborate test equipment than does the discrete point method, but it is much more efficient and can result in a more accurate response curve. A general test setup is shown in Figure 15–28(a) using a swept frequency generator and a spectrum analyzer. Figure 15–28(b) shows how the test can be made with an oscilloscope.



(a) Test setup for a filter response using a spectrum analyzer



(b) Test setup for a filter response using an oscilloscope. The scope is put in X-Y mode. The sawtooth waveform from the sweep generator drives the X-channel of the oscilloscope.

◀ FIGURE 15–28

Test setup for swept frequency measurement of the filter response.

The swept frequency generator produces a constant amplitude output signal whose frequency increases linearly between two preset limits, as indicated in Figure 15–28. The spectrum analyzer is essentially an elaborate oscilloscope that can be calibrated for a desired *frequency span/division* rather than for the usual *time/division* setting. Therefore, as the input frequency to the filter sweeps through a preselected range, the response curve is traced out on the screen of the spectrum analyzer or an oscilloscope.

SECTION 15–7 REVIEW

1. What is the purpose of the two tests discussed in this section?
2. Name one disadvantage and one advantage of each test method.

CHAPTER SUMMARY

- The bandwidth in a low-pass filter equals the critical frequency because the response extends to 0 Hz.
- The bandwidth in a high-pass filter extends above the critical frequency and is limited only by the inherent frequency limitation of the active circuit.
- A band-pass filter passes all frequencies within a band between a lower and an upper critical frequency and rejects all others outside this band.
- The bandwidth of a band-pass filter is the difference between the upper critical frequency and the lower critical frequency.
- A band-stop filter rejects all frequencies within a specified band and passes all those outside this band.

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14. The damping factor of an active filter determines
(a) the voltage gain **(b)** the critical frequency
(c) the response characteristic **(d)** the roll-off rate

15. A maximally flat frequency response is known as
(a) Chebyshev **(b)** Butterworth **(c)** Bessel **(d)** Colpitts

16. The damping factor of a filter is set by
(a) the negative feedback circuit **(b)** the positive feedback circuit
(c) the frequency-selective circuit **(d)** the gain of the op-amp

17. The number of poles in a filter affect the
(a) voltage gain **(b)** bandwidth **(c)** center frequency **(d)** roll-off rate

18. Sallen-Key filters are
(a) single-pole filters **(b)** second-order filters
(c) Butterworth filters **(d)** band-pass filters

19. When filters are cascaded, the roll-off rate
(a) increases **(b)** decreases **(c)** does not change

20. When a low-pass and a high-pass filter are cascaded to get a band-pass filter, the critical frequency of the low-pass filter must be
(a) equal to the critical frequency of the high-pass filter
(b) less than the critical frequency of the high-pass filter
(c) greater than the critical frequency of the high-pass filter

21. A state-variable filter consists of
(a) one op-amp with multiple-feedback paths
(b) a summing amplifier and two integrators
(c) a summing amplifier and two differentiators
(d) three Butterworth stages

22. When the gain of a filter is minimum at its center frequency, it is
(a) a band-pass filter **(b)** a band-stop filter
(c) a notch filter **(d)** answers (b) and (c)

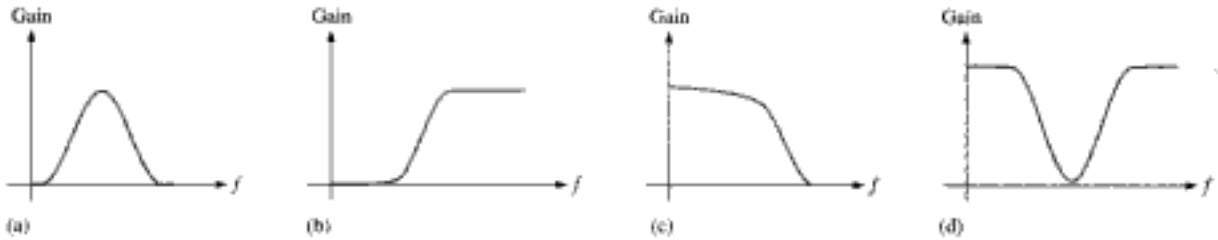
PROBLEMS

Answers to all selected problems are at the end of the book.

BASIC PROBLEMS

SECTION 15–1 Basic Filter Responses

1. Identify each type of filter response (low-pass, high-pass, band-pass, or band-stop) in Figure 15–27.



▲ **FIGURE 15–27**

2. A certain low-pass filter has a critical frequency of 800 Hz. What is its bandwidth?

3. A single-pole high-pass filter has a frequency-selective circuit with $R = 2.2\ \text{k}\Omega$ and $C = 0.0015\ \mu\text{F}$. What is the critical frequency? Can you determine the bandwidth from the available information?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SECTION 15–3 Active Low-Pass Filters

10. Is the four-pole filter in Figure 15–30 approximately optimized for a Butterworth response? What is the roll-off rate?

11. Determine the critical frequency in Figure 15–30.

12. Without changing the response curve, adjust the component values in the filter of Figure 15–30 to make it an equal-value filter. Select $C = 0.22\ \mu F$ for both stages.

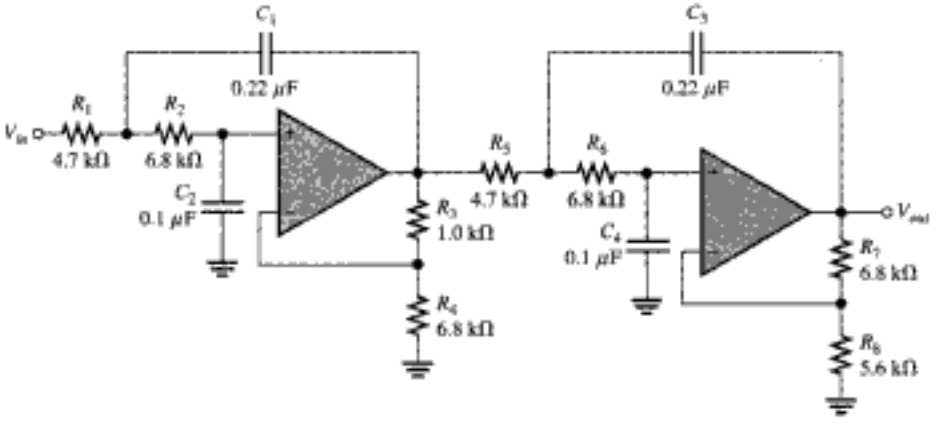
13. Modify the filter in Figure 15–30 to increase the roll-off rate to −120 dB/decade while maintaining an approximate Butterworth response.

14. Using a block diagram format, show how to implement the following roll-off rates using single-pole and two-pole low-pass filters with Butterworth responses.

(a) −40 dB/decade **(b)** −20 dB/decade

(c) −60 dB/decade **(d)** −100 dB/decade

(e) −120 dB/decade



▲ **FIGURE 15–30**

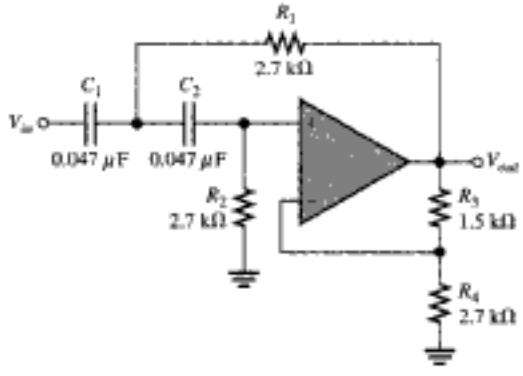
SECTION 15–4 Active High-Pass Filters

15. Convert the filter in Problem 12 to a high-pass with the same critical frequency and response characteristic.

16. Make the necessary circuit modification to reduce by half the critical frequency in Problem 15.

17. For the filter in Figure 15–31, **(a)** how would you increase the critical frequency? **(b)** How would you increase the gain?

▶ **FIGURE 15–31**

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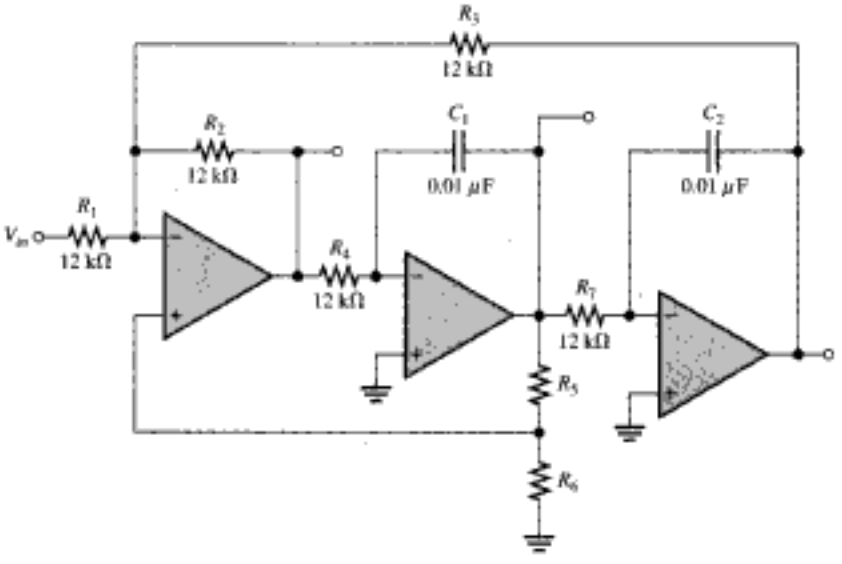
20. Optimize the state-variable filter in Figure 15–33 for $Q = 50$. What bandwidth is achieved?

▶ **FIGURE 15–33**



SECTION 15–6 Active Band-Stop Filters

21. Show how to make a notch (band-stop) filter using the basic circuit in Figure 15–33.

22. Modify the band-stop filter in Problem 21 for a center frequency of 120 Hz.

ANSWERS

SECTION REVIEWS

SECTION 15–1 Basic Filter Responses

1. The critical frequency determines the bandwidth.
2. The inherent frequency limitation of the op-amp limits the bandwidth.
3. Q and BW are inversely related. The higher the Q, the better the selectivity, and vice versa.

SECTION 15–2 Filter Response Characteristics

1. Butterworth is very flat in the passband and has a −20 dB/decade/pole roll-off. Chebyshev has ripples in the passband and has greater than −20 dB/decade/pole roll-off. Bessel has a linear phase characteristic and less than −20 dB/decade/pole roll-off.
2. The damping factor
3. Frequency-selective circuit, gain element, and negative feedback circuit are the parts of an active filter.

SECTION 15–3 Active Low-Pass Filters

1. A second-order filter has two poles. Two resistors and two capacitors make up the frequency-selective circuit.
2. The damping factor sets the response characteristic.
3. Cascading increases the roll-off rate.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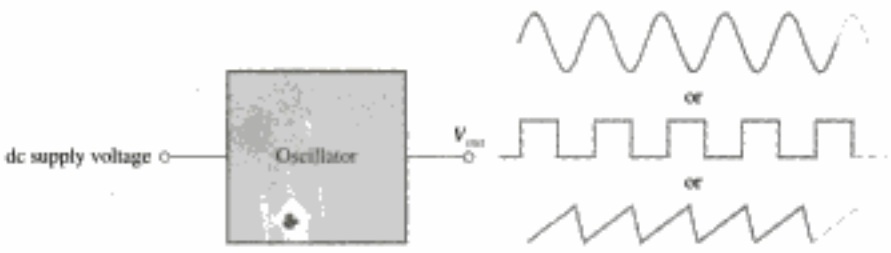
16–1 THE OSCILLATOR

An oscillator is a circuit that produces a periodic waveform on its output with only the dc supply voltage as an input. A repetitive input signal is not required except to synchronize oscillations in some applications. The output voltage can be either sinusoidal or nonsinusoidal, depending on the type of oscillator. Two major classifications for oscillators are feedback oscillators and relaxation oscillators.

Essentially, an **oscillator** converts electrical energy from the dc power supply to periodic waveforms. A basic oscillator is shown in Figure 16–1.

▶ FIGURE 16–1

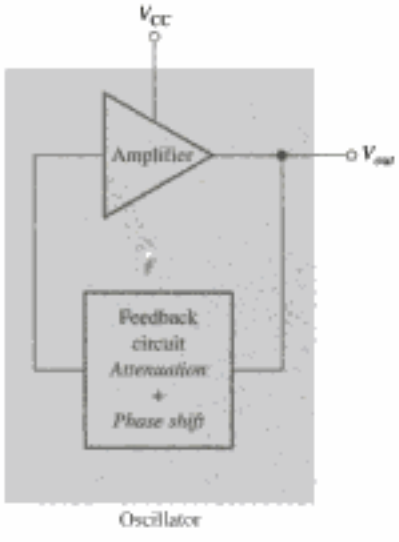
The basic oscillator concept showing three common types of output waveforms: sine wave, square wave, and sawtooth.



Feedback Oscillators One type of oscillator is the **feedback oscillator**, which returns a fraction of the output signal to the input with no net phase shift, resulting in a reinforcement of the output signal. After oscillations are started, the loop gain is maintained at 1.0 to maintain oscillations. A feedback oscillator consists of an amplifier for gain (either a discrete transistor or an op-amp) and a positive feedback circuit that produces phase shift and provides attenuation, as shown in Figure 16–2.

▶ FIGURE 16–2

Basic elements of a feedback oscillator.



Relaxation Oscillators A second type of oscillator is the **relaxation oscillator**. A relaxation oscillator uses an *RC* timing circuit to generate a waveform that is generally a square wave or other nonsinusoidal waveform. Typically, a relaxation oscillator uses a Schmitt trigger or other device that changes states to alternately charge and discharge a capacitor through a resistor.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SECTION 16–2 REVIEW

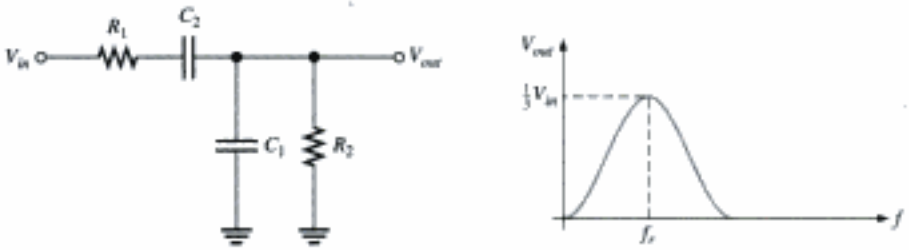
1. What are the conditions required for a circuit to oscillate?
2. Define *positive feedback*.
3. What is the voltage gain condition for oscillator start-up?

16–3 OSCILLATORS WITH *RC* FEEDBACK CIRCUITS

In this section, you will learn about three types of feedback oscillators that use *RC* circuits to produce sinusoidal outputs: the Wien-bridge oscillator, the phase-shift oscillator, and the twin-T oscillator. Generally, *RC* feedback oscillators are used for frequencies up to about 1 MHz. The Wien-bridge is by far the most widely used type of *RC* feedback oscillator for this range of frequencies.

The Wien-Bridge Oscillator

One type of sinusoidal feedback oscillator is the **Wien-bridge oscillator**. A fundamental part of the Wien-bridge oscillator is a lead-lag circuit like that shown in Figure 16–6(a). R_1 and C_1 together form the lag portion of the circuit; R_2 and C_2 form the lead portion. The operation of this lead-lag circuit is as follows. At lower frequencies, the lead circuit dominates due to the high reactance of C_2. As the frequency increases, X_{C2} decreases, thus allowing the output voltage to increase. At some specified frequency, the response of the lag circuit takes over, and the decreasing value of X_{C1} causes the output voltage to decrease.



(a) Circuit (b) Response curve

◀ **FIGURE 16–6**
A lead-lag circuit and its response curve.

The response curve for the lead-lag circuit shown in Figure 16–6(b) indicates that the output voltage peaks at a frequency called the resonant frequency, f_r. At this point, the attenuation (V_{out}/V_{in}) of the circuit is 1/3 if $R_1 = R_2$ and $X_{C1} = X_{C2}$ as stated by the following equation:

$$\frac{V_{out}}{V_{in}} = \frac{1}{3}$$ **Equation 16–1**

The formula for the resonant frequency (also derived in Appendix B) is

$$f_r = \frac{1}{2\pi RC}$$ **Equation 16–2**

To summarize, the lead-lag circuit in the Wien-bridge oscillator has a resonant frequency, f_r, at which the phase shift through the circuit is 0° and the attenuation is 1/3. Below f_r, the lead circuit dominates and the output leads the input. Above f_r, the lag circuit dominates and the output lags the input.

The Basic Circuit The lead-lag circuit is used in the positive feedback loop of an op-amp, as shown in Figure 16–7(a). A voltage divider is used in the negative feedback loop. The Wien-bridge oscillator circuit can be viewed as a noninverting amplifier configuration with

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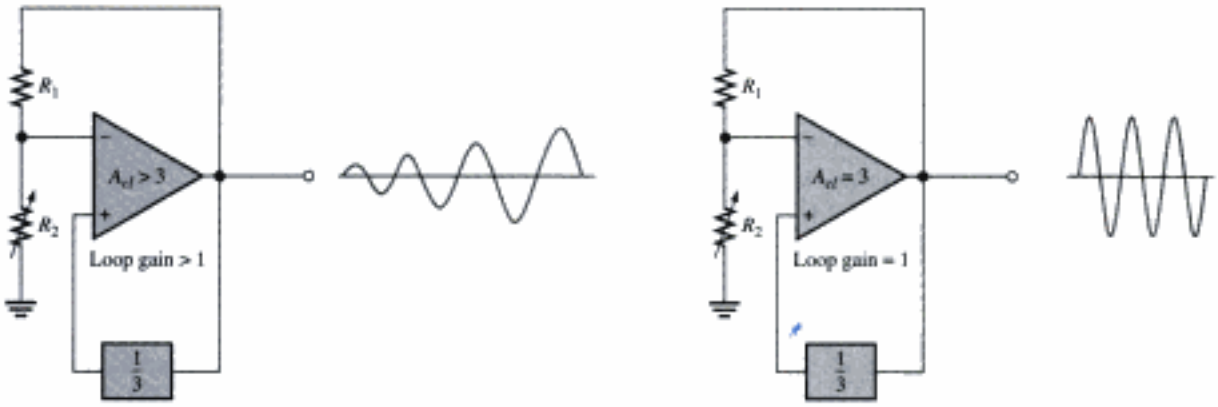
Then

$$A_{cl} = \frac{R_1 + R_2}{R_2} = \frac{2R_2 + R_2}{R_2} = \frac{3R_2}{R_2} = 3$$

Start-Up Conditions Initially, the closed-loop gain of the amplifier itself must be more than three ($A_{cl} > 3$) until the output signal builds up to a desired level. Ideally, the gain of the amplifier must then decrease to 3 so that the total gain around the loop is 1 and the output signal stays at the desired level, thus sustaining oscillation. This is illustrated in Figure 16–9.

The circuit in Figure 16–10 illustrates a method for achieving sustained oscillations. Notice that the voltage-divider circuit has been modified to include an additional resistor R_3 in parallel with a back-to-back zener diode arrangement. When dc power is first applied, both zener diodes appear as opens. This places R_3 in series with R_1, thus increasing the closed-loop gain of the amplifier as follows ($R_1 = 2R_2$):

$$A_{cl} = \frac{R_1 + R_2 + R_3}{R_2} = \frac{3R_2 + R_3}{R_2} = 3 + \frac{R_3}{R_2}$$

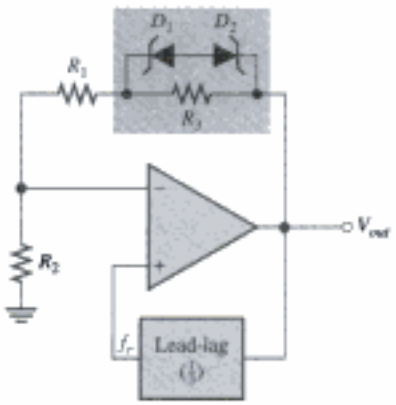


(a) Loop gain greater than 1 causes output to build up.

(b) Loop gain of 1 causes a sustained constant output.

▲ FIGURE 16–9

Conditions for start-up and sustained oscillations.



◀ FIGURE 16–10

Self-starting Wien-bridge oscillator using back-to-back zener diodes.

Initially, a small positive feedback signal develops from noise or turn-on transients. The lead-lag circuit permits only a signal with a frequency equal to f_r to appear in phase on the noninverting input. This feedback signal is amplified and continually reinforced, resulting in a buildup of the output voltage. When the output signal reaches the zener breakdown voltage, the zeners conduct and effectively short out R_3. This lowers the amplifier's closed-loop gain to 3. At this point, the total loop gain is 1 and the output signal levels off and the oscillation is sustained.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Solution For the lead-lag circuit, $R_1 = R_2 = R = 10\ \text{k}\Omega$ and $C_1 = C_2 = C = 0.01\ \mu\text{F}$. The frequency is

$$f_r = \frac{1}{2\pi RC} = \frac{1}{2\pi(10\ \text{k}\Omega)(0.01\ \mu\text{F})} = \mathbf{1.59\ kHz}$$

The closed-loop gain must be 3.0 for oscillations to be sustained. For an inverting amplifier, the gain is that of a noninverting amplifier.

$$A_v = \frac{R_f}{R_i} + 1$$

R_i is composed of R_3 (the source resistor) and r'_{ds}. Substituting,

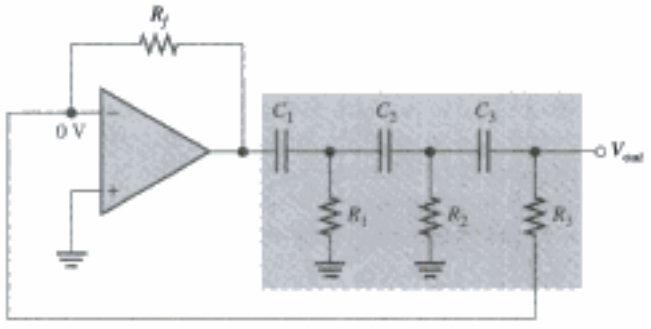
$$A_v = \frac{R_f}{R_3 + r'_{ds}} + 1$$

Rearranging and solving for R_f,

$$R_f = (A_v - 1)(R_3 + r'_{ds}) = (3 - 1)(1.0\ \text{k}\Omega + 500\ \Omega) = \mathbf{3.0\ k\Omega}$$

The Phase-Shift Oscillator

Figure 16–13 shows a sinusoidal feedback oscillator called the **phase-shift oscillator**. Each of the three *RC* circuits in the feedback loop can provide a *maximum* phase shift approaching 90°. Oscillation occurs at the frequency where the total phase shift through the three *RC* circuits is 180°. The inversion of the op-amp itself provides the additional 180° to meet the requirement for oscillation of a 360° (or 0°) phase shift around the feedback loop.



◀ **FIGURE 16–13**
Phase-shift oscillator.

The attenuation, B, of the three-section *RC* feedback circuit is

$$B = \frac{1}{29}$$

Equation 16–3

where $B = R_3/R_f$. To meet the greater-than-unity loop gain requirement, the closed-loop voltage gain of the op-amp must be greater than 29 (set by R_f and R_3). The frequency of oscillation (f_r) is stated in the following equation, where $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$.

$$f_r = \frac{1}{2\pi\sqrt{6}RC}$$

Equation 16–4

EXAMPLE 16–2

(a) Determine the value of R_f necessary for the circuit in Figure 16–14 to operate as an oscillator.

(b) Determine the frequency of oscillation.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where C_T is the total capacitance. Because the capacitors effectively appear in series around the tank circuit, the total capacitance (C_T) is

Equation 16–5

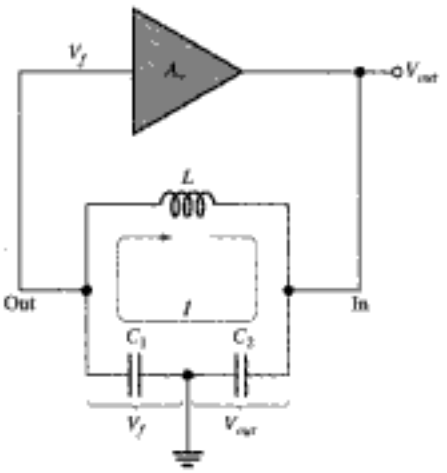
$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$

Conditions for Oscillation and Start-Up The attenuation, B, of the resonant feedback circuit in the Colpitts oscillator is basically determined by the values of C_1 and C_2.

Figure 16–17 shows that the circulating tank current is through both C_1 and C_2 (they are effectively in series). The voltage developed across C_2 is the oscillator's output voltage

▶ **FIGURE 16–17**

The attenuation of the tank circuit is the output of the tank (V_f) divided by the input to the tank (V_{out}). $B = V_f/V_{out} = C_2/C_1$. For $A_vB > 1$, A_v must be greater than C_1/C_2.



(V_{out}) and the voltage developed across C_1 is the feedback voltage (V_f), as indicated. The expression for the attenuation (B) is

$$B = \frac{V_f}{V_{out}} \cong \frac{IX_{C1}}{IX_{C2}} = \frac{X_{C1}}{X_{C2}} = \frac{1/(2\pi f_r C_1)}{1/(2\pi f_r C_2)}$$

Cancelling the $2\pi f_r$ terms gives

$$B = \frac{C_2}{C_1}$$

As you know, a condition for oscillation is $A_vB = 1$. Since $B = C_2/C_1$,

Equation 16–6

$$A_v = \frac{C_1}{C_2}$$

where A_v is the voltage gain of the amplifier, which is represented by the triangle in Figure 16–17. With this condition met, $A_vB = (C_1/C_2)(C_2/C_1) = 1$. Actually, for the oscillator to be self-starting, A_vB must be greater than 1 (that is, $A_vB > 1$). Therefore, the voltage gain must be made slightly greater than C_1/C_2.

$$A_v > \frac{C_1}{C_2}$$

Loading of the Feedback Circuit Affects the Frequency of Oscillation As indicated in Figure 16–18, the input impedance of the amplifier acts as a load on the resonant feedback circuit and reduces the Q of the circuit. Recall from your study of resonance that the resonant frequency of a parallel resonant circuit depends on the Q, according to the following formula:

Equation 16–7

$$f_r = \frac{1}{2\pi\sqrt{LC_T}}\sqrt{\frac{Q^2}{Q^2 + 1}}$$

As a rule of thumb, for a Q greater than 10, the frequency is approximately $1/(2\pi\sqrt{LC_T})$, as stated in Equation 16–5. When Q is less than 10, however, f_r is reduced significantly.

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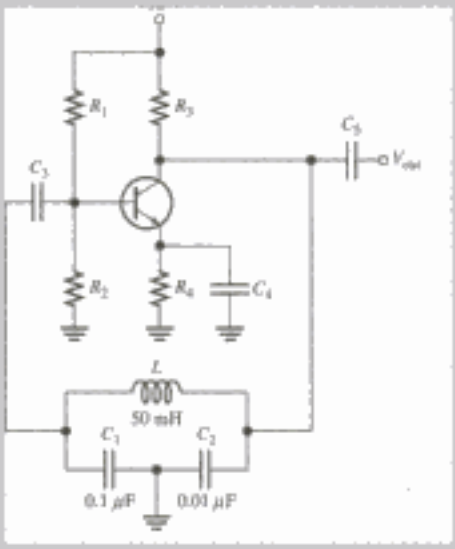
EXAMPLE 16–3

(a) Determine the frequency for the oscillator in Figure 16–21. Assume there is negligible loading on the feedback circuit and that its Q is greater than 10.

(b) Find the frequency if the oscillator is loaded to a point where the Q drops to 8.

► **FIGURE 16–21**



Solution

(a) $$C_T = \frac{C_1C_2}{C_1 + C_2} = \frac{(0.1\ \mu\text{F})(0.01\ \mu\text{F})}{0.11\ \mu\text{F}} = 0.0091\ \mu\text{F}$$

$$f_r \cong \frac{1}{2\pi\sqrt{LC_T}} = \frac{1}{2\pi\sqrt{(50\ \text{mH})(0.0091\ \mu\text{F})}} = \mathbf{7.46\ kHz}$$

(b) $$f_r = \frac{1}{2\pi\sqrt{LC_T}}\sqrt{\frac{Q^2}{Q^2 + 1}} = (7.46\ \text{kHz})(0.9923) = \mathbf{7.40\ kHz}$$

The Clapp Oscillator

The Clapp oscillator is a variation of the Colpitts. The basic difference is an additional capacitor, C_3, in series with the inductor in the resonant feedback circuit, as shown in Figure 16–22. Since C_3 is in series with C_1 and C_2 around the tank circuit, the total capacitance is

$$C_T = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}}$$

and the approximate frequency of oscillation ($Q > 10$) is

$$f_r \cong \frac{1}{2\pi\sqrt{LC_T}}$$

If C_3 is much smaller than C_1 and C_2, then C_3 almost entirely controls the resonant frequency ($f_r \cong 1/(2\pi\sqrt{LC_3})$). Since C_1 and C_2 are both connected to ground at one end, the junction capacitance of the transistor and other stray capacitances appear in parallel with C_1 and C_2 to ground, altering their effective values. C_3 is not affected, however, and thus provides a more accurate and stable frequency of oscillation.

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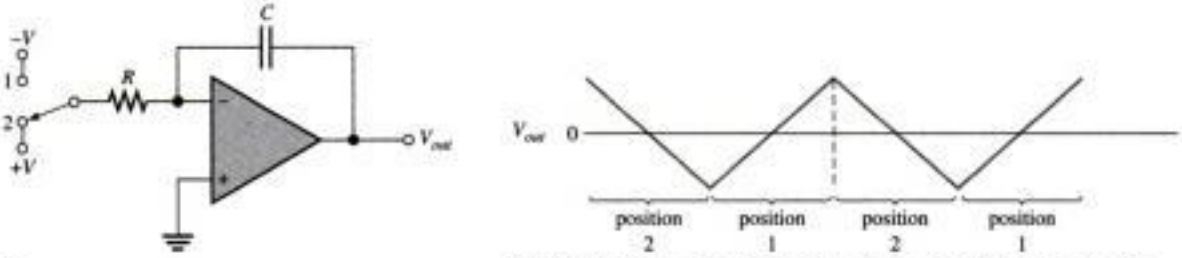
16–5 RELAXATION OSCILLATORS

The second major category of oscillators is the relaxation oscillator. Relaxation oscillators use an *RC* timing circuit and a device that changes states to generate a periodic waveform. In this section, you will learn about several circuits that are used to produce nonsinusoidal waveforms.

A Triangular-Wave Oscillator

The op-amp integrator can be used as the basis for a triangular-wave oscillator. The basic idea is illustrated in Figure 16–27(a) where a dual-polarity, switched input is used. We use the switch only to introduce the concept; it is not a practical way to implement this circuit. When the switch is in position 1, the negative voltage is applied, and the output is a positive-going ramp. When the switch is thrown into position 2, a negative-going ramp is produced. If the switch is thrown back and forth at fixed intervals, the output is a triangular wave consisting of alternating positive-going and negative-going ramps, as shown in Figure 16–27(b).



(a) (b) Output voltage as the switch is thrown back and forth at regular intervals

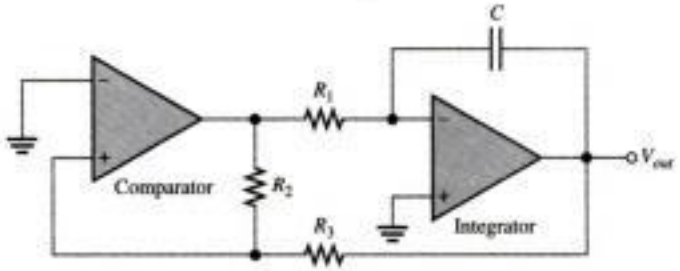
▲ FIGURE 16–27

Basic triangular-wave oscillator.

A Practical Triangular-Wave Oscillator One practical implementation of a triangular-wave oscillator utilizes an op-amp comparator to perform the switching function, as shown in Figure 16–28. The operation is as follows. To begin, assume that the output voltage of the comparator is at its maximum negative level. This output is connected to the inverting input

▶ FIGURE 16–28

A triangular-wave oscillator using two op-amps.



of the integrator through R_1, producing a positive-going ramp on the output of the integrator. When the ramp voltage reaches the upper trigger point (UTP), the comparator switches to its maximum positive level. This positive level causes the integrator ramp to change to a negative-going direction. The ramp continues in this direction until the lower trigger point (LTP) of the comparator is reached. At this point, the comparator output switches back to the maximum negative level and the cycle repeats. This action is illustrated in Figure 16–29.

Since the comparator produces a square-wave output, the circuit in Figure 16–28 can be used as both a triangular-wave oscillator and a square-wave oscillator. Devices of this type are commonly known as *function generators* because they produce more than one output

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(PUT) in parallel with the feedback capacitor to terminate each ramp at a prescribed level and effectively "reset" the circuit. Figure 16–31(a) shows the implementation.

The PUT is a programmable unijunction transistor with an anode, a cathode, and a gate terminal. The gate is always biased positively with respect to the cathode. When the anode voltage exceeds the gate voltage by approximately 0.7 V, the PUT turns on and acts as a forward-biased diode. When the anode voltage falls below this level, the PUT turns off. Also, the current must be above the holding value to maintain conduction.

The operation of the sawtooth VCO begins when the negative dc input voltage, $-V_{IN}$, produces a positive-going ramp on the output. During the time that the ramp is increasing, the circuit acts as a regular integrator. The PUT triggers on when the output ramp (at the anode) exceeds the gate voltage by 0.7 V. The gate is set to the approximate desired sawtooth peak voltage. When the PUT turns on, the capacitor rapidly discharges, as shown in Figure 16–31(b). The capacitor does not discharge completely to zero because of the PUT's forward voltage, V_F. Discharge continues until the PUT current falls below the holding value. At this point, the PUT turns off and the capacitor begins to charge again, thus generating a new output ramp. The cycle continually repeats, and the resulting output is a repetitive sawtooth waveform, as shown. The sawtooth amplitude and period can be adjusted by varying the PUT gate voltage.

The frequency of oscillation is determined by the R_iC time constant of the integrator and the peak voltage set by the PUT. Recall that the charging rate of a capacitor is V_{IN}/R_iC. The time it takes a capacitor to charge from V_F to V_p is the period, T, of the sawtooth waveform (neglecting the rapid discharge time).

$$T = \frac{V_p - V_F}{|V_{IN}|/R_iC}$$

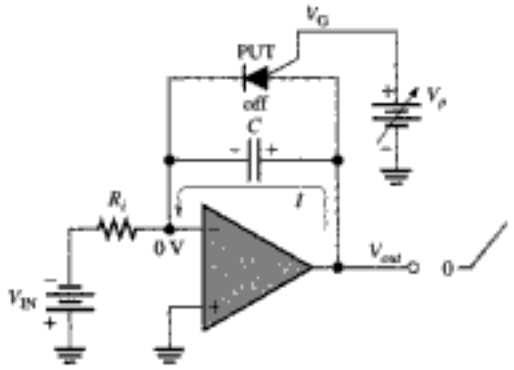
From $f = 1/T$,

Equation 16–11

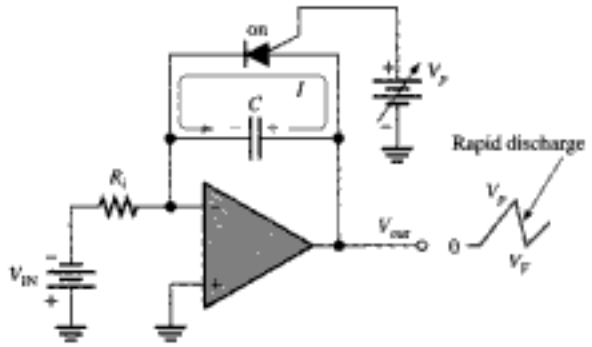
$$f = \frac{|V_{IN}|}{R_iC}\left(\frac{1}{V_p - V_F}\right)$$

► FIGURE 16–31

Sawtooth VCO operation.



(a) Initially, the capacitor charges, the output ramp begins, and the PUT is off.



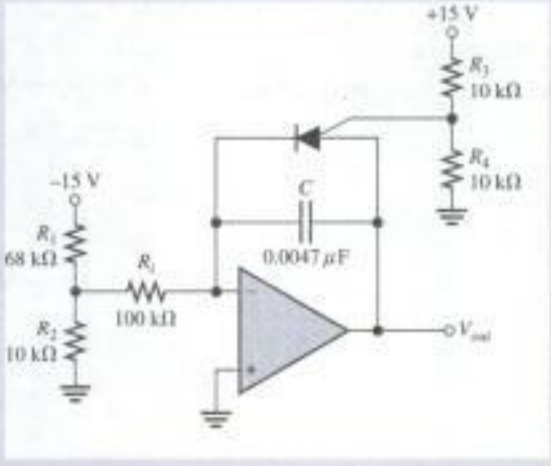
(b) The capacitor rapidly discharges when the PUT momentarily turns on.

EXAMPLE 16–5

(a) Find the amplitude and frequency of the sawtooth output in Figure 16–32. Assume that the forward PUT voltage, V_F, is approximately 1 V.

(b) Sketch the output waveform.

► FIGURE 16–32



Solution **(a)** First, find the gate voltage in order to establish the approximate voltage at which the PUT turns on.

$$V_G = \frac{R_4}{R_3 + R_4}(+V) = \frac{10\text{ k}\Omega}{20\text{ k}\Omega}(15\text{ V}) = 7.5\text{ V}$$

This voltage sets the approximate maximum peak value of the sawtooth output (neglecting the 0.7 V).

$$V_p \cong 7.5\text{ V}$$

The minimum peak value (low point) is

$$V_F \cong 1\text{ V}$$

So the peak-to-peak amplitude is

$$V_{pp} = V_p - V_F = 7.5\text{ V} - 1\text{ V} = \mathbf{6.5\text{ V}}$$

The frequency is determined as follows:

$$V_{BN} = \frac{R_2}{R_1 + R_2}(-V) = \frac{10\text{ k}\Omega}{78\text{ k}\Omega}(-15\text{ V}) = -1.92\text{ V}$$

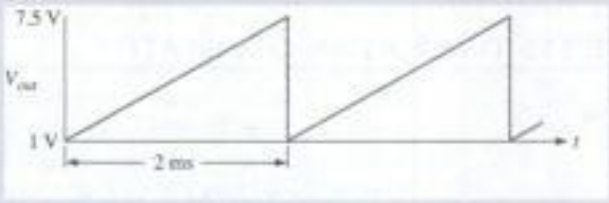
$$f = \frac{|V_{BN}|}{R_5 C}\left(\frac{1}{V_p - V_F}\right) = \left(\frac{1.92\text{ V}}{(100\text{ k}\Omega)(0.0047\ \mu\text{F})}\right)\left(\frac{1}{7.5\text{ V} - 1\text{ V}}\right) = \mathbf{628\text{ Hz}}$$

(b) The output waveform is shown in Figure 16–33, where the period is determined as follows:

$$T = \frac{1}{f} = \frac{1}{628\text{ Hz}} = 2\text{ ms}$$

► FIGURE 16–33

Output of the circuit in Figure 16–32.

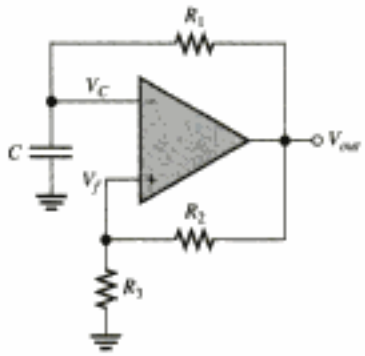


A Square-Wave Oscillator

The basic square-wave oscillator shown in Figure 16–34 is a type of relaxation oscillator because its operation is based on the charging and discharging of a capacitor. Notice that the op-amp's inverting input is the capacitor voltage and the noninverting input is a portion of the output fed back through resistors R_2 and R_3. When the circuit is first turned on, the capacitor is uncharged, and

▶ **FIGURE 16–34**

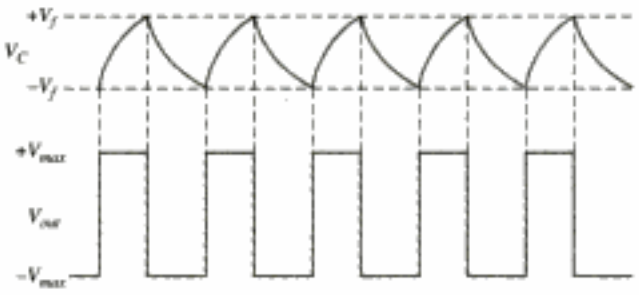
A square-wave relaxation oscillator.



thus the inverting input is at 0 V. This makes the output a positive maximum, and the capacitor begins to charge toward V_{out} through R_1. When the capacitor voltage (V_C) reaches a value equal to the feedback voltage (V_f) on the noninverting input, the op-amp switches to the maximum negative state. At this point, the capacitor begins to discharge from $+V_f$ toward $-V_f$. When the capacitor voltage reaches $-V_f$, the op-amp switches back to the maximum positive state. This action continues to repeat, as shown in Figure 16–35, and a square-wave output voltage is obtained.

▶ **FIGURE 16–35**

Waveforms for the square-wave relaxation oscillator.



SECTION 16–5 REVIEW

1. What is a VCO, and basically, what does it do?
2. Upon what principle does a relaxation oscillator operate?

16–6 THE 555 TIMER AS AN OSCILLATOR

The 555 timer is a versatile integrated circuit with many applications. In this section, you will see how the 555 is configured as an astable or free-running multivibrator, which is essentially a square-wave oscillator. The use of the 555 timer as a voltage-controlled oscillator (VCO) is also discussed.

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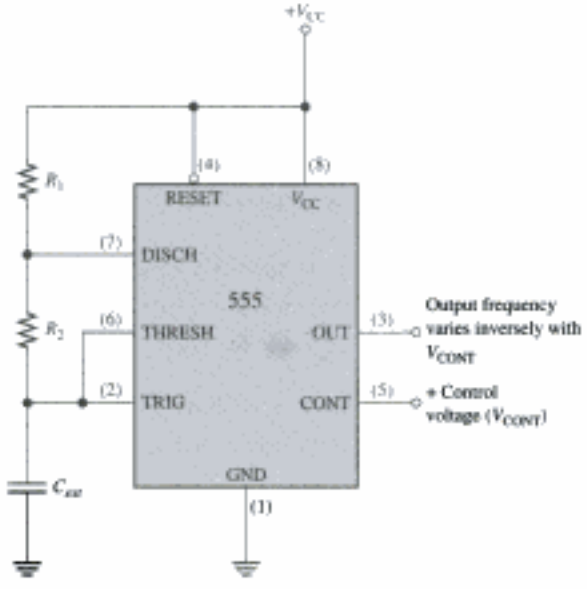
Operation as a Voltage-Controlled Oscillator (VCO)

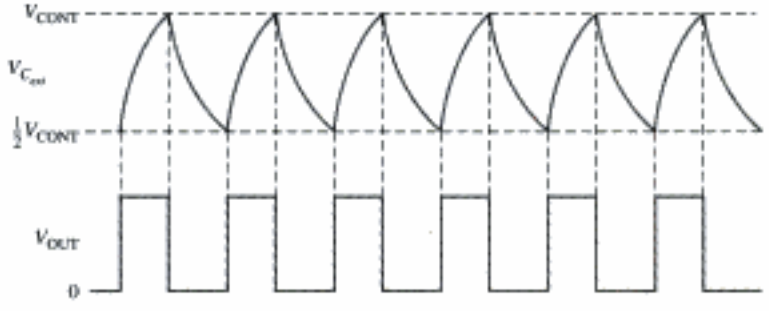
A 555 timer can be set up to operate as a VCO by using the same external connections as for astable operation, with the exception that a variable control voltage is applied to the CONT input (pin 5), as indicated in Figure 16–42.



◀ FIGURE 16–42

The 555 timer connected as a voltage-controlled oscillator (VCO). Note the variable control voltage input on pin 5.

As shown in Figure 16–43, the control voltage (V_{CONT}) changes the threshold values of $\frac{1}{3}V_{CC}$ and $\frac{2}{3}V_{CC}$ for the internal comparators. With the control voltage, the upper value is V_{CONT} and the lower value is $\frac{1}{2}V_{CONT}$, as you can see by examining the internal diagram of the 555 timer. When the control voltage is varied, the output frequency also varies. An increase in V_{CONT} increases the charging and discharging time of the external capacitor and causes the frequency to decrease. A decrease in V_{CONT} decreases the charging and discharging time of the capacitor and causes the frequency to increase.



◀ FIGURE 16–43

The VCO output frequency varies inversely with V_{CONT} because the charging and discharging time of C_{ext} is directly dependent on the control voltage.

An interesting application of the VCO is in phase-locked loops, which are used in various types of communication receivers to track variations in the frequency of incoming signals.

SECTION 16–6 REVIEW

1. Name the five basic elements in a 555 timer IC.
2. When the 555 timer is configured as an astable multivibrator, how is the duty cycle determined?

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(c) a phase shift around the feedback loop of 0°

(d) a gain around the feedback loop of less than 1

12. A second condition for oscillation is
(a) no gain around the feedback loop
(b) a gain of 1 around the feedback loop
(c) the attenuation of the feedback circuit must be one-third
(d) the feedback circuit must be capacitive

13. In a certain oscillator, $A_v = 50$. The attenuation of the feedback circuit must be
(a) 1 (b) 0.01 (c) 10 (d) 0.02

14. For an oscillator to properly start, the gain around the feedback loop must initially be
(a) 1 (b) less than 1 (c) greater than 1 (d) equal to B

15. In a Wien-bridge oscillator, if the resistances in the positive feedback circuit are decreased, the frequency
(a) decreases (b) increases (c) remains the same

16. The Wien-bridge oscillator's positive feedback circuit is
(a) an *RL* circuit (b) an *LC* circuit (c) a voltage divider (d) a lead-lag circuit

17. A phase-shift oscillator has
(a) three *RC* circuits (b) three *LC* circuits (c) a T-type circuit (d) a π-type circuit

18. Colpitts, Clapp, and Hartley are names that refer to
(a) types of *RC* oscillators (b) inventors of the transistor
(c) types of *LC* oscillators (d) types of filters

19. An oscillator whose frequency is changed by a variable dc voltage is known as
(a) a crystal oscillator (b) a VCO
(c) an Armstrong oscillator (d) a piezoelectric device

20. The main feature of a crystal oscillator is
(a) economy (b) reliability (c) stability (d) high frequency

21. The operation of a relaxation oscillator is based on
(a) the charging and discharging of a capacitor
(b) a highly selective resonant circuit
(c) a very stable supply voltage
(d) low power consumption

22. Which one of the following is *not* an input or output of the 555 timer?
(a) Threshold (b) Control voltage (c) Clock
(d) Trigger (e) Discharge (f) Reset

PROBLEMS

Answer to all odd-numbered problems are at the end of the book.

BASIC PROBLEMS

SECTION 16–1 The Oscillator

1. What type of input is required for an oscillator?
2. What are the basic components of an oscillator circuit?

SECTION 16–2 Feedback Oscillator Principles

3. If the voltage gain of the amplifier portion of an oscillator is 75, what must be the attenuation of the feedback circuit to sustain the oscillation?
4. Generally describe the change required in the oscillator of Problem 3 in order for oscillation to begin when the power is initially turned on.

SECTION 16–3 Oscillators with *RC* Feedback Circuits

5. A certain lead-lag circuit has a resonant frequency of 3.5 kHz. What is the rms output voltage if an input signal with a frequency equal to f_r and with an rms value of 2.2 V is applied to the input?


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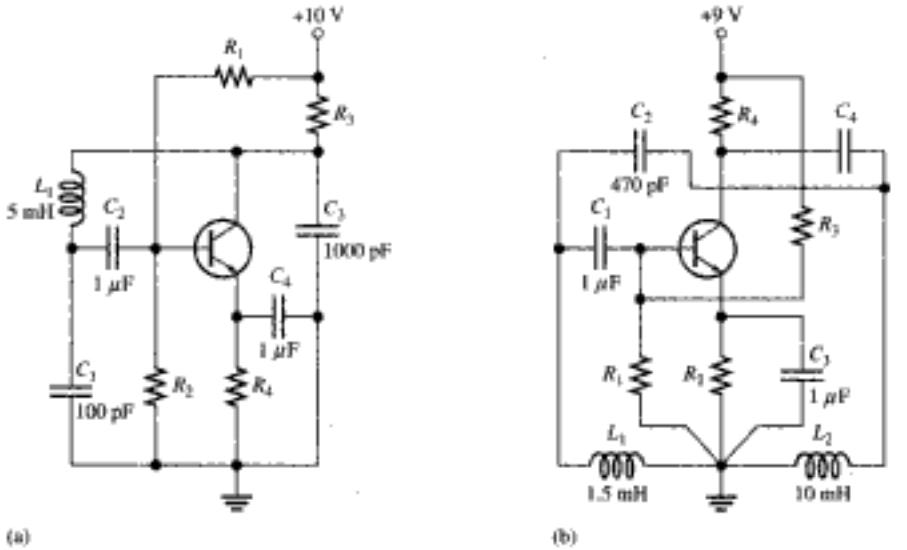
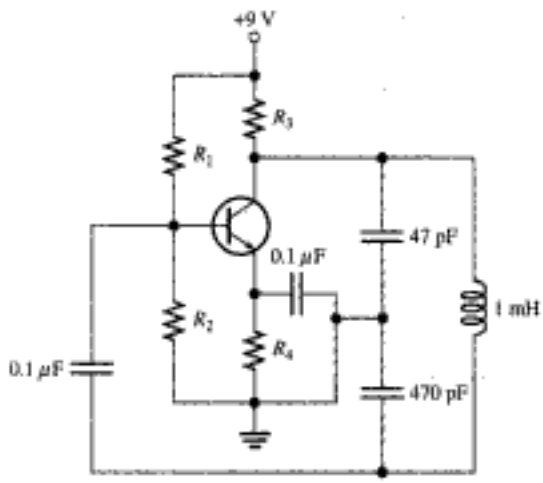
▶ FIGURE 16–47



13. Determine what the gain of the amplifier stage must be in Figure 16–48 in order to have sustained oscillation.

▶ FIGURE 16–48

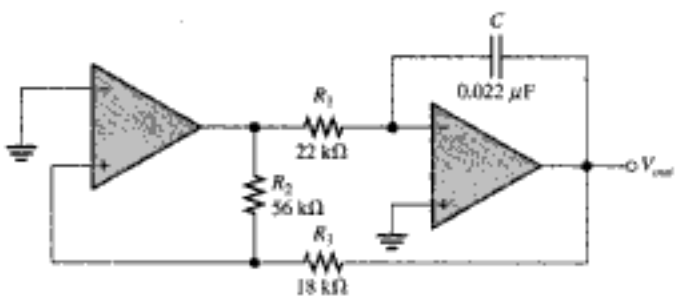


SECTION 16–5 Relaxation Oscillators

14. What type of signal does the circuit in Figure 16–49 produce? Determine the frequency of the output.

15. Show how to change the frequency of oscillation in Figure 16–49 to 10 kHz.

▶ FIGURE 16–49



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17–1 VOLTAGE REGULATION

Two basic categories of voltage regulation are line regulation and load regulation. The purpose of line regulation is to maintain a nearly constant output voltage when the input voltage varies. The purpose of load regulation is to maintain a nearly constant output voltage when the load varies.

Line Regulation

When the dc input (line) voltage changes, an electronic circuit called a **regulator** maintains a nearly constant output voltage, as illustrated in Figure 17–1. **Line regulation** can be defined as the percentage change in the output voltage for a given change in the input (line) voltage. When taken over a range of input voltage values, line regulation is expressed as a percentage by the following formula:

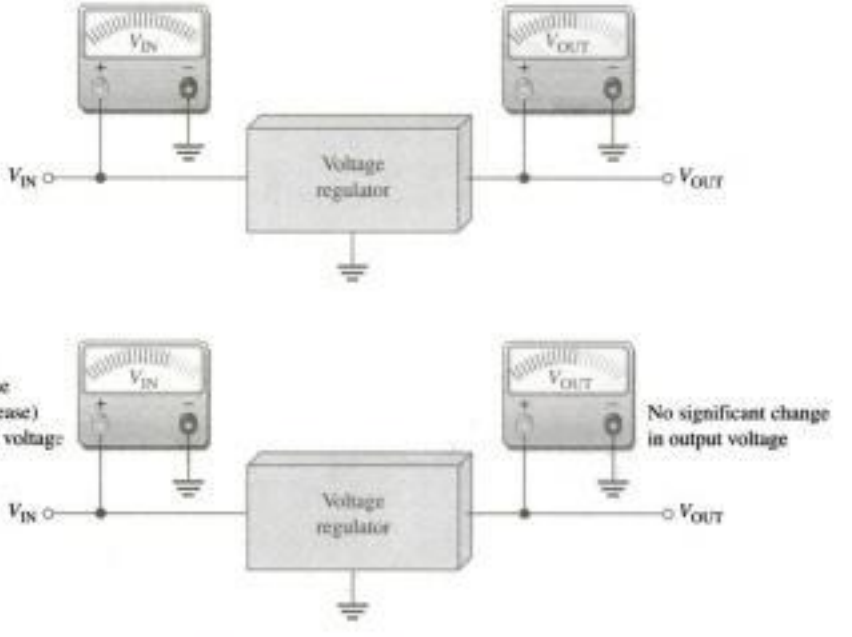
Equation 17–1

$$\text{Line regulation} = \left(\frac{\Delta V_{OUT}}{\Delta V_{IN}}\right)100\%$$

Line regulation can also be expressed in units of %/V. For example, a line regulation of 0.05%/V means that the output voltage changes 0.05 percent when the input voltage increases or decreases by one volt. Line regulation can be calculated using the following formula (Δ means "a change in"):

Equation 17–2

$$\text{Line regulation} = \frac{(\Delta V_{OUT}/V_{OUT})100\%}{\Delta V_{IN}}$$



▶ **FIGURE 17–1**

Line regulation. A change in input (line) voltage does not significantly affect the output voltage of a regulator (within certain limits).

EXAMPLE 17–1

When the input to a particular voltage regulator decreases by 5 V, the output decreases by 0.25 V. The nominal output is 15 V. Determine the line regulation in %/V.

Solution The line regulation as a percentage change per volt is

$$\text{line regulation} = \frac{(\Delta V_{OUT}/V_{OUT})100\%}{\Delta V_{IN}} = \frac{(0.25\text{ V}/15\text{ V})100\%}{5\text{ V}} = \mathbf{0.333\%/V}$$

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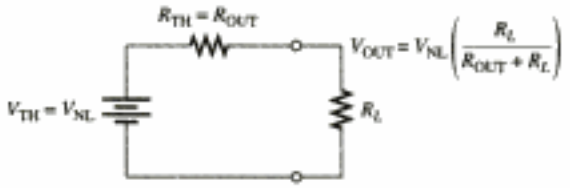
Sometimes power supply manufacturers specify the equivalent output resistance of a power supply (R_{OUT}) instead of its load regulation. Recall that an equivalent Thevenin circuit can be drawn for any two-terminal linear circuit. Figure 17–3 shows the equivalent Thevenin circuit for a power supply with a load resistor. The Thevenin voltage is the voltage from the supply with no load (V_{NL}), and the Thevenin resistance is the specified output resistance, R_{OUT}. Ideally, R_{OUT} is zero, corresponding to 0% load regulation, but in practical power supplies R_{OUT} is a small value. With the load resistor in place, the output voltage is found by applying the voltage-divider rule:

$$V_{OUT} = V_{NL}\left(\frac{R_L}{R_{OUT} + R_L}\right)$$

▶ FIGURE 17–3

Thevenin equivalent circuit for a power supply with a load resitor.



If we let R_{FL} equal the smallest-rated load resistance (largest-rated current), then the full-load output voltage (V_{FL}) is

$$V_{FL} = V_{NL}\left(\frac{R_{FL}}{R_{OUT} + R_{FL}}\right)$$

By rearranging and substituting into Equation 17–3,

$$V_{NL} = V_{FL}\left(\frac{R_{OUT} + R_{FL}}{R_{FL}}\right)$$

$$\text{Load regulation} = \frac{V_{FL}\left(\frac{R_{OUT} + R_{FL}}{R_{FL}}\right) - V_{FL}}{V_{FL}} \times 100\%$$

$$= \left(\frac{R_{OUT} + R_{FL}}{R_{FL}} - 1\right)100\%$$

Equation 17–4

$$\text{Load regulation} = \left(\frac{R_{OUT}}{R_{FL}}\right)100\%$$

Equation 17–4 is a useful way of finding the percent load regulation when the output resistance and minimum load resistance are specified.

SECTION 17–1 REVIEW

Answers are at the end of the chapter.

1. Define *line regulation*.
2. Define *load regulation*.
3. The input of a certain regulator increases by 3.5 V. As a result, the output voltage increases by 0.042 V. The nominal output is 20 V. Determine the line regulation in both % and in %/V.
4. If a 5.0 V power supply has an output resistance of 80 mΩ and a specified maximum output current of 1.0 A, what is the load regulation? Give the result as a % and as a %/mA.

17–2 BASIC SERIES REGULATORS

The fundamental classes of voltage regulators are linear regulators and switching regulators. Both of these are available in integrated circuit form. There are two basic types of linear regulator. One is the series regulator and the other is the shunt regulator. In this section, we will look at the series regulator. The shunt and switching regulators are covered in the next two sections.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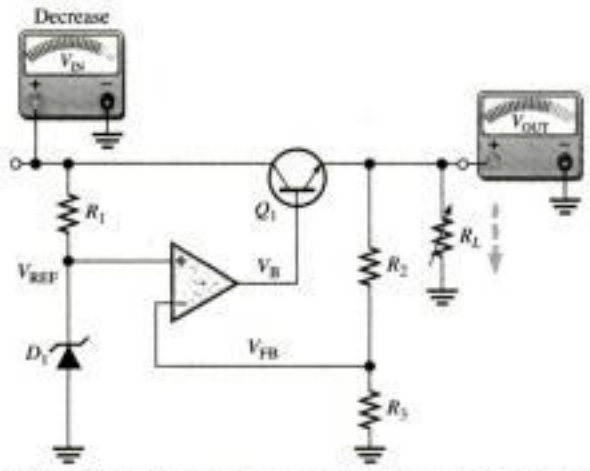
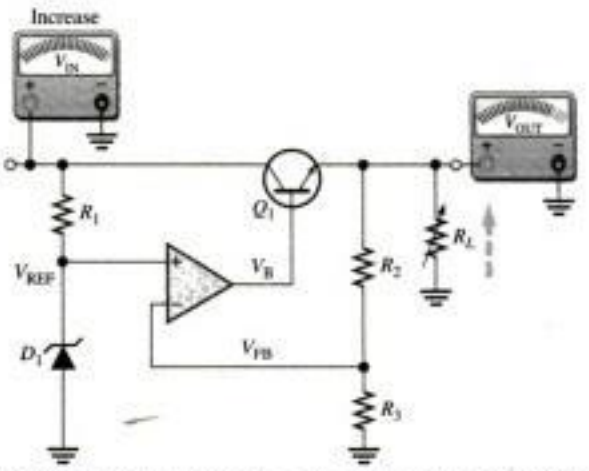


(a) When V_{IN} or R_L decreases, V_{OUT} attempts to decrease. The feedback voltage, V_{FB}, also attempts to decrease, and as a result, the op-amp's output voltage V_B attempts to increase, thus compensating for the attempted decrease in V_{OUT} by increasing the Q_1 emitter voltage. Changes in V_{OUT} are exaggerated for illustration.

When V_{IN} (or R_L) stabilizes at its new lower value, the voltages return to their original values, thus keeping V_{OUT} constant as a result of the negative feedback.



(b) When V_{IN} or R_L increases, V_{OUT} attempts to increase. The feedback voltage, V_{FB}, also attempts to increase, and as a result, V_B, applied to the base of the control transistor, attempts to decrease, thus compensating for the attempted increase in V_{OUT} by decreasing the Q_1 emitter voltage.

When V_{IN} (or R_L) stabilizes at its new higher value, the voltages return to their original values, thus keeping V_{OUT} constant as a result of the negative feedback.

▲ FIGURE 17–6

Illustration of series regulator action that keeps V_{OUT} constant when V_{IN} or R_L changes.

Therefore, the regulated output voltage of the series regulator (neglecting the base-emitter voltage of Q_1) is

Equation 17–5

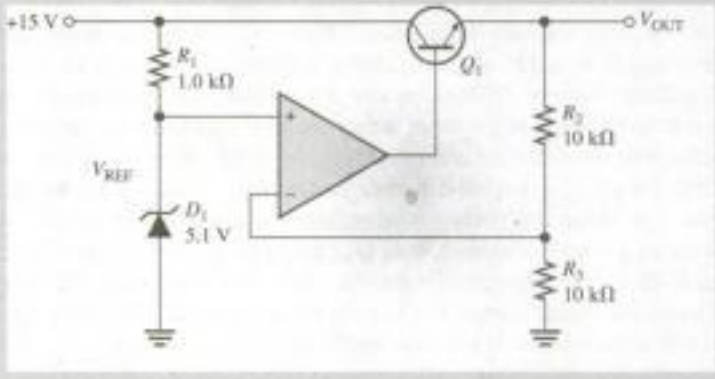
$$V_{OUT} = \left(1 + \frac{R_2}{R_3}\right)V_{REF}$$

From this analysis, you can see that the output voltage is determined by the zener voltage and the resistors R_2 and R_3. It is relatively independent of the input voltage, and therefore, regulation is achieved (as long as the input voltage and load current are within specified limits).

EXAMPLE 17–3

Determine the output voltage for the regulator in Figure 17–7.

► FIGURE 17–7

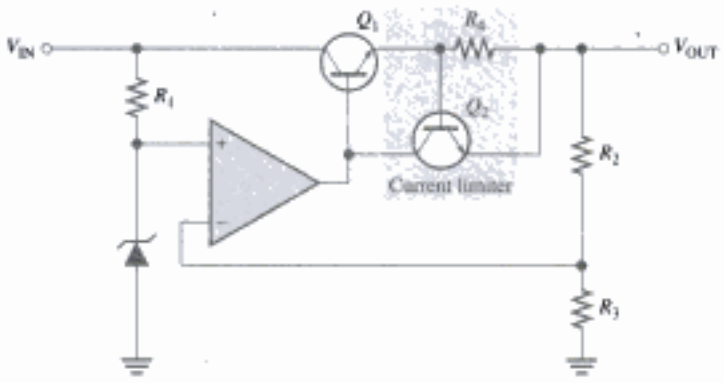


Solution $V_{REF} = 5.1$ V, the zener voltage. The regulated output voltage is therefore

$$V_{OUT} = \left(1 + \frac{R_2}{R_3}\right)V_{REF} = \left(1 + \frac{10\text{ k}\Omega}{10\text{ k}\Omega}\right)5.1\text{ V} = (2)5.1\text{ V} = \mathbf{10.2\text{ V}}$$

Short-Circuit or Overload Protection

If an excessive amount of load current is drawn, the series-pass transistor can be quickly damaged or destroyed. Most regulators use some type of excess current protection in the form of a current-limiting mechanism. Figure 17–8 shows one method of current limiting to prevent overloads called *constant-current limiting*. The current-limiting circuit consists of transistor Q_2 and resistor R_4.



◀ **FIGURE 17–8**
Series regulator with constant-current limiting.

The load current through R_4 produces a voltage from base to emitter of Q_2. When I_L reaches a predetermined maximum value, the voltage drop across R_4 is sufficient to forward-bias the base-emitter junction of Q_2, thus causing it to conduct. Enough op-amp output current is diverted through Q_2 to reduce the Q_1 base current, so that I_L is limited to its maximum value, $I_{L(max)}$. Since the base-to-emitter voltage of Q_2 cannot exceed approximately 0.7 V for a silicon transistor, the voltage across R_4 is held to this value, and the load current is limited to

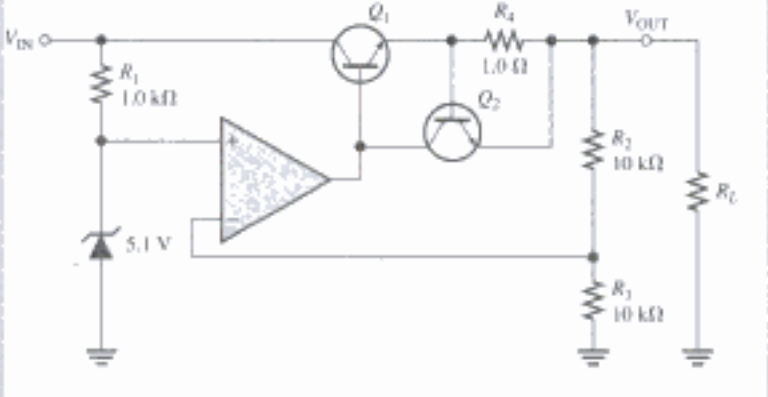
$$I_{L(max)} = \frac{0.7\text{ V}}{R_4}$$

Equation 17–6

EXAMPLE 17–4

Determine the maximum current that the regulator in Figure 17–9 can provide to a load.

▶ **FIGURE 17–9**



Solution

$$I_{L(max)} = \frac{0.7\text{ V}}{R_4} = \frac{0.7\text{ V}}{1.0\,\Omega} = 0.7\text{ A}$$

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The power dissipation in R_1 is

$$P_{R1} = \frac{V_{R1}^2}{R_1} = \frac{(12.5\text{ V})^2}{22\ \Omega} = 7.10\text{ W}$$

Therefore, a resistor with a rating of at least 10 W should be used.

SECTION 17–3 REVIEW

1. How does the control element in a shunt regulator differ from that in a series regulator?
2. What is one advantage of a shunt regulator over a series type? What is a disadvantage?

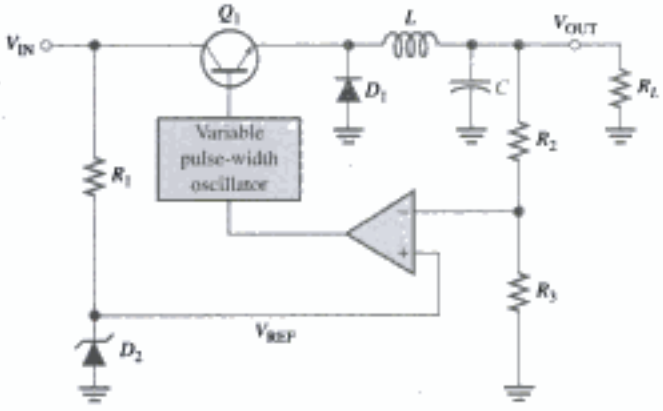
17–4 BASIC SWITCHING REGULATORS

The two types of linear regulators, series and shunt, have control elements (transistors) that are conducting all the time, with the amount of conduction varied as demanded by changes in the output voltage or current. The switching regulator is different because the control element operates as a switch.

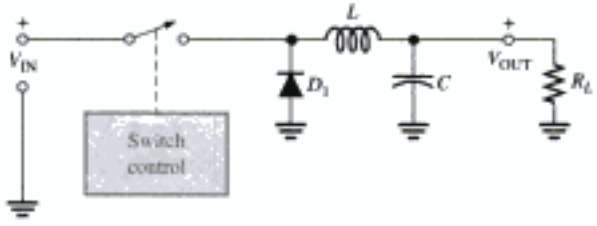
A greater efficiency can be realized with a switching type of voltage regulator than with the linear types because the transistor is not always conducting. Therefore, switching regulators can provide greater load currents at low voltage than linear regulators because the control transistor doesn't dissipate as much power. Three basic configurations of switching regulators are step-down, step-up, and inverting.

Step-Down Configuration

In the step-down configuration, the output voltage is always less than the input voltage. A basic step-down **switching regulator** is shown in Figure 17–16(a), and its simplified equivalent is shown in Figure 17–16(b). Transistor Q_1 is used to switch the input voltage at a duty cycle that is based on the regulator's load requirement. The *LC* filter is then used to average the switched voltage. Since Q_1 is either *on* (saturated) or *off*, the power lost in the control element is relatively small. Therefore, the switching regulator is useful primarily in higher power applications or in applications where efficiency is of utmost concern.



(a) Typical circuit



(b) Simplified equivalent circuit

▲ FIGURE 17–16

Basic step-down switching regulator.

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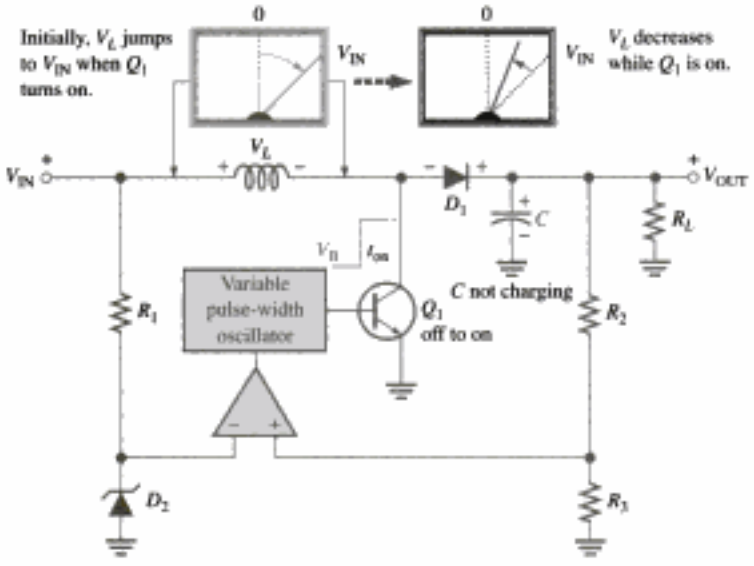
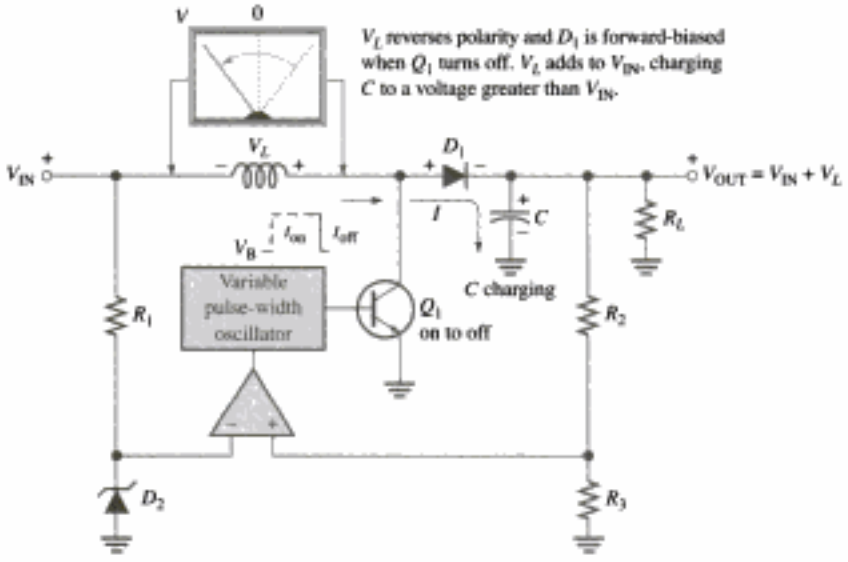
▶ **FIGURE 17–20**

Basic action of a step-up regulator when Q_1 is on.



▶ **FIGURE 17–21**

Basic switching action of a step-up regulator when Q_1 turns off.



in Figure 17–20. During the on-time (t_{on}) of Q_1, the inductor voltage, V_L, decreases from its initial maximum and diode D_1 is reverse-biased. The longer Q_1 is on, the smaller V_L becomes. During the on-time, the capacitor only discharges an extremely small amount through the load.

When Q_1 turns off, as indicated in Figure 17–21, the inductor voltage suddenly reverses polarity and adds to V_{IN}, forward-biasing diode D_1 and allowing the capacitor to charge. The output voltage is equal to the capacitor voltage and can be larger than V_{IN} because the capacitor is charged to V_{IN} plus the voltage induced across the inductor during the off-time of Q_1. The output voltage is dependent on both the inductor's magnetic field action (determined by t_{on}) and the charging of the capacitor (determined by t_{off}).

Voltage regulation is achieved by the variation of the on-time of Q_1 (within certain limits) as related to changes in V_{OUT} due to changing load or input voltage. If V_{OUT} tries to increase, the on-time of Q_1 will decrease, resulting in a decrease in the amount that C will charge. If V_{OUT} tries to decrease, the on-time of Q_1 will increase, resulting in an increase in the amount that C will charge. This regulating action maintains V_{OUT} at an essentially constant level.

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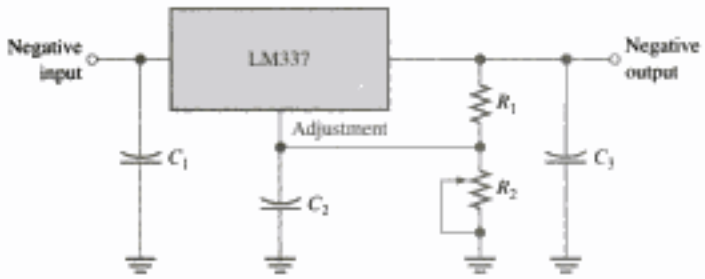
▶ FIGURE 17–30

The LM337 three-terminal adjustable negative voltage regulator.



Switching Voltage Regulators

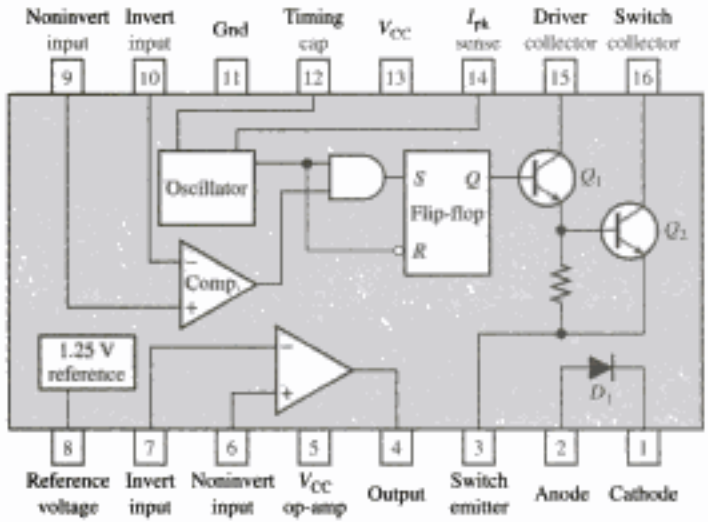
As an example of an IC switching voltage regulator, let's look at the 78S40. This is a universal device that can be used with external components to provide step-up, step-down, and inverting operation.

The internal circuitry of the 78S40 is shown in Figure 17–31. This circuit can be compared to the basic switching regulators that were covered in Section 17–4. For example, look back at Figure 17–16(a). The oscillator and comparator functions are directly comparable. The gate and flip-flop in the 78S40 were not included in the basic circuit of Figure 17–16(a), but they provide additional regulating action. Transistors Q_1 and Q_2 effectively perform the same function as Q_1 in the basic circuit. The 1.25 V reference block in the 78S40 has the same purpose as the zener diode in the basic circuit, and diode D_1 in the 78S40 corresponds to D_1 in the basic circuit.

The 78S40 also has an "uncommited" op-amp thrown in for good measure. It is not used in any of the regulator configurations. External circuitry is required to make this device operate as a regulator, as you will see in Section 17–6.

▶ FIGURE 17–31

The 78S40 switching regulator.



SECTION 17–5 REVIEW

1. What are the three terminals of a fixed-voltage regulator?
2. What is the output voltage of a 7809? Of a 7915?
3. What are the three terminals of an adjustable-voltage regulator?
4. What external components are required for a basic LM317 configuration?

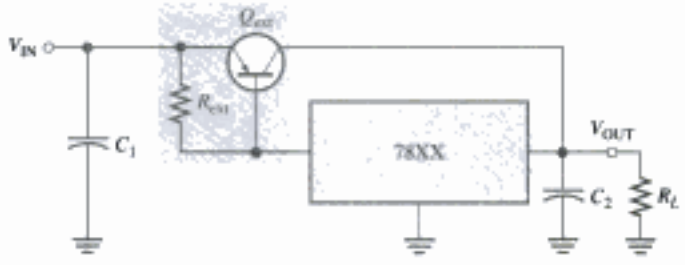
17–6 APPLICATIONS OF IC VOLTAGE REGULATORS

In the last section, you saw several devices that are representative of the general types of IC voltage regulators. Now, several different ways these devices can be modified with external circuitry to improve or alter their performance are examined.

The External Pass Transistor

As you know, an IC voltage regulator is capable of delivering only a certain amount of output current to a load. For example, the 78XX series regulators can handle a peak output current of 1.3 A (more under certain conditions). If the load current exceeds the maximum allowable value, there will be thermal overload and the regulator will shut down. A thermal overload condition means that there is excessive power dissipation inside the device.

If an application requires more than the maximum current that the regulator can deliver, an external pass transistor Q_{ext}, can be used. Figure 17–32 illustrates a three-terminal regulator with an external pass transistor for handling currents in excess of the output current capability of the basic regulator.



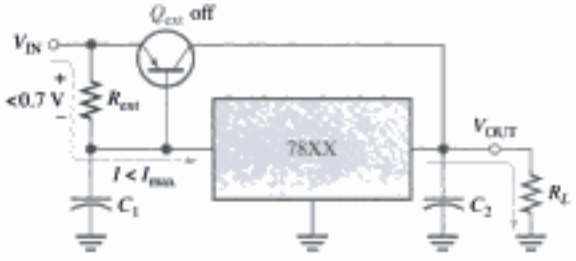
◀ **FIGURE 17–32**
A 78XX-series three-terminal regulator with an external pass transitor to increase power dissipation.

The value of the external current-sensing resistor, R_{ext}, determines the value of current at which Q_{ext} begins to conduct because it sets the base-to-emitter voltage of the transistor. As long as the current is less than the value set by R_{ext}, the transistor Q_{ext} is off, and the regulator operates normally as shown in Figure 17–33(a). This is because the voltage drop across R_{ext} is less than the 0.7 V base-to-emitter voltage required to turn Q_{ext} on. R_{ext} is determined by the following formula, where I_{max} is the highest current that the voltage regulator is to handle internally.

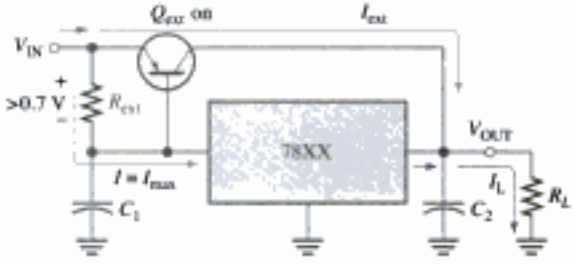
$$R_{ext} = \frac{0.7\text{ V}}{I_{max}}$$

Equation 17–10

When the current is sufficient to produce at least a 0.7 V drop across R_{ext}, the external pass transistor Q_{ext} turns on and conducts any current in excess of I_{max}, as indicated in Figure 17–33(b). Q_{ext} will conduct more or less, depending on the load requirements. For example, if the total load current is 3 A and I_{max} was selected to be 1 A, the external pass transistor will conduct 2 A, which is the excess over the internal voltage regulator current I_{max}.



(a) When the regulator current is less than I_{max}, the external pass transistor is off and the regulator is handling all of the current.



(b) When the load current exceeds I_{max}, the drop across R_{ext} turns Q_{ext} on and it conducts the excess current.

▲ **FIGURE 17–33**
Operation of the regulator with an external pass transitor.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5. If R_2 in Figure 17–15 is increased, the power dissipation in R_1 will
   (a) increase **(b)** decrease **(c)** not change
6. If the duty cycle of the variable pulse-width oscillator in Figure 17–16(a) is increased, the output voltage will
   (a) increase **(b)** decrease **(c)** not change
7. To increase the maximum current that the regulator in Figure 17–26 can supply, the value of R_{sc} must
   (a) increase **(b)** decrease **(c)** not change
8. In the case of line regulation,
   (a) when the temperature varies, the output voltage stays constant
   (b) when the output voltage changes, the load current stays constant
   (c) when the input voltage changes, the output voltage stays constant
   (d) when the load changes, the output voltage stays constant
9. In the case of load regulation,
   (a) when the temperature varies, the output voltage stays constant
   (b) when the input voltage changes, the load current stays constant
   (c) when the load changes, the load current stays constant
   (d) when the load changes, the output voltage stays constant
10. All of the following are parts of a basic voltage regulator *except*
    (a) control element **(b)** sampling circuit
    (c) voltage-follower **(d)** error detector **(e)** reference voltage
11. The basic difference between a series regulator and a shunt regulator is
    (a) the amount of current that can be handled **(b)** the position of the control element
    (c) the type of sample circuit **(d)** the type of error detector
12. In a basic series regulator, V_{OUT} is determined by
    (a) the control element **(b)** the sample circuit
    (c) the reference voltage **(d)** answers (b) and (c)
13. The main purpose of current limiting in a regulator is
    (a) protection of the regulator from excessive current
    (b) protection of the load from excessive current
    (c) to keep the power supply transformer from burning up
    (d) to maintain a constant output voltage
14. In a linear regulator, the control transistor is conducting
    (a) a small part of the time **(b)** half the time
    (c) all of the time **(d)** only when the load current is excessive
15. In a switching regulator, the control transistor is conducting
    (a) part of the time **(b)** all of the time
    (c) only when the input voltage exceeds a set limit **(d)** only when there is an overload
16. The LM317 is an example of an IC
    (a) three-terminal negative voltage regulator **(b)** fixed positive voltage regulator
    (c) switching regulator **(d)** linear regulator
    (e) variable positive voltage regulator **(f)** answers (b) and (d) only
    (g) answers (d) and (e) only
17. An external pass transistor is used for
    (a) increasing the output voltage **(b)** improving the regulation
    (c) increasing the current that the regulator can handle **(d)** short-circuit protection

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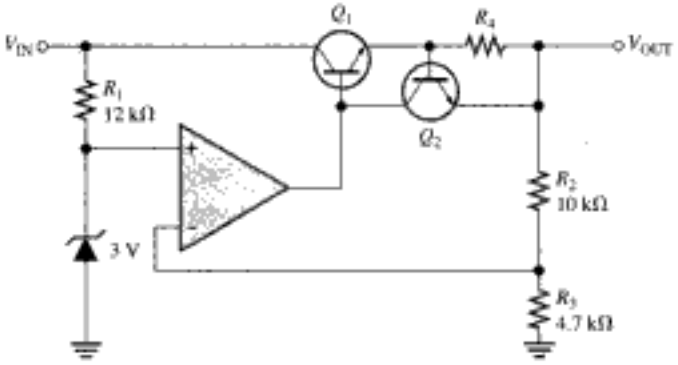
8. If R_3 in Figure 17–35 is increased to 4.7 kΩ, what happens to the output voltage?

9. If the zener voltage is 2.7 V instead of 2.4 V in Figure 17–46, what is the output voltage?

10. A series voltage regulator with constant-current limiting is shown in Figure 17–36. Determine the value of R_4 if the load current is to be limited to a maximum value of 250 mA. What power rating must R_4 have?

► **FIGURE 17–36**

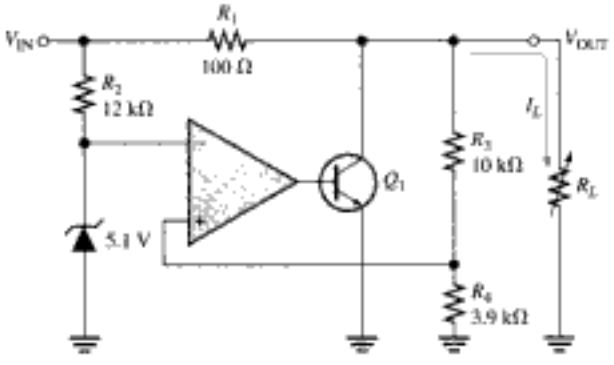


11. If the R_4 determined in Problem 10 is halved, what is the maximum load current?

SECTION 17–3 Basic Shunt Regulators

12. In the shunt regulator of Figure 17–37, when the load current increases, does Q_1 conduct more or less? Why?

► **FIGURE 17–37**



13. Assume I_L remains constant and V_{IN} changes by 1 V in Figure 17–37. What is the change in the collector current of Q_1?

14. With a constant input voltage of 17 V, the load resistance in Figure 17–37 is varied from 1 kΩ to 1.2 kΩ. Neglecting any change in output voltage, how much does the shunt current through Q_1 change?

15. If the maximum allowable input voltage in Figure 17–37 is 25 V, what is the maximum possible output current when the output is short-circuited? What power rating should R_1 have?

SECTION 17–4 Basic Switching Regulators

16. A basic switching regulator is shown in Figure 17–38. If the switching frequency of the transistor is 100 Hz with an off-time of 6 ms, what is the output voltage?

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18

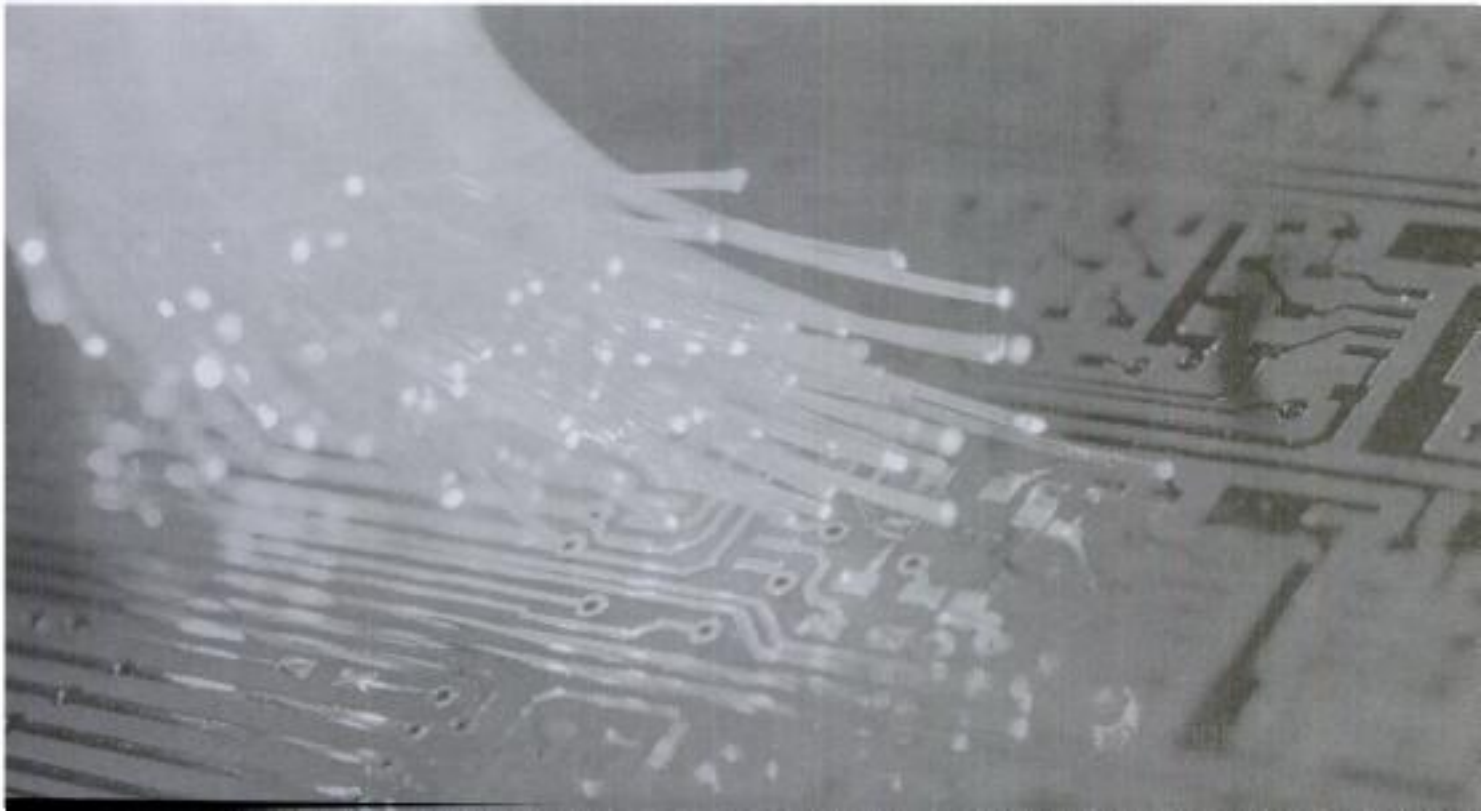
PROGRAMMABLE ANALOG ARRAYS

CHAPTER OUTLINE

INTRODUCTION

Programmable analog devices and programming are introduced in this chapter. Programmable devices have been applied in digital systems for quite some time, and they are now becoming popular for implementing analog designs.

Although programmable analog devices and software are also available from other manufacturers, selected products of Anadigm Corporation are used as examples for the topics of programmable hardware and the accompanying software in this chapter. The AnadigmDesigner2 development software is referenced and is used for illustrations. You can download a 60-day free trial version of this software at www.anadigm.com. Also, you can obtain a development kit that includes a development board with a field-programmable analog array (FPAA) installed, the interface to connect it to your computer, and the development software. Many of the problems at the end of the chapter require the AnadigmDesigner2 software for implementing circuits up to the point of downloading them to a hardware device. If you wish to optionally download the circuits created by the software, you must have the development kit.

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filters) that can be made with individual op-amps and conventional passive components (resistors and capacitors) can be implemented at less cost, in a much smaller size, and with increased reliability and component stability. In addition, the programmability makes it easy to change designs or to modify values in any given circuit or system at any time.

All FPAAs require a software development package that allows you to enter an analog circuit design on your computer, test it by simulation, and download it to the FPAA chip using a standard interface. The programmable CABs and the interconnection network are controlled by on-chip clock sources, a memory, a shift register, and other logic. The software program performs the necessary operations to add the required analog functions, to make appropriate interconnections, and to properly configure the switched-capacitor networks to produce circuit values and parameters for achieving specified performance characteristics in the FPAA device.

SECTION 18–1 REVIEW

Answers are at the end of the chapter.

1. What does the acronym FPAA stand for?
2. What does the acronym CAB stand for?
3. Name the programmable features of a typical FPAA.
4. What is a common technology used to implement analog functions in a CAB?

18–2 SWITCHED-CAPACITOR CIRCUITS

Switched-capacitor circuits are used in field-programmable analog arrays to implement various analog circuits on an IC chip using only capacitors. A capacitor can be implemented on a chip more easily than can a resistor. Capacitors also offer other advantages such as no power dissipation. When a resistance is required in a circuit, a switched capacitor can be made to emulate (to imitate or act the same as) a resistor. Reprogramming switched-capacitors can readily change resistor values, and a more accurate and stable resistance can be achieved. You should have a basic understanding of switched capacitors; however, when you program an FPAA, the software shields you from all of the complex circuit details.

Recall that the definition of current in terms of charge and time is expressed as

$$I = \frac{Q}{t}$$

This formula shows that current is the rate at which charge flows through a circuit. Also, recall that the definition of charge in terms of capacitance and voltage is

$$Q = CV$$

By substituting CV for Q, you can express the current as

$$I = \frac{CV}{t}$$

Basic Operation

A general model of a switched-capacitor circuit, as shown in Figure 18–3(a), consists of a capacitor, two voltage sources, V_1 and V_2, and a two-pole switch. Let's examine this circuit for a specified period of time, T. Assume that V_1 and V_2 are constant during the time period T and $V_1 > V_2$. Of particular interest is the *average* current I_1 produced by the source V_1 during the time period T.

During the first half of the time period T, the switch is in position 1, as indicated in Figure 18–3(b). The capacitor charges very rapidly to the source voltage V_1. Therefore, an average current I_1 due to V_1 is charging the capacitor during the interval from $t = 0$ to $t = T/2$.


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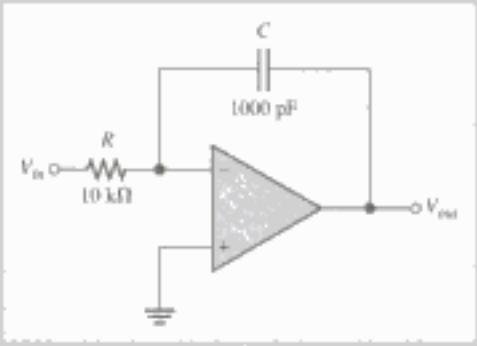
EXAMPLE 18–1

Replace the input resistor in the integrator of Figure 18–8 with a switched-capacitor and show the resulting circuit.

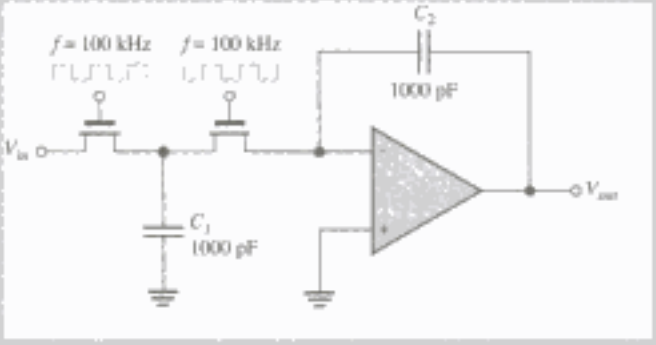
▶ **FIGURE 18–8**



Solution An integrator with a switched-capacitor circuit that emulates the resistor is shown in Figure 18–9.

▶ **FIGURE 18–9**

Switched-capacitor integrator equivalent to the circuit in Figure 18–8.



The values shown in Figure 18–9 are determined as follows. Assume that the switched-capacitor value is 1000 pF. You want the switched capacitor to emulate a 10 kΩ resistor by effectively providing the same average current as the actual resistor would. Using the formula $R = T/C$,

$$T = RC = (10\ \text{k}\Omega)(1000\ \text{pF}) = 10\ \mu\text{s}$$

This means that each switch must be operated at a frequency of

$$f = \frac{1}{T} = \frac{1}{10\ \mu\text{s}} = 100\ \text{kHz}$$

The duty cycle should be 50% so that the switch is in each position half of the period. Two non-overlapping 100 kHz, 50% duty cycle voltages that are 180° out-of-phase with each other are applied to the transistor switches in Figure 18–9.

Emulating Feedback Resistors

You have seen in the preceding discussion and example how the input resistor to an op-amp circuit can be emulated with a switched-capacitor circuit. However, feedback resistors, such as used in differentiators, inverting and noninverting amplifiers, and certain types of filters require a variation in approach.

The switched-capacitor implementation for the input resistor used in the integrator of Figure 18–9 is impractical for emulating a feedback resistor such as shown in the op-amp in Figure 18–10(a). Because the two transistor switches are never on at the same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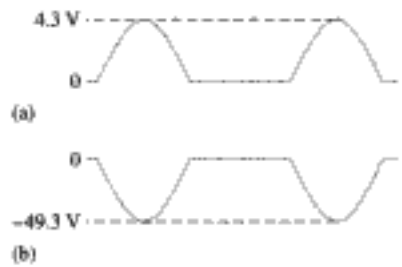
Answers to Selected Problems

Chapter 1

1. 6 electrons; 6 protons
3. **(a)** insulator **(b)** semiconductor **(c)** conductor
5. Four
7. Conduction band and valence band
9. Antimony is a pentavalent material. Boron is a trivalent material. Both are used for doping.
11. No. The barrier potential is a voltage drop.
13. To prevent excessive forward current.
15. A temperature increase.
17. **(a)** −3 V **(b)** 0.7 V **(c)** 0.7 V **(d)** 0.7 V

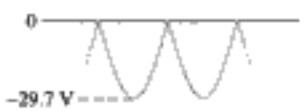
Chapter 2

1. See Figure ANS–1.



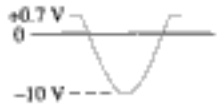
▲ **FIGURE ANS–1**

3. 23 V rms
5. **(a)** 1.59 V **(b)** 63.7 V **(c)** 16.4 V **(d)** 10.5 V
7. 173 V
9. 78.5 V
11. See Figure ANS–2.



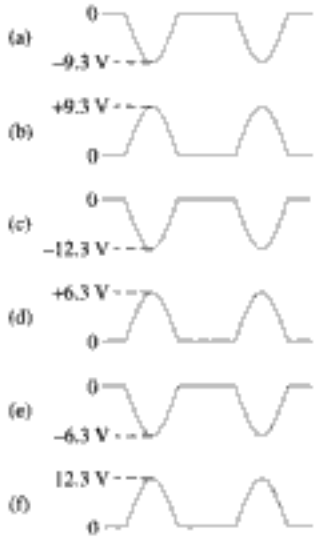
▲ **FIGURE ANS–2**

13. $V_r = 8.33$ V; $V_{DC} = 25.8$ V
15. 556 μF
17. $V_{r(pp)} = 1.25$ V; $V_{DC} = 48.9$ V
19. 4%
21. See Figure ANS–3.



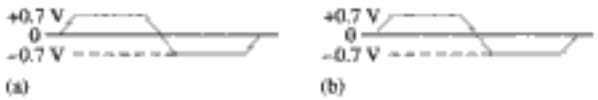
▲ **FIGURE ANS–3**

23. See Figure ANS–4.



▲ **FIGURE ANS–4**

25. See Figure ANS–5.



▲ **FIGURE ANS–5**

27. **(a)** A sine wave with a positive peak at +0.7 V, a negative peak at −7.3 V, and a dc value of −3.3 V.
    (b) A sine wave with a positive peak at +29.3 V, a negative peak at −0.7 V, and a dc value of +14.3 V.
    (c) A square wave varying from +0.7 V down to −15.3 V, with a dc value of −7.3 V.
    (d) A square wave varying from +1.3 V down to −0.7 V, with a dc value of +0.3 V.
29. 56.6 V

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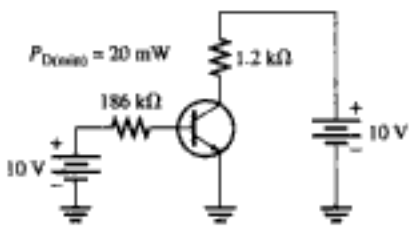
5. Negative, positive
7. 0.947
9. 101.5
11. 8.98 mA
13. 0.99
15. **(a)** $V_{BE} = 0.7$ V, $V_{CE} = 5.10$ V, $V_{CB} = +4.40$ V
    (b) $V_{BE} = -0.7$ V, $V_{CE} = -3.83$ V, $V_{CB} = -3.13$ V
17. $I_B = 30\ \mu$A, $I_E = 1.3$ mA, $I_C = 1.27$ mA
19. 3 μA
21. 425 mW
23. 33.3
25. 500 μA, 3.33 μA, 4.03 V

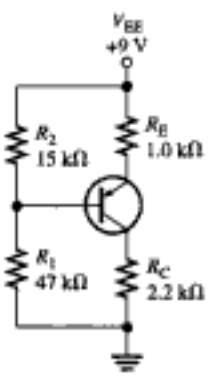
Chapter 5

1. Saturation
3. 18 mA
5. $V_{CE} = 20$ V; $I_{C(sat)} = 2$ mA
7. See Figure ANS–14.



▲ **FIGURE ANS–14**

9. 69.1
11. $I_C \cong 809\ \mu$A; $V_{CE} = 13.2$ V
13. See Figure ANS–15.

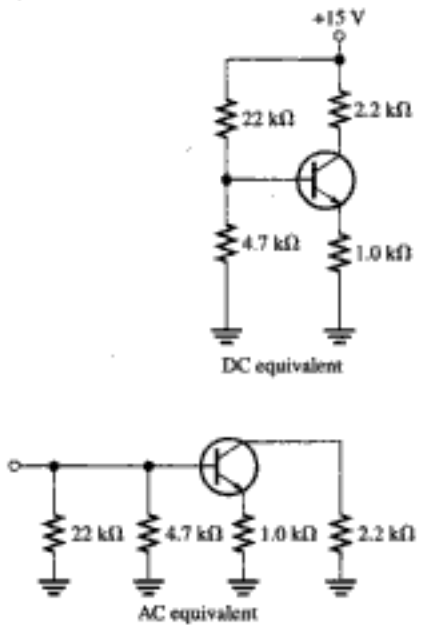


▲ **FIGURE ANS–15**

15. **(a)** −1.41 mA, −8.67 V
    (b) 12.2 mW
17. $I_{CQ} = 92.5$ mA; $V_{CEQ} = 2.75$ V
19. 27.7 mA to 69.2 mA; 6.23 V to 2.08 V; Yes
21. $V_B = -391$ mV; $V_E = -1.10$ V; $V_C = 3.22$ V
23. 0.09 mA
25. $I_C = 16.3$ mA; $V_{CE} = -6.95$ V
27. 2.53 kΩ
29. 7.87 mA; 2.56 V

Chapter 6

1. Slightly greater than 1 mA min.
3. 8.33 Ω
5. $r'_e \cong 19\ \Omega$
7. See Figure ANS–18.



▲ **FIGURE ANS–18**

9. **(a)** 1.29 kΩ **(b)** 968 Ω **(c)** 171
11. **(a)** $V_B = 3.25$ V **(b)** $V_E = 2.55$ V
    (c) $I_E = 2.55$ mA **(d)** $I_C \cong 2.55$ mA
    (e) $V_C = 9.59$ V **(f)** $V_{CE} = 7.04$ V
13. $A'_v = 131$; $\theta = 180°$
15. $A_{v(max)} = 65.5$, $A_{v(min)} = 2.06$
17. A_v is reduced to approximately 30. See Figure ANS–19
19. $R_{in(tot)} = 3.1$ kΩ; $V_{OUT} = 1.06$ V
21. 270 Ω
23. 8.8
25. $R_{in(emitter)} = 2.28\ \Omega$; $A_v = 526$; $A_i \cong 1$; $A_p = 526$
27. 400

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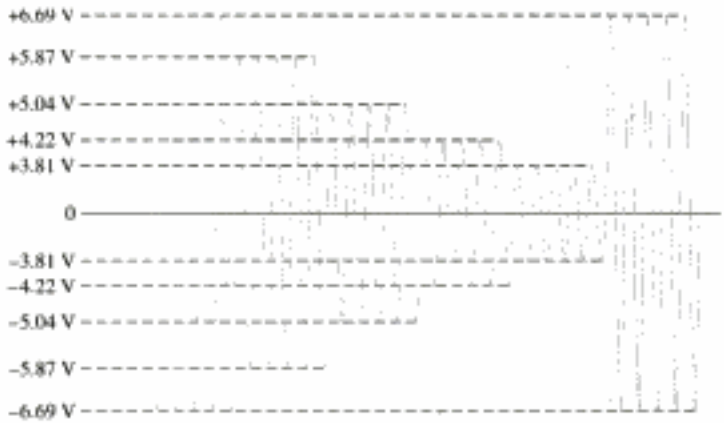
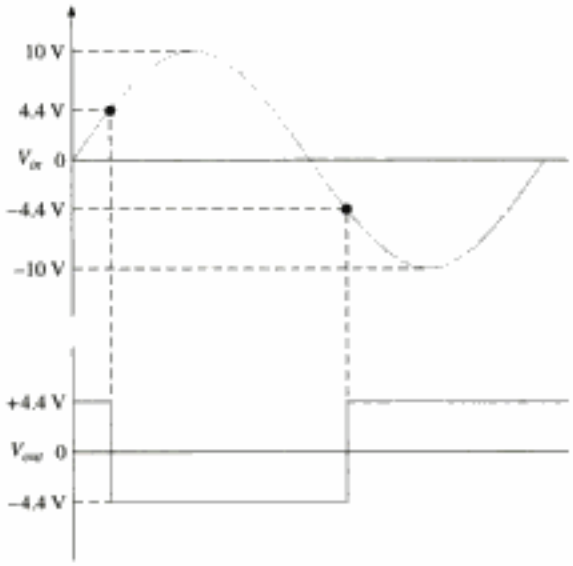


▲ FIGURE ANS–38



▲ FIGURE ANS–39

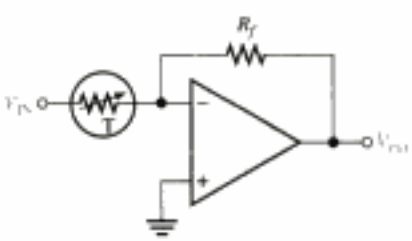
23. **(a)** −0.301 **(b)** **(c)** 1.70 **(d)** 2.11

25. The output of a log amplifier is limited to 0.7 V because of the transistor's *pn* junction.

27. −157 mV

29. $V_{out(max)} = -147$ mV, $V_{out(min)} = -89.2$ mV; the 1 V input peak is reduced 85% whereas the 100 mV input peak is reduced only 10%.

31. See Figure ANS–40.



▲ FIGURE ANS–40

Chapter 15

1. **(a)** Band-pass **(b)** High-pass **(c)** Low-pass **(d)** Band-stop

3. 48.2 kHz, No

5. 700 Hz, 5.04

7. **(a)** 1, not Butterworth
(b) 1.44, approximate Butterworth
(c) 1st stage: 1.67; 2nd stage: 1.67; Not Butterworth

9. **(a)** Chebyshev **(b)** Butterworth **(c)** Bessel **(d)** Butterworth

11. 190 Hz

13. Add another identical stage and change the ratio of the feedback resistors to 0.068 for first stage, 0.586 for second stage, and 1.482 for third stage.

15. Exchange positions of resistors and capacitors.

17. **(a)** Decrease R_1 and R_2 or C_1 and C_2.
(b) Increase R_3 or decrease R_4.

19. **(a)** $f_0 = 4.95$ kHz, $BW = 3.84$ kHz
(b) $f_0 = 449$ Hz, $BW = 96.4$ Hz
(c) $f_0 = 15.9$ kHz, $BW = 838$ Hz

21. Sum the low-pass and high-pass outputs with a two-input adder.

Chapter 16

1. An oscillator requires no input (other than dc power).

3. $\frac{1}{73} = 0.0133$

5. 733 mV

7. 50 kΩ

9. 2.34 kΩ

11. 136 kΩ, 628 Hz

13. 10

15. Change R_1 to 3.54 kΩ

17. $R_4 = 65.8$ kΩ, $R_5 = 47$ kΩ

19. 3.33 V, 6.67 V

21. 0.0076 μF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Glossary

ac ground A point in a circuit that appears as ground to ac signals only.

active filter A frequency-selective circuit consisting of active devices such as transistors or op-amps coupled with reactive components.

A/D conversion A process whereby information in analog form is converted into digital form.

alpha (α) The ratio of dc collector current to dc emitter current in a bipolar junction transistor.

amplification The process of increasing the power, voltage, or current by electronic means.

amplifier An electronic circuit having the capability to amplify power, voltage, or current.

amplitude modulation (AM) A communication method in which a lower-frequency signal modulates (varies) the amplitude of a higher-frequency signal (carrier).

analog Characterized by a linear process in which a variable takes on a continuous set of values.

angle of incidence The angle at which a light ray strikes a surface.

anode The *p* region of a diode.

antilogarithm The result obtained when the base of a number is raised to a power equal to the logarithm of that number.

astable Characterized by having no stable states.

atom The smallest particle of an element that possesses the unique characteristics of that element.

atomic number The number of protons in an atom.

attenuation The reduction in the level of power, current, or voltage.

audio Related to the frequency range of sound waves that can be heard by the human ear and generally considered to be in the 20 Hz to 20 kHz range.

avalanche The rapid buildup of conduction electrons due to excessive reverse-bias voltage.

avalanche breakdown The higher voltage breakdown in a zener diode.

balanced modulation A form of amplitude modulation in which the carrier is suppressed; sometimes known as *suppressed-carrier modulation*.

band-pass filter A type of filter that passes a range of frequencies lying between a certain lower frequency and a certain higher frequency.

band-stop filter A type of filter that blocks or rejects a range of frequencies lying between a certain lower frequency and a certain higher frequency.

bandwidth The characteristic of certain types of electronic circuits that specifies the usable range of frequencies that pass from input to output.

barrier potential The amount of energy required to produce full conduction across the *pn* junction in forward bias.

base One of the semiconductor regions in a BJT. The base is very thin and lightly doped compared to the other regions.

Bessel A type of filter response having a linear phase characteristic and less than −20 dB/decade/pole rolloff.

beta (β) The ratio of dc collector current to dc base current in a BJT; current gain from base to collector.

bias The application of a dc voltage to a diode, transistor, or other device to produce a desired mode of operation.

bipolar Characterized by both free electrons and holes as current carriers.

BJT Bipolar junction transistor; a transistor constructed with three doped semiconductor regions separated by two *pn* junctions.

Bode plot An idealized graph of the gain in dB versus frequency used to graphically illustrate the response of an amplifier or filter.

bounding The process of limiting the output range of an amplifier or other circuit.

breakdown The phenomenon of a sudden and drastic increase when a certain voltage is reached across a device.

bridge rectifier A type of full-wave rectifier consisting of diodes arranged in a four-cornered configuration.

Butterworth A type of filter response characterized by flatness in the passband and a −20 dB/decade/pole roll-off.

bypass capacitor A capacitor placed across the emitter resistor of an amplifier.

byte A group of eight bits in binary data.

CAB Configurable analog block; one of the programmable resources in an FPAA generally consisting of one or more op-amps, a switch matrix, and a capacitor bank.

CAM Configurable analog module; a predesigned analog circuit for which some of its parameters can be selectively programmed.

capture range The range of frequencies over which a PLL can acquire lock.

carbon A semiconductive material.

carrier The high radio frequency (RF) signal that carries modulated information in AM, FM, or other systems.

cascade An arrangement of circuits in which the output of one circuit becomes the input to the next.

cathode The *n* region of a diode.

C code A code used for dynamically configuring an FPAA.

center-tapped rectifier A type of full-wave rectifier consisting of a center-tapped transformer and two diodes.

channel The conductive path between the drain and source in a FET.

Chebyshev A type of filter response characterized by ripples in the passband and a greater than −20 dB/decade/pole roll-off.

clamper A circuit that adds a dc level to an ac voltage using a diode and a capacitor.

class A A type of amplifier that operates entirely in its linear (active) region.

class AB A type of amplifier that is biased into slight conduction.

class B A type of amplifier that operates in the linear region for 180° of the input cycle because it is biased at cutoff.

class C A type of amplifier that operates only for a small portion of the input cycle.

clipper See Limiter.

closed-loop An op-amp configuration in which the output is connected back to the input through a feedback circuit.

closed-loop voltage gain (A_{cl}) The voltage gain of an op-amp with external feedback.

CMRR Common-mode rejection ratio; the ratio of open-loop gain to common-mode gain; a measure of an op-amp's ability to reject common-mode signals.

coherent light Light having only one wavelength.

collector The largest of the three semiconductor regions of a BJT.

common-base (CB) A BJT amplifier configuration in which the base is the common terminal to an ac signal or ground.

common-collector (CC) A BJT amplifier configuration in which the collector is the common terminal to an ac signal or ground.

common-drain (CD) A FET amplifier configuration in which the drain is the grounded terminal.

common-emitter (CE) A BJT amplifier configuration in which the emitter is the common terminal to an ac signal or ground.

common-gate (CG) A FET amplifier configuration in which the gate is the grounded terminal.

common mode A condition where two signals applied to differential inputs are of the same phase, frequency, and amplitude.

common-source (CS) A FET amplifier configuration in which the source is the grounded terminal.

comparator A circuit which compares two input voltages and produces an output in either of two states indicating the greater or less than relationship of the inputs.

complementary symmetry transistors Two transistors, one *npn*, and one *pnp*, having matched characteristics.

conduction electron A free electron.

conductor A material that conducts electrical current very well.

configuration RAM A random-access memory used in FPAAs for storing configuration data from the shadow RAM immediately prior to reconfiguring the FPAA.

core The central part of an atom, includes the nucleus and all but the valence electrons.

covalent Related to the bonding of two or more atoms by the interaction of their valence electrons.

critical angle The angle that defines whether a light ray will be reflected or refracted when it strikes a surface.

critical frequency The frequency at which the response of an amplifier or filter is 3 dB less than at midrange.

crossover distortion Distortion in the output of a class B push-pull amplifier at the point where each transistor changes from the cutoff state to the *on* state.

crystal A solid material in which the atoms are arranged in a symmetrical pattern.

current The rate of flow of electrical charge.

current mirror A circuit that uses matching diode junctions to form a current source. The current in a diode junction is reflected as a matching current in the other junction (which is typically the base-emitter junction of a transistor). Current mirrors are commonly used to bias a push-pull amplifier.

cutoff The nonconducting state of a transistor.

cutoff frequency Another term for critical frequency.

cutoff voltage The value of the gate-to-source voltage that makes the drain current approximately zero.

D/A conversion The process of converting a sequence of digital codes to an analog form.

damping factor A filter characteristic that determines the type of response.

dark current The amount of thermally generated reverse current in a photodiode in the absence of light.

darlington pair A configuration of two transistors in which the collectors are connected and the emitter of the first drives the base of the second to achieve beta multiplication.

dBm A unit for measuring power levels referenced to 1 mW.

dc load line A straight line plot of I_C and V_{CE} for a transistor circuit.

decade A ten-times increase or decrease in the value of a quantity such as frequency.

decibel (dB) A logarithmic measure of the ratio of one power to another or one voltage to another.

demodulation The process in which the information signal is recovered from the IF carrier signal; the reverse of modulation.

depletion In a MOSFET, the process of removing or depleting the channel of charge carriers and thus decreasing the channel conductivity.

depletion region The area near a *pn* junction on both sides that has no majority carriers.

derivative The instantaneous rate of change of a function, determined mathematically.

development software A software that is used for entering a circuit design on the computer, simulating the design, and downloading the design to the FPAA device.

diac A two-terminal four-layer semiconductor device (thyristor) that can conduct current in either direction when properly activated.

differential mode A mode of op-amp operation in which two opposite polarity signal voltages are applied to two inputs.

differential amplifier (diff-amp) An amplifier in which the output is a function of the difference between two input voltages, used as the input stage of an op-amp.

differentiator A circuit that produces an output which approximates the instantaneous rate of change of the input function.

digital Characterized by a process in which a variable takes on either of two values.

diode A semiconductor device with a single *pn* junction that conducts current in only one direction.

diode drop The voltage across the diode when it is forward-biased; approximately the same as the barrier potential and typically 0.7 V for silicon.

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