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DIYALA UNIVERSITY
COLLEGE OF ENGINEERING
ELECTRICAL POWER & MACHINE DEPARTMENT

INDUSTRIAL POWER ELECTRONIC LABROTORY

PRACTICAL EXPERIMENTS IN POWER ELECTRONIC

FOR STUDENTS OF THIRD STAGE

EXPERIMENT NO.5

EXPERIMENT NA.PUT OSCILLATOR & TIMER CIRCUITS

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EXPERIMENT 5

PUT OSCILLATOR & TIMER CIRCUITS

A WORD OF THE CHIEF OF ELECTRICAL POWER & MACHINE DEPARTMENT

Dear students

I'm hoping you will be benefit from studying this experiment. ask your teacher about all problems that will accrued in connection of the experiment circuit &

look please ...

You must success in all measurements you followed according to the experiment procedure & You must getting about the products to be enabled in PUT oscillator& timer circuits. the discussion will help you in understanding & conclusion ,be remembered your answers must be right & limited.

Good luck

the Chief of electrical power & machine department

PH.D

NISREAN KHAMMASS SABAE

OBJECTIVE

1. Understanding the operation and design of PUT relaxation oscillator.
2. Understanding the operation of PUT timer circuit.

DISCUSSION

The characteristic of the PUT was discussed in preceding discussion. We focus on the design and application of the basic PUT relaxation oscillator. The characteristics of the PUT and UJT are similar. Since the PUT is a semiconductor device with the negative resistance characteristic, it is suitable for the use of relaxation oscillators.

At present only a few types of PUT are available in the market. These are 2N6027 and 2N6028, and equivalent types MEU21 and MEU22, and GE types DBT1 and DBT2. We introduce the design procedure for PUT relaxation oscillator by using the specifications of 2N6027 and 2N6028.

Choice of the PUT type

The first step in design procedure is to determine the desired frequency of oscillation. The next is to select the PUT type whose frequency range covers the desired frequencies in your design. From data sheets, the frequency range of 2N6027 is from 0.1Hz to 80KHz, whereas 2N6028 type operates in the frequency below 10KHz.

Basic PUT Oscillator Circuit

Fig. 5-1 shows the circuit of basic PUT relaxation oscillator. The following design notes are based on this circuit.

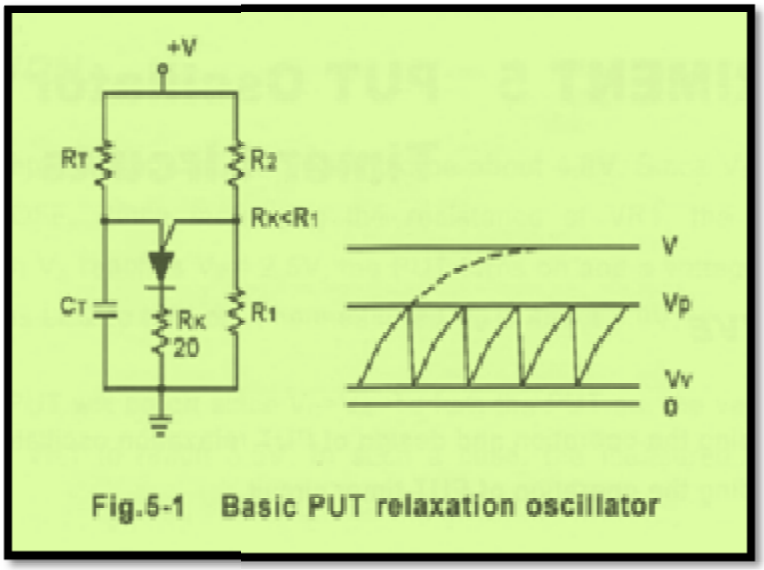


Fig.5-1 Basic PUT relaxation oscillator

Design Notes

1. Considering the frequency stability

The period of oscillation in Fig. 5-1 can be expressed by

$$t = R_T C_T \ln\left(\frac{V - V_P}{V + V_P}\right) = R_T C_T \ln\left(\frac{V - V_V}{V - \eta V - V_T}\right) \quad \text{.....(5-1)}$$

where V_V = valley voltage

V_P = peak voltage

η = intrinsic stand-off ratio

V_T = offset voltage

If $V \gg V_V$ and $(V - \eta V) \gg V_T$, Eq. (5-1) can be rewritten in

$$t \approx R_T C_T \ln(1/(1 - \eta)) \quad \text{.....(5-2)}$$

Therefore the greater the supply voltage, the more stable the frequency becomes.

A silicon diode added to the gate, as shown in Fig. 5-2, improves the frequency stability of the PUT oscillator. At the peak point on the characteristic curve of the PUT, the forward voltage between the anode and gate (V_{AG}) drifts with the temperature coefficient of -2.5mV/°C. The voltage variation of V_{AG} will affect the offset voltage V_T so that the frequency of oscillation is changed. The silicon diode with the same coefficient of temperature is used for improving the thermal stability.

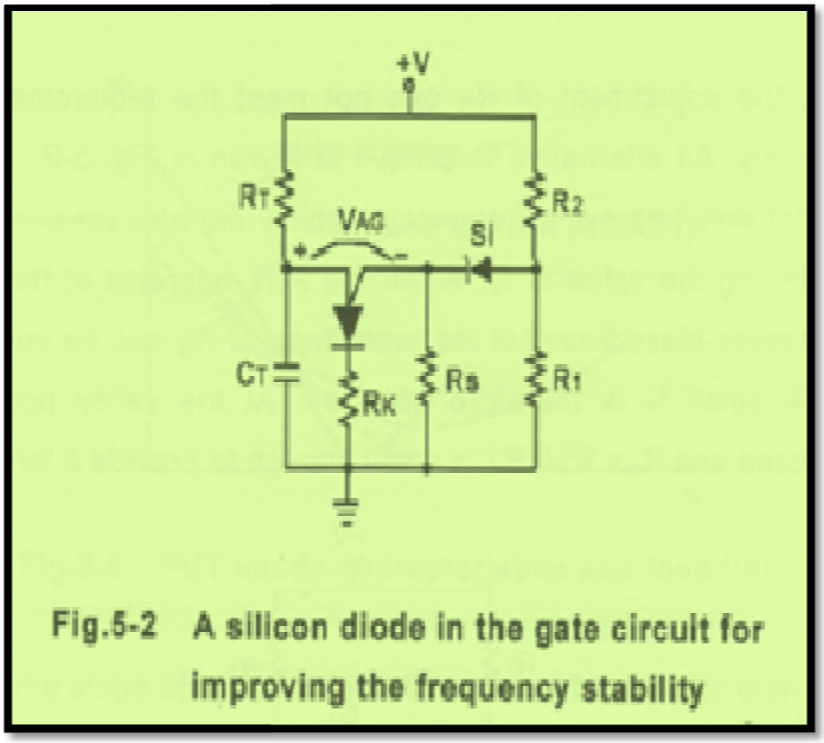


Fig.5-2 A silicon diode in the gate circuit for improving the frequency stability

2. Determining I_P and I_V

A PUT relaxation oscillator needs a wide range of the negative resistance region for a wide range of frequencies. In other words, the smaller I_P and larger I_V as possible are required. But from Fig. 5-3, we can see that the value of R_G must be large for a small I_P and R_G must be small for a large I_V.

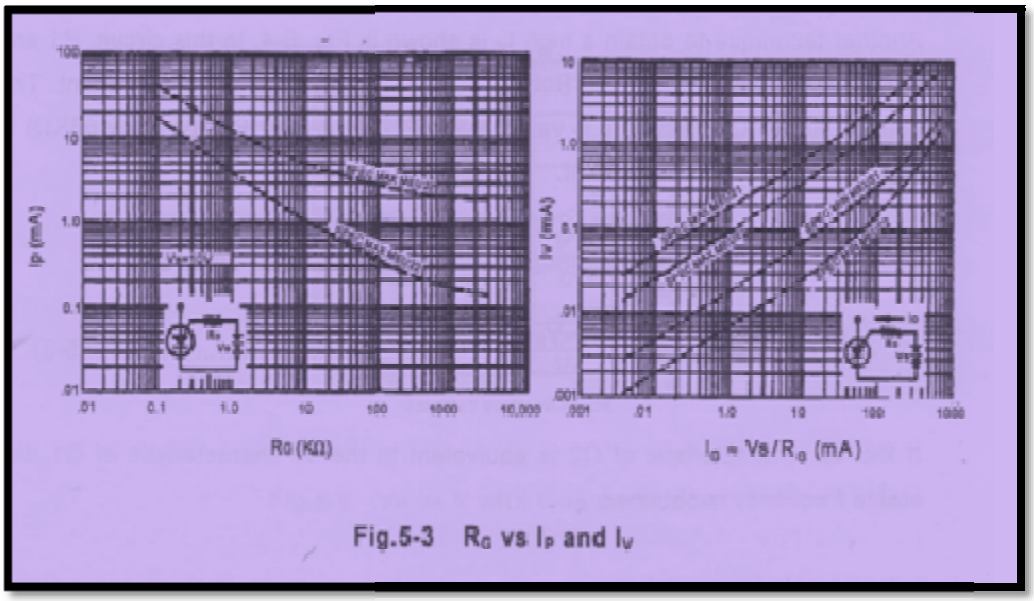


Fig.5-3 R_G vs I_P and I_V

Obviously, the adjustment of R_G can not meet the requirements of I_P and I_V simultaneously. An alternative technique is shown in Fig. 5-2. The silicon diode performs not only improving frequency stability but also lowering the value of I_P and heightening the value of I_V. When the PUT operates at the peak point, the diode is reverse-biased so that the resistance of R_G can be considered as high as 1MΩ. A small I_P is therefore obtained. At the valley point, the diode is forward-biased and R_G= R1// R2 is small enough to provide a large I_V.

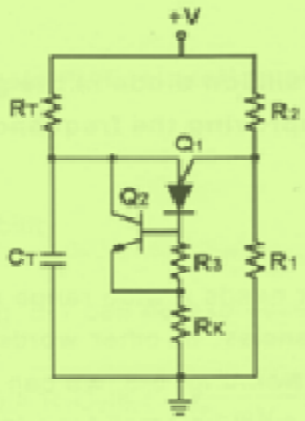


Fig.5-4 Circuit for low I_P and high I_V

Another technique to obtain a high I_V is shown in Fig. 5-4. In this circuit, R1 and R2 are enlarged for a low I_P. Both Q1 and Q2 conduct at the valley point. The current flow in Q2 gains the I_V value of the PUT. Resistor R3 (typically 68KΩ) is used to cut Q2 off at peak point.

In the circuit of Fig. 5-4, the period of oscillation can be expressed as

$$t = R_T C_T \ln \left(\frac{V - Vv - V_{BE(Q2)}}{V - \eta V - V_T} \right) \quad \text{.....(5-3)}$$

If the V_{BE} characteristic of Q2 is equivalent to the V_T characteristic of Q1, the stable frequency is obtained.

Requirements for oscillation

Refer to Fig. 5-5. The R_T load line should lie in the negative resistance portion on the characteristic curve to ensure oscillation.

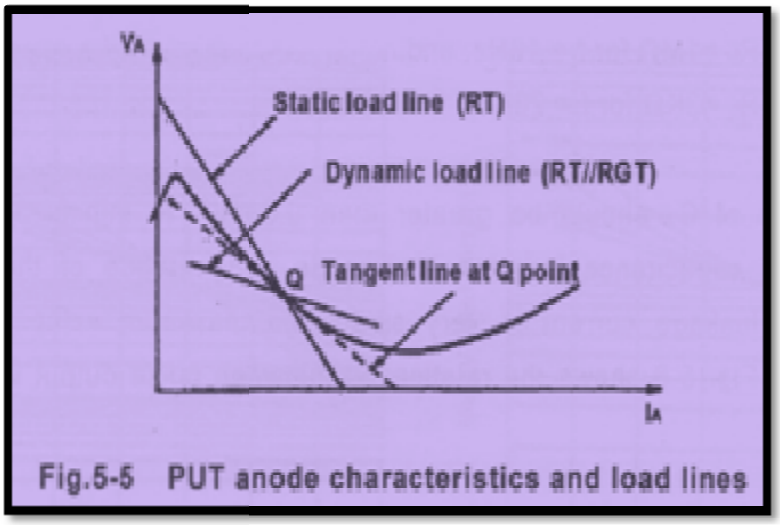


Fig.5-5 PUT anode characteristics and load lines

In addition, the slope of dynamic load line should be smaller than that of tangent at Q point. To achieve this goal, the following equation should be followed:

$$\frac{V - V_P}{I_P} > R_T > \left(\frac{V - V_V}{I_V}\right)\left(\frac{10 + C_T}{5 + C_T}\right) \quad \text{.....(5-4)}$$

where C_T is measured in nF (10^{-9} F). The term of $(10+C_T)/(5+C_T)$ is an empirically derived equation for 2N6027 and 2N6028. If C_T is very high, this term can be considered as 1.

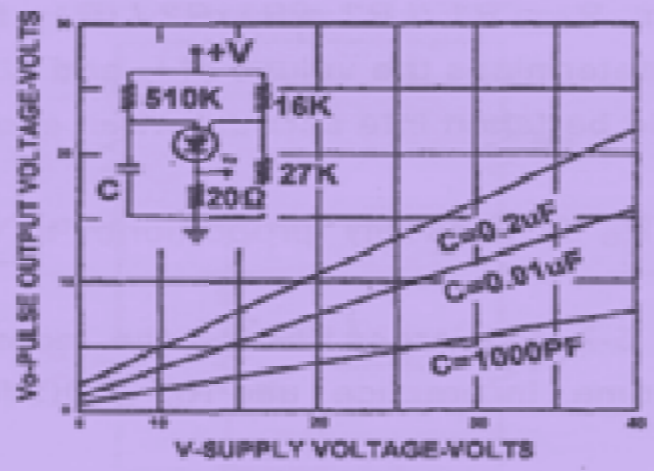


Fig.5-6 Vo vs V with C as parameter

4. Determining R_TC_T time constant

The maximum and minimum values of R_T are expressed in Eq. (5-4). In normal operation, R_T value can be chosen by

R_T =1MΩ for f = 10Hz, and
R_T =3KΩ for f = 20KHz

The value of C_T should be greater than 0.001μF to minimize the effect of distributed capacitance between the anode and cathode of the PUT. If the capacitor leakage current is very small, the maximum value of C_T will be unlimited. Fig. 5-6 shows the relationship between pulse output voltage and C_T value.

5. Determining R_K

The cathode resistor R_K is used to limit the capacitor discharging current and provides the pulse output. The typical value of R_K is calculated by the equation:

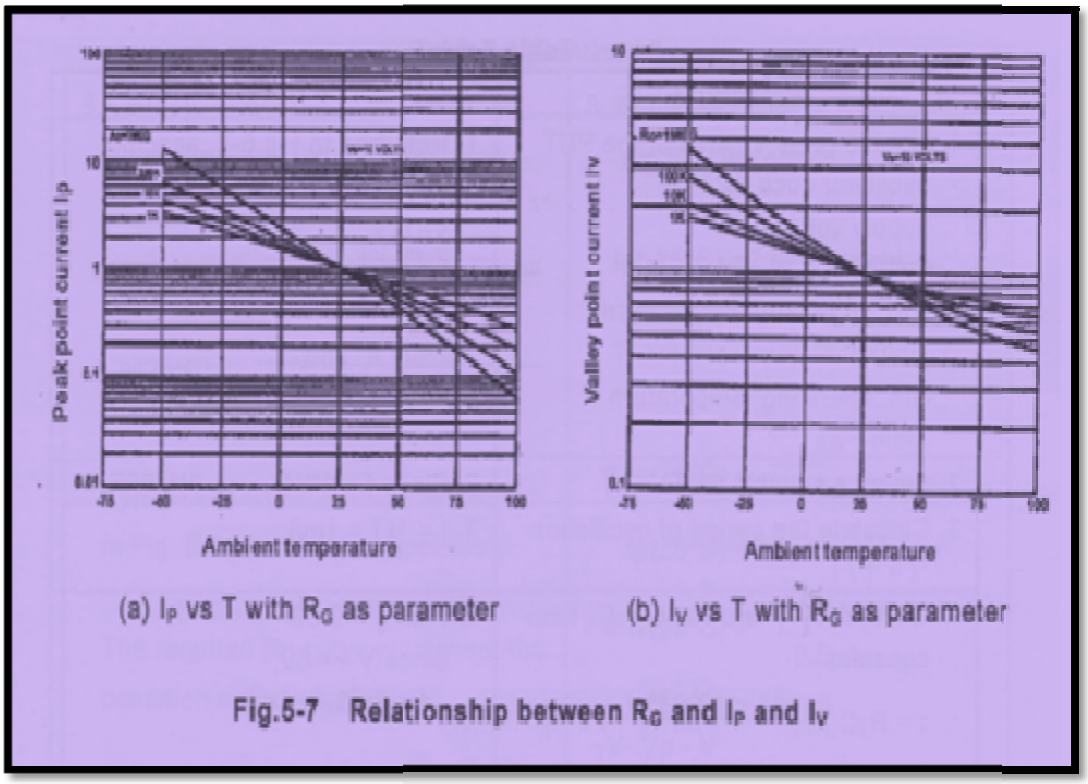
$$R_K = 20\Omega + 1\Omega \times C_T$$

where C_T is measured in μF.

6. Determining R_G

By Thevenin's theorem, $R_G = R1 // R2 = R1xR2 / (R1+ R2)$. As mentioned above, the magnitude of R_G determines the values of I_P and I_V. In addition, there are two factors that should be taken into account when choosing a R_G.

(1) The amount of R_G is inversely proportional to the power dissipation in oscillator circuit.
(2) As shown in Fig. 5-7, the larger the R_G, the more sensitive to temperature the I_P and I_V become. In practice, use R_G=200Ω for f=20KHz and 10KΩ for 10Hz.



(a) I_P vs T with R_G as parameter (b) I_V vs T with R_G as parameter

Fig.5-7 Relationship between R_G and I_P and I_V

Design Example for PUT Relaxation Oscillator

We now summarize the design procedure of PUT relaxation oscillator in Table 5-1 using the circuit of Fig. 6-8 as an example.

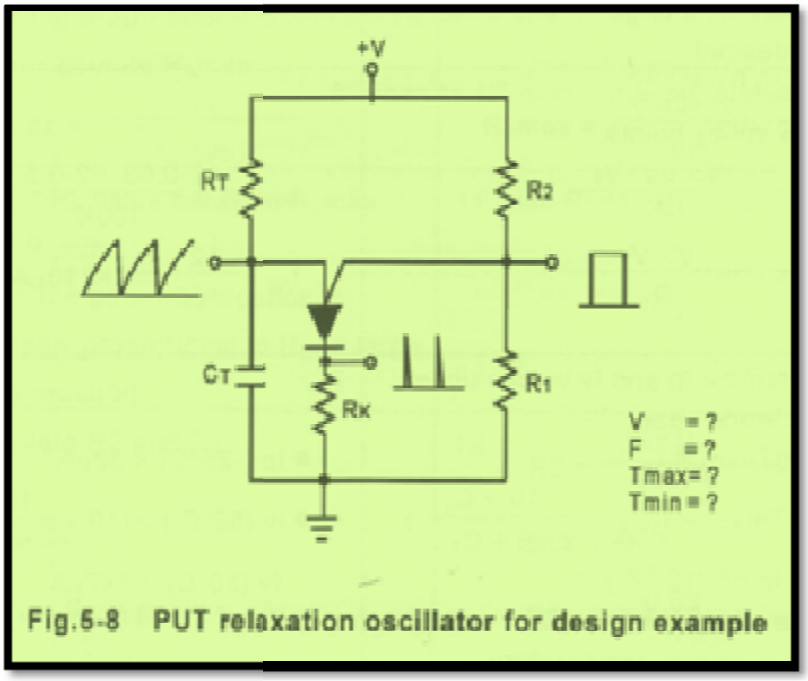


Fig.5-8 PUT relaxation oscillator for design example

Table 5-1

Procedure	Example
1. List the requirements of the PUT oscillator such as: Supply voltage V = ? Frequency f = ? Max. operating temperature Tmax = ? Min. operating temperature Tmin = ?	1. Referring to Fig.6-8, assume that V=12V f = 1KHz Tmax = 50°C Tmin = -25°C
2. Select a suitable PUT	2. Since f = 1KHz, use 2N6027
3. Calculate the period of oscillation $t = 1 / f$	3. $t = 1/f = 1mS$
4. Determine η value and R_TC_T time constant $t = R_TC_T \ln\left(\frac{V - Vv}{V - \eta V - V_T}\right)$ In general, Vv = 1.0 V and V_T = 0.5 V If η=0.63 and V >> 6V, then $t \approx R_T C_T$	4. Pick η = 0.63 Since V >> 6V, $\therefore t \approx R_T C_T \approx 1mS$
5. Determine R_T and C_T. Generally, a large R_T and small C_T are desired.	5. Let R_T = 100KΩ and C_T = 0.01μF
6. Calculate the currents in R1 at peak and valley points. $I_{AP} = \frac{V - \eta V - V_T}{R_T}$ $I_{AV} = \frac{V - Vv}{R_T}$	6. $I_{AP} = \frac{12-0.63\times12-0.5}{100K} = 39\mu A$ $I_{AV} = \frac{12 - 1}{100K} = 110\mu A$
7. Determine Ip and Iv values under the worst case. ● $Ip(Tmin) < I_{AP}$ ● $Iv(Tmax) > I_{AV}\left(\frac{10 + C_T}{5 + C_T}\right)$ C_T in nF (10^{-9} F) The worst case : (1) Ip at min. temperature (2) Iv at max. temperature	7. ● Ip (-25°C) < 39μA ● $Iv\ (50°C) > 110 \times \frac{10+10}{5+10}\ \mu A$ Iv (50°C) > 147μA

Table 5-1 (Continued)

8. Determine IP and IV in normal condition ● $Ip(25°C) < \frac{Ip(Tmin)}{\text{Typical value at Tmin}}$ ● $Iv(25°C) < \frac{Iv(Tmax)}{\text{Typical value at Tmax}}$ Typical values of Ip and Iv are found in Fig. 6-7(a) and (b), respectively. The required R_G curve must meet the condition of $R_G \leq 0.1R_T$.	8. From the curve of R_G=10KΩ in Fig.6-7, we obtain Ip(-25°C) =2.8μA typical Therefore ● $Ip(25°C) < \frac{39}{2.8\mu A}$ Ip(25°C) < 14μA ● $Iv(25°C) > \frac{147}{0.8\mu A}$ Iv(25°C) > 184μA
9. Determine $R_G$min from Fig.6-3(a) and the condition in step 8. $R_G$min = ?	9. Since Ip(2C)<14μA, then $R_G$min ≈ 700Ω.
10. Determine the minimum value of I_G from Fig.6-3(b) and item in step 8. Then calculate $R_G$max. $R_G max \approx \frac{\eta V}{I_G(min)}$	10.Iv(25°C)>184μA $I_G$min ≈4.5 mA $R_G max = \frac{0.63 \times 12}{4.5} = 1.68K\Omega$
11. Select R_G value between $R_G$max and $R_G$min. Since the power dissipation is inversely proportional to R_G, a large R_G is required.	11. Use R_G=1.2KΩ
12. Calculate R2 and R1. $R2 = \frac{R_G}{\eta}$ $R1 = (\frac{\eta}{1-\eta})\ R2$	12. $R2 = \frac{1.2K\Omega}{0.63} = 1.9K\Omega$, pick 1.8KΩ $R2 = (\frac{0.63}{1-0.63}) \times 1.8K\Omega$ = 3.0KΩ, use 3KΩ
13. Draw the circuit.	13. As shown in Fig.5-9.

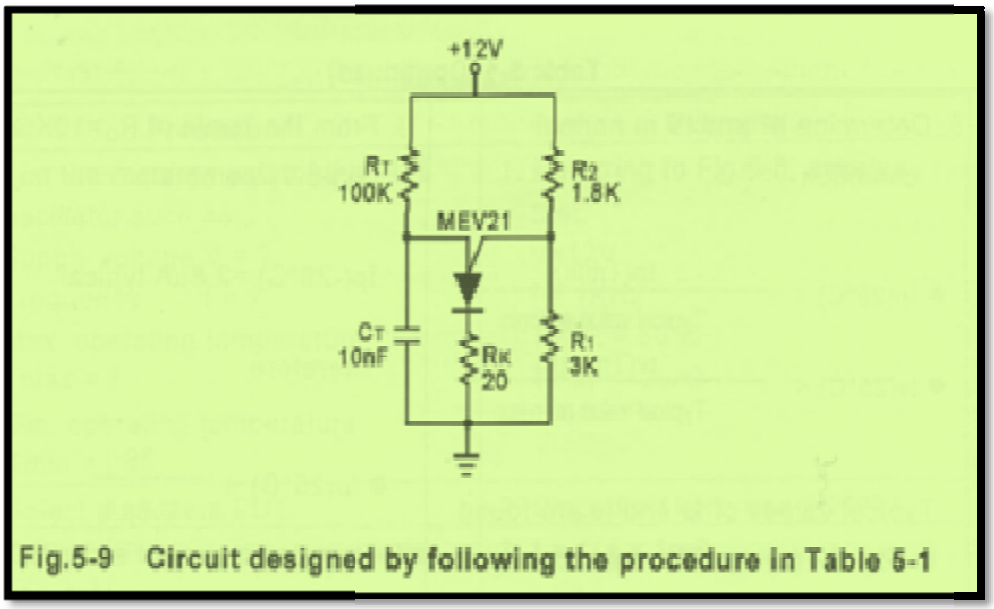


Fig.5-9 Circuit designed by following the procedure in Table 5-1

Quick Design for UJT Relaxation Oscillator

Table 5-2 Quick design for 2N6027(MEU21)

RT \ CT / R2(max)	1nF	10nF	≥ 100nF
10K		300	330
12K		330	390
15K	300	390	470
18K	330	390	560
22K	390	470	680
27K	470	560	820
33K	560	680	1K
39K	680	820	1.2K
47K	820	1K	1.5K
56K	1K	1.5K	1.8K
68K	1.2K	1.8K	2.2K
82K	1.5K	2.2K	3.3K
100K	2.2K	3.3K	4.7K
120K	2.7K	3.9K	5.6K
150K	3.3K	4.7K	6.8K
180K	4.7K	6.8K	10K
220K	5.6K	8.2K	12K
270K	8.2K	12K	18K
330K	12K	18K	27K
390K	18K	27K	39K
470K	22K	33K	47K
560K	33K	47K	68K
680K	47K	68K	100K
820K	68K	100K	150K
1M	82K	120K	180K

There are a number of complicated calculations in Table 5-1 for designing a PUT oscillator. Fortunately, with known R_T and C_T values, the maximum value of R2 can be easily determined by using the tables provided by device manufactures. Tables 5-2 and 5-3 are suitable for these conditions: (1) supply voltage less than 25V, (2) ambient temperature at 25°C. At 50°C, the values of R2 column must be times 0.7.

If R1=1.7R2, then $t \approx R_T C_T$.

Table 5-3 Quick design for 2N6028(MEU22)

RT \ CT / R2(max)	1nF	10nF	≥ 100nF
22K			330
27K		300	390
33K		330	470
39K		390	560
47K		470	680
56K	390	560	820
68K	470	680	1K
82K	560	820	1.2K
100K	820	1K	1.5K
120K	1K	1.2K	1.8K
150K	1.2K	1.5K	2.2K
180K	1.5K	1.8K	2.7K
220K	1.8K	2.7K	3.3K
270K	2.7K	3.9K	4.7K
330K	3.3K	4.7K	6.8K
390K	4.7K	6.8K	10K
470K	6.8K	8.2K	15K
560K	8.2K	12K	18K
680K	10K	15K	22K
820K	12K	18K	27K
1M	18K	27K	39K
1.5M	33K	47K	68K
2.2M	58K	82K	120K

PUT Timer Circuit

A PUT timer circuit is essentially a relaxation oscillator with a long period of oscillation. Since the important parameters of the PUT are programmable, the design of the PUT timer circuit is more flexible than the UJT timer circuit discussed in experiment 3.

The design of PUT timer circuit is similar to that of the PUT relaxation oscillator. For precise timing, the timing C_T in PUT timer circuit requires the capacitor with very low leakage current. In addition, values of I_P, I_V and I_{GAO} should be as small as possible.

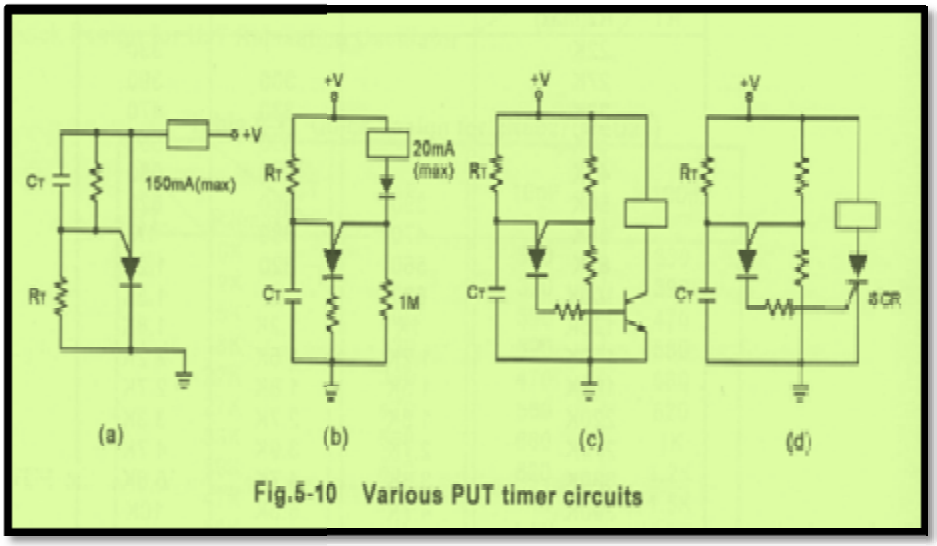


Fig.5-10 Various PUT timer circuits

Various physical PUT timer circuits are shown in Fig. 5-10. The circuit of Fig. 5-10(a) is a basic PUT delay switch circuit. The value of RT in circuits of Figs. 5-10(b) and (c) should be small enough to provide a sufficient holding current to the PUT. In the circuit of Fig. 5-10(d), no holding current is need for the PUT once the SCR is turned on, therefore the time constant R_TC_T can be used as above one hour.

A special timer circuit shown in Fig. 5-11 is a PUT timer circuit with timing network

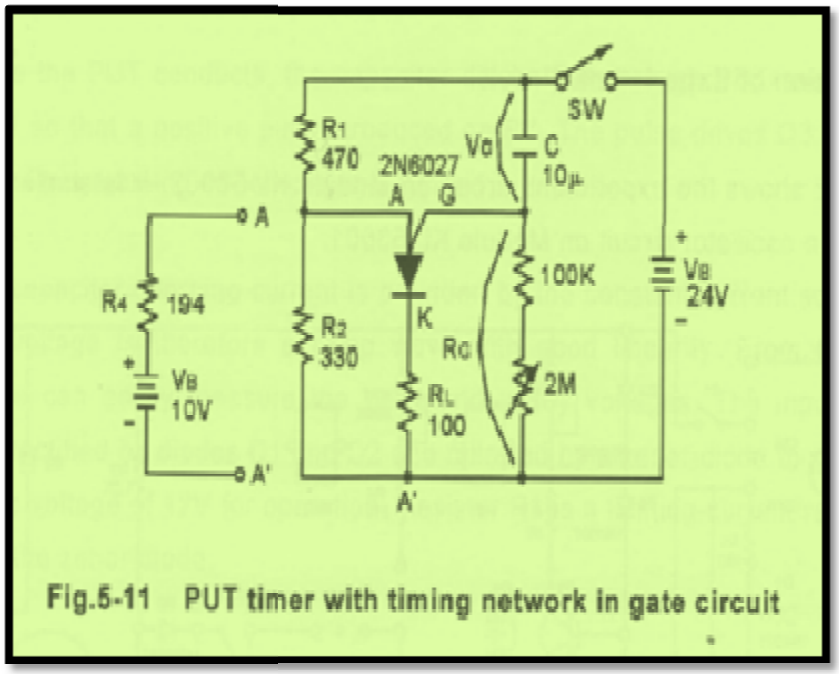


Fig.5-11 PUT timer with timing network in gate circuit

1. When SW is closed, the anode voltage is calculated by the voltage-divider formula:

$$V_A = V_B \times \frac{R2}{R1 + R2} = 10V$$

Since the capacitor can not charge at that instant SW closed, $V_C=0$ and $V_G>V_A$ so that the PUT is off.

2. When the capacitor is charged up and V_G is reduced to meet $V_A>V_G$, the PUT switches on. The charging time is calculated by

$$T = R_G\, C \ln \frac{R1 + R2}{R2}$$

3. If $R_G=1.1M\Omega$, the charging time will be

$$T = 1.1\times10^{6}\times10\times10^{-6}\ln\frac{470+330}{330} = 11\ln2.43 = 10sec$$

Description of Experiment Circuit

Fig. 5-12 shows the experiment circuit on Module KL-53002. It is similar to the UJT relaxation oscillator circuit on Module KL-53001.

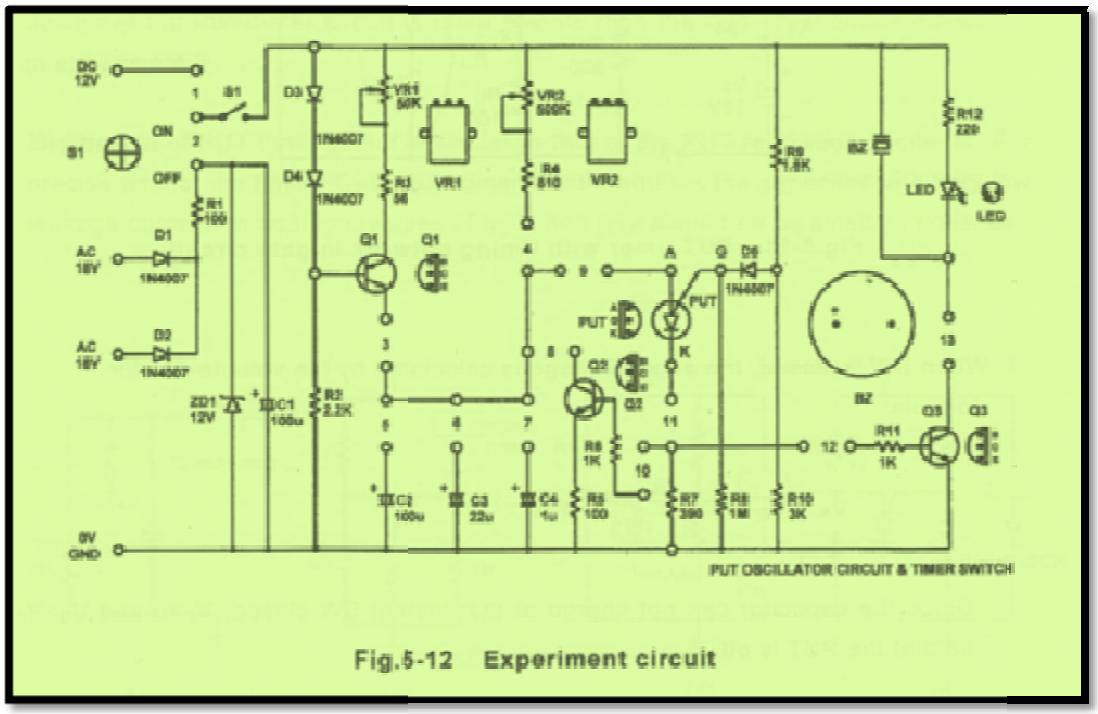


Fig.5-12 Experiment circuit

The gate voltage of the PUT is determined by the voltage-divider rule. The η of the PUT is found as

$$\eta = \frac{R10}{R9 + R10}$$

The functions of diode D5 and resistor R8 are introduced in the circuit of Fig. 5-2. As mentioned above, diode D5 is used to reduce the I_P value and for thermal stability. The period of oscillation is calculated by Eq. (5-2). The constant-current source consisting of Q1, D3 a D4 provides the charging current to the capacitor. When the capacitor voltage reaches the peak voltage of the PUT; that is $V_A = V_G + V_T$, the PUT is turned on. The period of oscillation is calculated by $T=(R4 + VR2)\times C\times \ln[1/ (1 - \eta)]$. If $\eta=0.63$, then $T=(R4+VR2)\times C$.

When once the PUT conducts, the capacitor discharges through PUT and the load resistor R7 so that a positive pulse produced on R7. The pulse drives Q3, LED and buzzer on. Thus a timing switch circuit is formed.

Since the capacitor charging current is provided by the constant-current source, the capacitor voltage is therefore a ramp wave with good linearity. From this ramp voltage, we can easily measure the peak and valley voltages. The input 18-Vac voltage is rectified by diodes D1 and D2 and followed by a zener diode to supply the required dc voltage of 12V for operation. Resistor R1 is a limiting-current resistor for protecting the zener diode.

EQUIPMENT REQUIRED

1 — Power Supply Unit KL-51001
1 — Isolation Transformer KL-58002
1 — Module KL-53002
1 — Oscilloscope

PROCEDURE

1. Connect the DC12V-0V input terminals on Module KL-53002 to DC12V-0V output terminals on Power Supply Unit KL-51001 - KL-58002. Set S1 to OFF position.

2. Insert connect plugs in positions 1, 4, 7, 9, 11, 12, and 13. Turn VR2 fully CCW to get the minimum value. (If circuit can't oscillate,turn VR2 CW slowly.)

3. Calculate the value of η of the PUT oscillator by the equation below.

$$\eta = \frac{R10}{R9 + R10} = \frac{3K}{1.8K + 3K} = 0.63$$

The period of oscillation T = R4 × C4 = _____

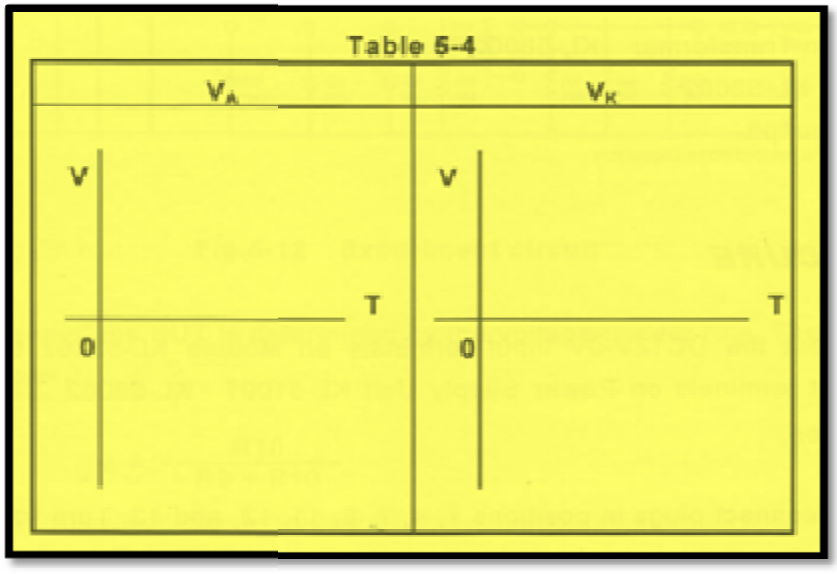
4. Turn on the power. Using a stopwatch, count and record the time interval from setting S1 ON to LED and BZ ON. (When T is near ms, it can't be visually saw the reaction of LED. You have to connect an oscilloscope)
T= _____

5. Does the measured T agree with the calculated T? _____

6. Using the oscilloscope, measure and record the voltage waveforms at the anode (A) and cathode (K) of the PUT in Table 5-4. Measure and record the period of oscillation.
T= _____

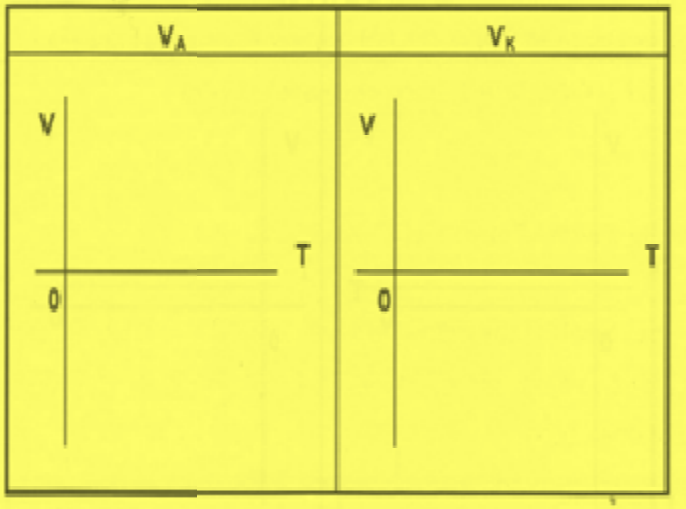
Does this T value agree with the T values in steps 3 and 4.

Table 5-4



7. Slowly turning VR2 toward the right, observe and record the change of T. When VR2 reaches at the most right end (maximum value), measure and record the voltage waveforms at the anode (A) and cathode (K) of the PUT in Table 5-5 using the oscilloscope.
Record the period of oscillation. T= _____

Table 5-5



8. Calculate the period of oscillation.

T=(VR2 + R4) × C4 = _____

9. From Table 5-4, observe and record the values of V_P and V_V.

V_P = _____ V , V_V = _____ V

10. Remove the connect plug from position 7 and insert it in position 6 or 5. Set S1 to OFF and turn VR2 fully CCW.

11. Repeat steps 3 through 9 and record the results in Tables 5-6 and 5-7.

Table 5-6

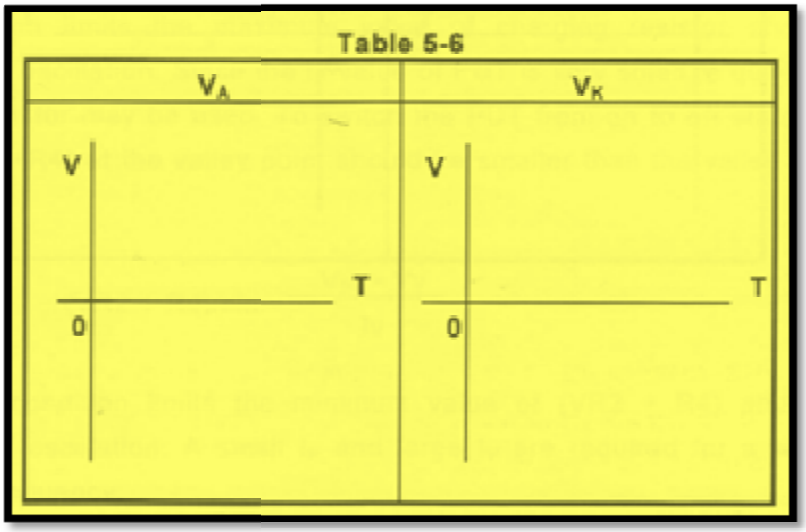
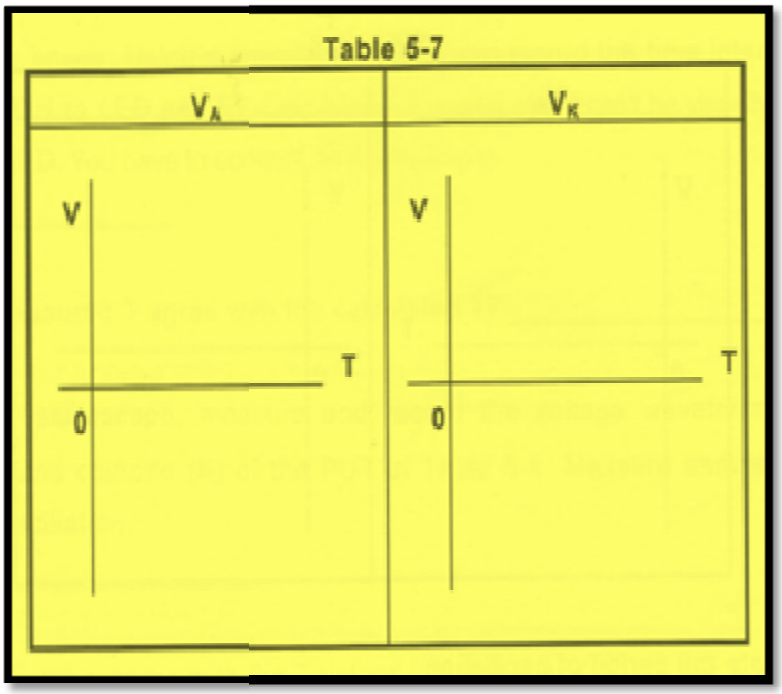


Table 5-7



12. Set S1 to OFF position. Turn VR1 fully CCW. Insert connect plugs in positions 1, 4, 7, 8, 9, 10, 11, 12, and 13.

13. Repeat steps 3 through 9 and record the results in Tables 5-8 and 5-9.

Table 5-8

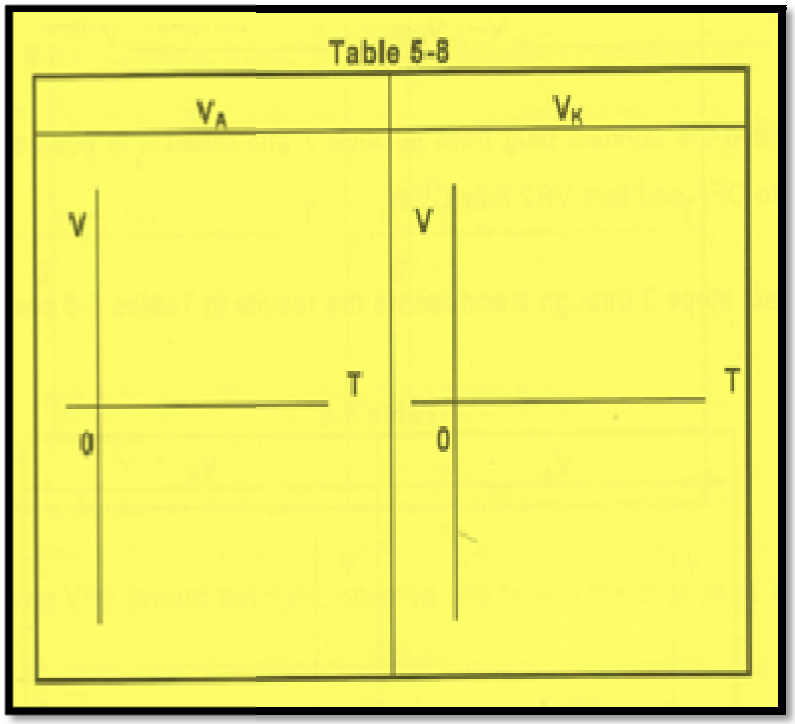
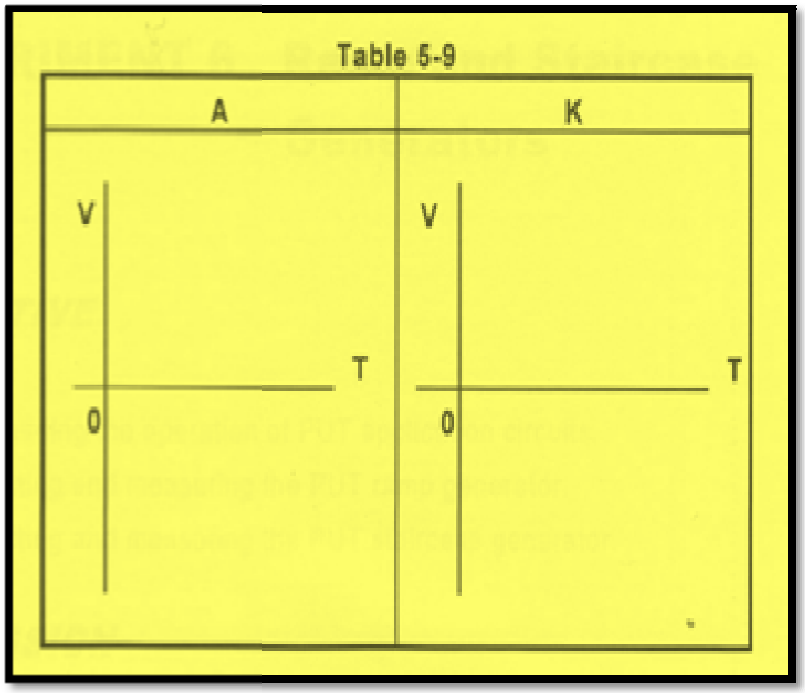


Table 5-9



CONCLUSION

The resistance between the anode and cathode of the PUT in conduction is lower than the resistance between the emitter and base one of the UJT in conducting. Therefore the discharging time is shorter and the pulse voltage on the cathode resistor R7 is higher and narrower in a PUT relaxation oscillator. To switch the PUT from off to on state, the anode current in (VR2+R4) at the peak point must be larger than I_p. That is,

$$(VR2 + R4)max = \frac{V_{BB} - Vp}{Ip}$$

This condition limits the maximum value of charging resistor and the lowest frequency of oscillation. Since the I_p value of PUT is very small, a quite value of the charging resistor may be used. To switch the PUT from on to off state, the current flow in (VR2+R4) at the valley point should be smaller than the valley current. That is,

$$(VR2 + R4)min = \frac{V_{BB} - Vv}{Iv}$$

The above condition limits the minimum value of (VR2 + R4) and the highest frequency of oscillation. A small I_p and large I_v are required for a wide range of oscillating frequency.