Development of Design and Testing Approaches of Embedded Passive Structure for High Frequency Applications

A THESIS
SUBMITTED TO THE FACULTY OF THE GRADUATE SCHOOL OF THE UNIVERSITY OF MINNESOTA

BY

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IN PARTIAL FULFILMENT FOR THE DEGREE OF MASTER OF SCIENCE IN ELECTRICAL ENGINEERING (M.S.E.E.)

October 2005

Acknowledgements

I wish to express my sincere thanks and appreciation to my adviser Dr. Rhonda Franklin Drayton for her guidance and support that made the completion of this work possible. Her constant challenge and encouragement throughout this endeavor allowed me to maintain my focus even when the outcome appeared quite bleak.

I would also like to thank my committee members Dr. Ramesh Harjani and Dr. Norman Meyers for their time and effort.

I will always treasure the fond moments and experiences of sharing a lab with a group of wonderful and diverse colleagues. These included Issac Itotia, Riki Banerjee, Can Akgun, Ethan Miller, Dan Kollmann, Chenglin Zheng, Sitha Chuum, Shreyasse Kambale, Napol Chaisilwattana, Hoseng Kim and Young Seek Cho. The personal and professional discussion with Issac Itotia and Riki Banerjee helped me navigate through puzzling problems and processes. Ethan Miller provided the SEMs displayed in this document along with valuable discussions on fabrication processes. I am also grateful for the assistance I received from Hoseng Kim with SEMs.

The help of people in the department is also greatly appreciated. I would like to specifically thank Dr. Babak Ziaie for the use of his laboratory and fabrication equipment without which it would have been difficult for some of this work to be realized. I would also like to thank Tingrui Pan for his assistance and valuable advice on the fabrication process utilized in this work. My thanks also go to Dr.

Stephen Campbell and Dr. Emad Ebbini for allowing the use of their laboratory and measurement equipment.

The staff of the Nanofabrication Center at the University of Minnesota including Kathy Burkland, Suzanne Miller, Tony Whipple, Kevin Roberts and Mark Fisher was an invaluable resource. I especially like to thank Kevin Roberts for his help with dicing and the chemical mechanical polishing process, Suzzane Miller for her help with dicing, and Mark Fisher for his help with wirebonding.

This work was supported by a grant provided by the National Science Foundation under the President Early Career Award for Scientists and Engineers Award (ECS-9996017). I also like to acknowledge Rogers Corporation for donating the duroid material used in this work.

The help of Marcus Drayton who has been a friend and mentor for the past five years is invaluable. His professional and personal advice has guided me throughout the years.

Finally, I would like to acknowledge my family and close friends whom have been a valuable source of support throughout my life. I thank my parents for believing in me and encouraging me to pursuit my dreams even when faced with the greatest of challenges. My mum in particular, for the constant reassurance she has always offered to me along the way. Thanks go to my sisters Emilia and Evelyn for their constant support and great humor. The shared experience and motivation of my sister Evelyn was very helpful in difficult times.

Abstract

This work explores the use of substrate machining in the development of high and low impedance structures. It also examines test method approaches for characterizing embedded components.

A novel approach for developing low impedance structures using embedded conductors for compact circuit design is examined in coplanar waveguide architecture. It is implemented in high resistivity silicon substrate using silicon microfabrication techniques. Demonstration of compactness using a low pass filter attains a size reduction of 23% compare with an equivalent surface design implementation. There is also an improvement in other characteristics such as the stopband performance that is 10 dB lower than that of the surface filter.

Mixed dielectric constant material is considered for use in the development of microwave circuits. The reduction of effective dielectric constant of a high dielectric constant material using a bilayer approach with air is demonstrated. Measured results indicated approximately 50% reduction in effective dielectric constant for a 40% air (ε_r=1.0) and 60% duroid (ε_r=10.2) composition. Simulations show promising results in the development of passives such as a microstrip filter designed with mixed dielectric. Filter properties are varied by altering composition of mixed dielectric while keeping circuit dimensions constant.

Test methods using different interface approached indicate that both discrete and integrated testing of embedded passives is realizable. Though integrated

testing is repeatable, measured result indicated that careful consideration has to be given to the feeding structure used to prevent degradation of performance.

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Chapter 1: Introduction

1.1 Motivation and Background

The need to obtain smaller electronic devices has been driving the development of integrated circuit (IC) technology for some time. This has resulted in digital circuits with transistor numbers approaching a billion [1], to address computing markets that require machines to be smaller, lighter and offer more information handling capacity.

Also growing are communication markets with demand for smaller and lighter devices. In this area, a revolution in analog circuit design is occurring for low frequency design methods to be pushed to radio frequency (RF) operation. Also, efforts to produce smaller IC and board level circuits have increased in recent years. To meet these demands, several approaches including multilayered circuits using layered board technology ([2], [3],) and monolithic integrated circuits (MMIC) [4] have been developed.

In this decade is the drive to achieve high level integration of computers, connections, sensors, etc. as it does not only make devices smaller but also cheaper. Emerging trends combine various circuits such as active, passive circuits and microelectromechanical (MEM) devices to form integrated systems. This has introduced concepts such as system on a chip (SOC) ([5], [6]) and System on a package (SOP). In system on a chip, all devices including passives and MEMs device are fabricated on chip while in system on a package approach [7], passives are fabricated off chip on a common platform. As such, the size

associated with passives devices, unlike active devices has become a primary issue to address. While active devices are regularly scaled down, passives present different challenges. Researchers have sought several approaches to reduce devices such as folding to generate compact geometric shapes while retaining functionality of the device.

For the size of passives and hence integrated systems to reduce further, new design approaches will have to be considered. Currently, most passive designs only utilize the surface area of the fabrication platform but using the volume to develop embedded passive structures will be a more efficient way to use the fabrication platform. The use of multi-functional devices to reduce the physical area required and hence result in a smaller device will also have to be considered. For example a transmission line acting as a feed from an antenna could have filtering characteristic eliminating the need for a dedicated filter further down the circuit to eliminate spurious signals.

1.2 Thesis Overview

The goal of this thesis is to develop fundamental approaches to address RF passive device size reduction utilizing three-dimensional substrate manipulation techniques. In chapter 2, fundamentals are presented on some of the embedded circuit design basics and development. Chapter 3 presents a novel approach to size reduction of passives using a three dimensional embedding method. It also addresses the utilization of substrate machining in board level designs to create a multilayer substrate. Finally, chapter 4 addresses the test methodology for

embedded devices on lossy silicon substrate as well as the performance of different interface methods.

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Chapter 2: Behavior of RF Signals on Silicon-Based Transmission Lines

2.1 Introduction

The transfer of Radio Frequency (RF) signals or waves is achieved either through space or along guiding structures. Several guiding structures currently exist for this purpose. Some of these (i.e. coax) are capable of transferring signals with broadband frequency operation from DC to RF bands. While others (i.e. waveguides) are band limited.

This chapter discusses the general properties of transmission lines. It introduces the operation of two specific planar transmission structures, microstrip and coplanar waveguide. The effect of implementing these structures in certain material mediums is discussed followed by an examination of circuit design using transmission line structures.

2.2 Ideal Transmission Line Behavior

At low frequencies, the wavelength of electrical signals is much greater than the physical length of a circuit; therefore single wires can be used to establish connection between two points on the circuit and thus viewed as lumped elements. As frequency increases and the physical length of the circuit become comparable to the guided wavelength (λ_g) of the signal, standard voltage theory becomes inapplicable. A specific wire configuration is capable of transmitting a signal at different wavelengths; as a result, the voltage can vary greatly along the

length of wire. The voltage and current on the structure is a variable of time and location i.e. $V(l,t)$, $I(l,t)$, where l is the location in the direction of propagation and t is time.

At these frequencies, the use multiple (i.e. a minimum of two) wire lines known as transmission lines are required. The standard representation for a transmission line is shown below in Figure 2.1. A short section of this transmission line without loss effects and length $\Delta\ell$ can be represented in terms of discrete elements as shown in Figure 2.2.

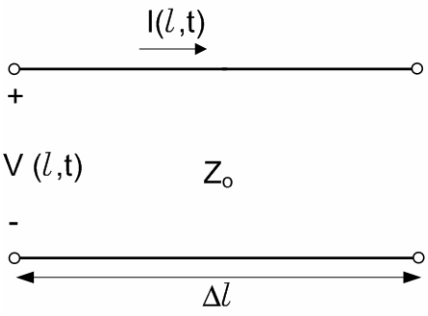

Figure 2.1. Standard representation of a short section of transmission line with length $\Delta\ell$.

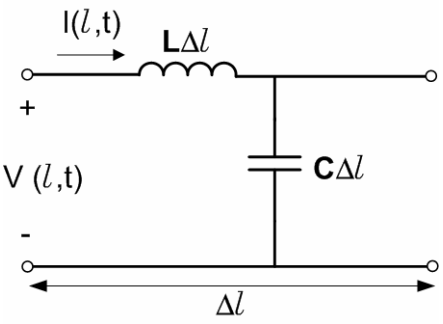

Figure 2.2. Discrete element model of a short section of lossless transmission with length $\Delta\ell$. L is inductance per unit length while C is capacitance per unit length.

In Figure 2.2 the ratio of the inductance of the structure to its capacitance (Eqn. 2.1) is referred to as its characteristic impedance (Z_o).

$$Z_o = \sqrt{\frac{L}{C}} \tag{2.1}$$

However, when loss due to the conductors and substrate is accounted for, the circuit is modified to indicate metal resistance (R) and dielectric conductance (G) as shown in Figure 2.3. Accordingly, the transmission line model in Figure 2.2 is referred to as a lossless model while that in Figure 2.3 is referred to as a lossy model.

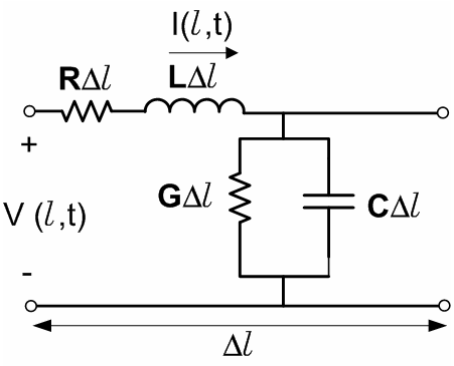

Figure 2.3. Modified discrete element model of a short section of transmission line with length $\Delta\ell$ indicating circuit metal resistance (R) and dielectric conductance. (G).

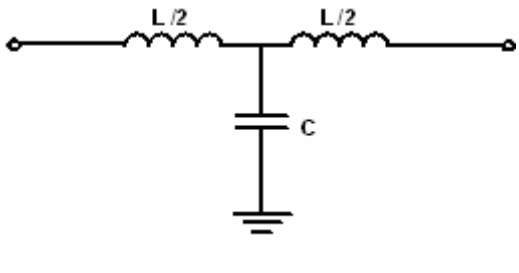

Figure 2.4. T-network model representation of a section of lossless transmission line with inductance (L) and capacitance(C).

A length of ideal transmission line can also be represented as a T-network equivalent circuit as shown in Figure 2.4. When the length $\Delta\ell$, of the transmission line structure represented in Figure 2.4 is electrically short ($\leq \lambda_g/10$), it can be substituted for an inductor or capacitor in a circuit. Extensive details on how this representation is done can be found in [1].

2.3 Planar Transmission Lines

While a variety of planar transmission lines can be used on silicon, the most popular and easily fabricated designs are the microstrip and coplanar waveguide (CPW) structures shown in Figure 2.5 (a) and (b) respectively.

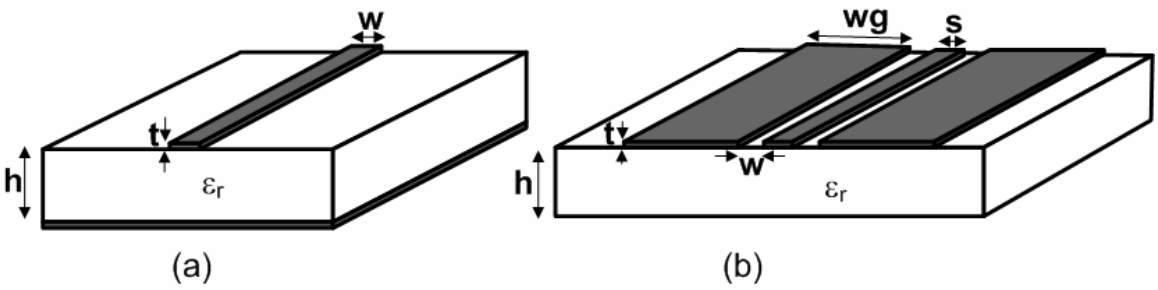

Figure 2.5. Illustration of (a) planar microstrip and (b) Conventional planar CPW transmission line structures.

The structures are usually designed to operate over a range of frequencies maintaining a single or dominant mode of propagation. This mode of operation for these structures is usually referred to as quasi-transverse electromagnetic (TEM). In a pure TEM mode of propagation, the electric and magnetic field of the structure are perpendicular to each other and the direction of signal propagation. In quasi-TEM structures, the components of the fields are in two material mediums which propagate with different velocities resulting in a small amount of

the field components along the direction of propagation. However, the field distribution closely resembles that of a pure TEM propagation hence the name quasi-TEM.

2.3.1 Microstrip

The microstrip is the most widely used transmission line in the design of circuits. It has been around for several decades [2] and the theory behind its operation is well understood. It can be divided into two main categories planar and non-planar. An illustration of a planar microstrip is shown in Figure 2.5(a). This transmission line has the ability to attain a very high line density in a limited area compared with other transmission lines such as the coplanar waveguide. This makes it quite attractive in circuit design. Its limitations however are it requires vias which limit bandwidth operation for shunt connections and has high coupling between adjacent signal lines. The impedance property of this structure varies with its signal conductor width (w) and the substrate height (h).

The planar microstrip is capable of supporting various propagation modes. The primary mode of operation is a quasi-TEM mode. An illustration of the quasi-TEM field distribution of a planar microstrip propagating in this mode is shown in Figure 2.6. In the quasi-TEM approximation, the combined effect of a two material media (dielectric constant (ε_r) of the substrate material and of air) is represented by a single homogenous medium with a dielectric constant referred to as an effective dielectric constant (ε_e), approximated by the formula [3] in Eqn. (2.2).

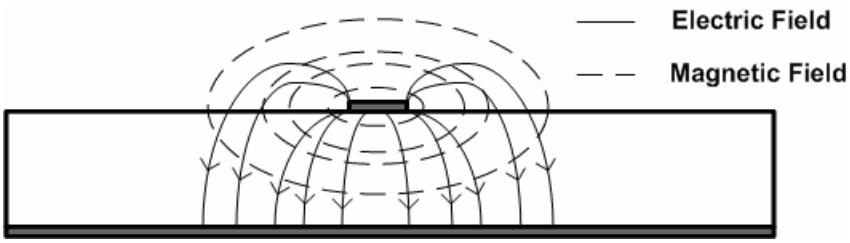

Figure 2.6. Illustration of quasi-TEM dominant mode Electric and Magnetic field distribution for a planar microstrip transmission line.

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 10\frac{h}{w}\right)^{-ab} \tag{2.2}$$

In the equation, a and b are constants dependent on the dimensions and of the microstrip and the dielectric constant of the substrate, h is substrate height and w is conductor width.

Secondary modes can exist on the microstrip line, namely transverse electric (TE) with a magnetic field component in direction of propagation or transverse magnetic (TM) with an electric field component in direction of propagation. The frequency at which these modes propagate is dependent on the thickness of the substrate (h). Therefore, in order to obtain a wideband structure, the microstrip has to be fabricated on a relatively thin substrate.

2.3.2 Coplanar Waveguide

The coplanar waveguide (CPW), though not as popular as the microstrip, is another planar transmission line structure used in the design of circuits. It can be classified into three main categories (a) conventional, (b) conductor-backed and (3) micromachined. These different types of CPW structures are extensively

addressed in [4]. One of the advantages of the CPW over microstrip is its ability to easily integrate shunt element connections without the need for vias. The fabrication process for a conventional planar CPW is also simple since all conductors are on the surface, as illustrated in Figure 2.5(b). The center conductor, width (s) is the signal line while the finite conductors, width (w_g) on either side are ground planes. The width (s) of the central conductor and spacing to the grounds (w) determine the inductance and capacitance of the structure and hence its characteristic impedance. CPW design tools such as ADS linecalc [5] based on closed-form formulas are used to obtain approximate dimensions for certain impedance requirements. Some design models assume infinite ground plane widths [5]. Closed form formulas are obtained using techniques such as conformal mapping [4], [6], [7], and iterative methods such as the relaxation [8] and hybrid method [9]. More accurate design approaches use techniques such as spectral domain analysis [10], [11] that account for frequency dependence. In this work, finite width ground plane structures are used in the design of CPWs. Work done by several authors has shown that the finite width of the ground plane affects the loss properties [12], [13] of the structure.

A conventional planar CPW such as that in Figure 2.5(b) is capable of supporting various modes of propagation among them TE and TM modes. Since multimoding consumes additional energy, the CPW is usually designed to support a single dominant quasi-TEM mode of propagation to minimize losses. An illustration of the quasi-TEM field distribution for this mode is shown in Figure 2.7. Secondary modes in CPWs are usually introduced in the structure above

certain frequencies; therefore the maximum allowable operating frequency must be below this value.

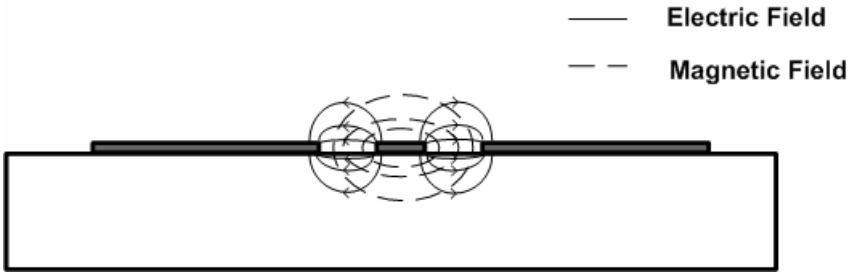

Figure 2.7: Illustration of quasi-TEM dominant mode Electric and Magnetic field distribution for a planar coplanar waveguide transmission line.

Other potential modes that could be generated on CPWs, include a surface wave mode and slotline mode. The surface wave mode is generated when propagating waves are reflected from the backside of the substrate, therefore this mode is dependent on the thickness of the substrate. The thinner the substrate, the less likely it is to encounter this mode. For circuits designed to operate over a wide bandwidth however, it is almost impossible to avoid this mode. The slotline mode is generated when the potential between the ground planes become unequal. Several approaches such as wirebond air bridges to equate the ground potential [14] and upper and/or lower grounded conducting shields are used to eliminate this mode [15].

There are several additional avenues for loss in a CPW structures other than modes. Assuming dominant mode of operation, these include conductor loss, dielectric loss as well as radiation. Radiation loss has being shown to increase as the separation distance of the ground planes $(s+2w)$ increase [16]. In a low-loss substrate such as high resistivity silicon, the loss at low frequencies is usually

dominated by conductor loss while at higher frequencies it is dominated by radiation and dielectric loss.

2.4 Resistivity Implication

The loss property of fabricated microstrip and coplanar waveguide structures is dependent on several factor among which is the substrate resistivity. In traditional high resistivity semiconductor substrate such as gallium arsenide (GaAs) with resistivity in the millions of Ω-cm, the substrate loss tends to be very low. However, when these structures are implemented in silicon, the loss characteristics vary greatly. Measured results by Ponchak et al [17], indicates an attenuation of approximately 4.0 dB/cm on GaAs at 20 GHz for CPW with dimensions s=10 μm and w= 9 μm. The attenuation for the same structure on 400-700 Ω-cm silicon is almost twice the values on GaAs at 7.0 dB/cm. When the resistivity of the silicon substrate is increased to 2.5 KΩ-cm, the attenuation is approximately equivalent. Heinrich et al [18] showed similar results for CPW with a 20 μm width center conductor and 15 μm gap spacing. The attenuation decreases by a factor of approximately five at 20GHz with an increase in resistivity from 30 Ω-cm to 3000 Ω-cm. The attenuation of the GaAs CPW is approximately equivalent to that on silicon with a 3000 Ω-cm resistivity. This decrease in attenuation with increased silicon resistivity is also corroborated by Reyes et al [19] for CPWs with signal line width of 10 μm and gap spacing of 30 μm. It shows similar loss characteristic for 3-7 KΩ-cm silicon and 10-40 MΩ-cm GaAs with 2 μm oxide/nitride insulator layer. The excess loss in the low resistivity

silicon CPWs is due to the conductive nature of the substrate allowing energy to be dissipated into the substrate. When the resistivty of silicon is increased the loss decreases greatly in each case. Therefore, the use of high resistivity substrates in the implementation of high frequency designs in silicon is essential for loss reduction.

2.5 Circuit Design Implication

2.5.1 Equivalent Lumped Element Behavior

At relatively high frequencies, circuit design using discrete elements is all but impossible due to the overwhelming parasitics of these structures. This is where distributed design using transmission lines become useful in implementing circuits. As shown in the ideal representation of a transmission line model, Figure 2.4, the structure is made of a shunt capacitor and series inductor. When the length of the line is electrically short, it can easily be used to approximate either an inductor for a high impedance structure or capacitors for a low impedance structure. Since a parasitic capacitance is present in every distributed inductance implemented using a transmission line and vice versa, the accuracy of the implementation will depend on minimizing these parasitics.

2.5.2 Interconnect Response

The most basic use of a transmission line structures is as an interconnect between two or more devices. When used in this capacity, the ability to obtain dense networks with reasonable isolation between individual lines is important. Generally, CPW tends to have greater isolation than microstrip lines due to their

ground planes separating adjacent structures. Low loss structures are also essential to maintain signal integrity primarily in cases where connected devices are separated by a wide distance. The frequency response of interconnects are usually analyzed using S-parameter measurements. The S_{12} or insertion loss is a measure of the total loss of the structure due to conductor, dielectric and radiation. The S_{11} or return loss measures the level of impedance matching relative to a specified reference impedances.

2.6 Summary

The operation of the planar microstrip and coplanar waveguide transmission line has been briefly discussed. Properties including the quasi-TEM nature of each line were highlighted along with its advantages and limitations. The contribution of substrate resistivity on the overall loss of these structures, specifically the planar CPW when fabricated on silicon was also mentioned. Use of transmission lines in general for the distributed implementation of discrete element LC circuits and its accuracy were highlighted. Next, a novel CPW structure with signal and ground plane lines embedded into the substrates is used to design a stepped impedance filter in chapter 3. This effect of embedding the conductors of the CPW structure is addressed in detail, highlighting its advantages over a conventional planar CPW such as that discussed in section 2.3.

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Chapter 3: Embedded Design Methods for Low and High Impedance Lines in High Resistivity Substrate.

3.1 Introduction

The design of low impedance lines require very high capacitance with low inductance. This can theoretically be seen from the lossless impedance formula shown in Eqn. 2.1. The design of high impedance transmission lines on the other hand requires the exact opposite. In transmission line architectures such as CPW, this means very narrow gap spacing for low impedances while very narrow conductors are required for high impedances lines in microstrip. However, fabrication tolerances limit the extent to which these narrow dimensions can be fabricated and/or repeated.

In this chapter, novel approaches that attain low and high impedances lines through capacitance modification of a structure are discussed. In order to attain higher capacitance embedded conductors are utilized whereas for lower capacitance values mixed dielectric materials are used. As a demonstration problem, a stepped impedance filter is realized using embedded conductors. The design of a photonic bandgap filter using mixed dielectric material is also examined using simulation.

3.2 Coplanar Waveguide Design Methods

In CPW structures, capacitance is increased using approaches such as overlapping MEMS fabricated using out of plane conductors [1], [2] and thin dielectric separation layers between surface and underpass conductors [3]. The approach in [1] and [2] reduces loss by having air as the dielectric material. The method utilizing underpass conductors in [3] has been used to realize impedances as low as 7.5Ω. In general, the lower impedance limit is set by mechanical strength and realizable gap separation constraints. These structures rely on an increase in effective area and/or smaller gap spacing to attain higher capacitance values and hence a lower impedance. This increased capacitance can be used to improve the performance of structure such as filters, couplers and other transmission line based structures. A partially embedded and fully embedded conductor CPW approach was examined to obtain low impedance lines.

3.2.1 Partially Embedded Coplanar Waveguide

To obtain a larger capacitance in a CPW architecture, the effective capacitance area (A) of a structure or effective dielectric constant (ε_{eff}) of the structure has to be increased (Eqn. 3.1). Alternatively, the reduction in the separation distance also produces a larger capacitance.

$$C = \frac{\varepsilon_{eff}\varepsilon_o A}{d} \tag{3.1}$$

where C=capacitance, A=effective area, d=gap spacing, ε_{eff} = effective dielectric constant, ε_o =permittivity of free-space.

The partially embedded coplanar waveguide (PECPW) design uses embedded ground planes as illustrated in Figure 3.1 to obtain a higher effective dielectric constant and area. The embedded ground planes attract more electric field lines into the dielectric substrate (Figure 3.2) compared to a regular CPW design. This increases the effective area of the structure and hence its capacitance.

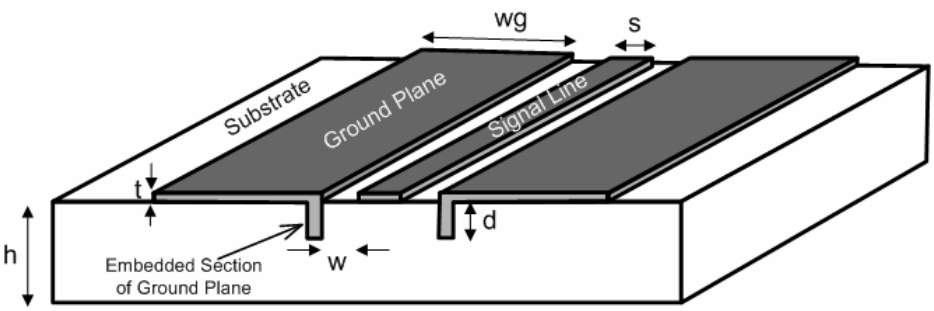

Figure 3.1. Illustration of a partially embedded coplanar waveguide (PECPW) with vertically embedded ground plane conductors to a depth, d. The substrate height is h, ground plane width w_g, signal line width s, gap spacing w and metal thickness t.

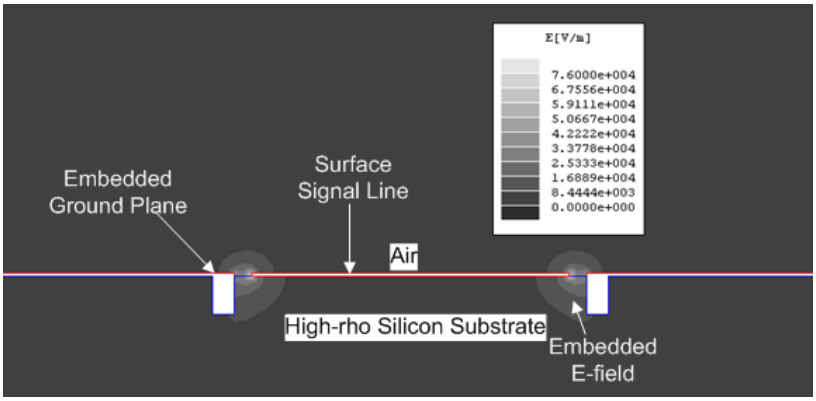

Figure 3.2. Cross sectional view of Maxwell 2D simulated electric field plot of a PECPW with inner ground-to-ground spacing (s+2w) of 500μm, d =60μm, s =450 μm and w =25μm. The CPW is simulated on high resistivity (rho) silicon substrate with dielectric constant of 11.7.

The extent to which the effective dielectric constant or capacitance changes vary with depth (d) of the structure for a PECPW structure with a fixed ground spacing (s+2w). In general, the effective dielectric constant increases the further the ground planes are embedded into the substrate as seen in Figure 3.3. The increase appears to be more prominent when d is less than the gap (w) of the PECPW. For a PECPW with a gap spacing of 10 μm, 14% of the 19% increase in effective dielectric constant obtain at a d of 90 μm is achieve in the first 30 μm. The effective dielectric constant values only vary slightly with CPW gap spacing (w) in this architecture.

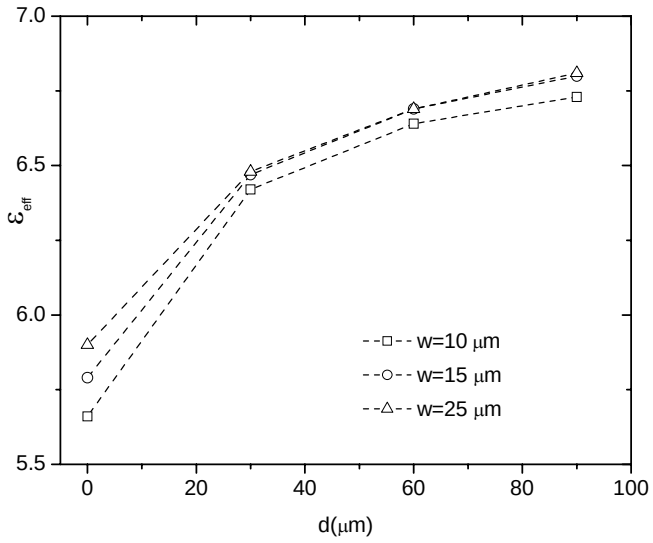

Figure 3.3. Simulated [4] results showing change in effective dielectric constant (ε_{eff}) of PECPW with embedded depth (d) as gap spacing (w) is varied. The PECPW structure in this simulation has fixed inner-to-inner ground spacing (s+2w) of 500 μm.

The increase in effective dielectric constant value with d is reflected in the impedance of the shown in Figure 3.4. As observed, the range of achievable

impedance values is limited to a few ohms mostly were the embedded depth (d) is comparable to or lower than gap spacing (w).

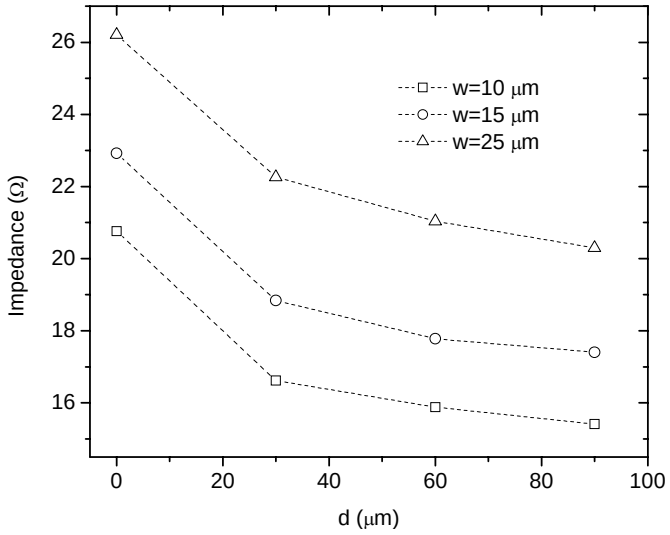

Figure 3.4. Simulated Maxwell 2D lossless impedance corresponding to change in PECPW effective dielectric constant (ε_{eff}) shown in Figure 3.3 with fixed inner-to-inner ground spacing (s+2w) of 500 μm.

3.2.2 Embedded Coplanar Waveguide

The embedded coplanar waveguide (ECPW) design illustrated in Figure 3.5 achieves lower impedance structures than the PECPW. The ground planes are similar to those of the PECPW transmission line however its signal line conductor is also embedded.

The low impedance values of the ECPW results from larger capacitance due to the increase in the effective area and dielectric constant. This is caused by the concentration of the electric fields in the substrate as shown in Figure 3.6. As reflected in the effective dielectric constant values in Figure 3.7, the attainable capacitance of the structure with embed depth (d) is much greater than that of the PECPW in Figure 3.1. The increased concentration of fields in the substrate

increases loss which can be minimized with the use of a low-loss substrate such as high resistivity silicon.

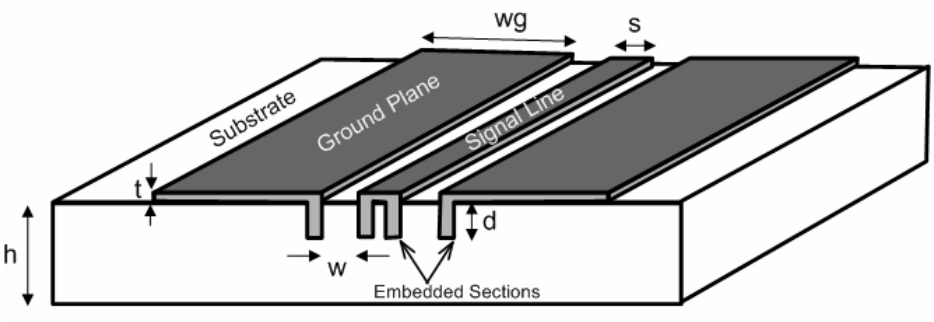

Figure 3.5. Illustration of an embedded coplanar waveguide (ECPW) with vertically embedded ground planes and signal line sections to a depth (d). The substrate height is (h), ground plane width (w_g), signal line width (s), gap spacing (w) and metal thickness (t).

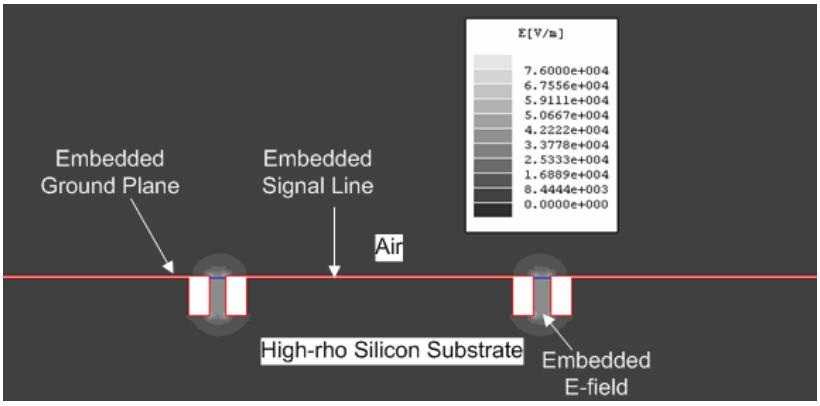

Figure 3.6: Cross sectional view of Maxwell 2D simulated Electric Field plot of a ECPW with inner ground-to-ground spacing (s+2w) of 500μm, d =60μm, s =450 μm and w =25μm. The CPW is simulated on high resistivity silicon substrate with dielectric constant of 11.7.

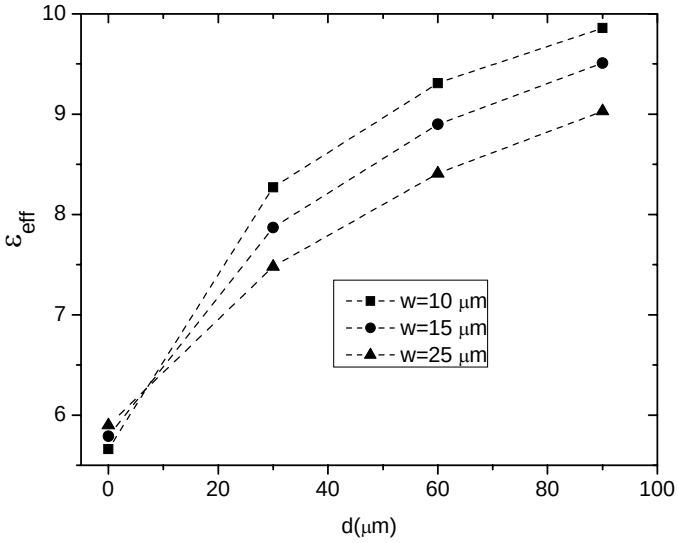

Figure 3.7. Simulated [4] results showing change in effective dielectric constant (ε_{eff}) of ECPW as depth and gap spacing are varied. The structure in this simulation has a fixed inner-to-inner ground spacing of 500 μm.

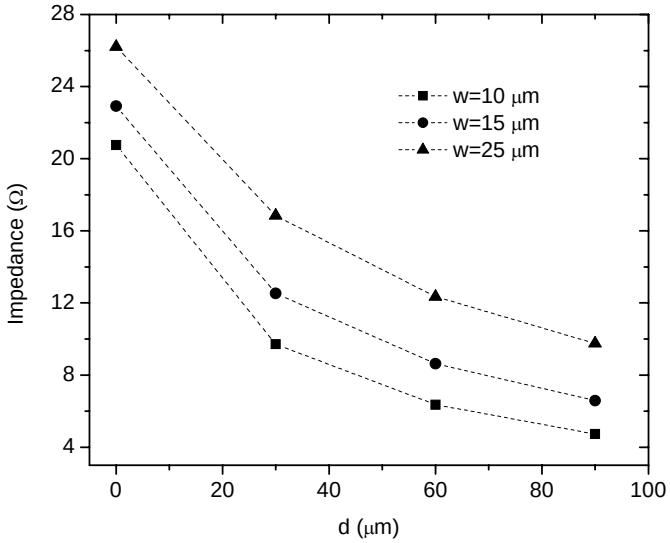

Figure 3.8. Simulated [4] lossless impedance corresponding to change in ECPW effective dielectric constant (ε_e) shown in Figure 3.7 with fixed inner-to-inner ground spacing (s+2w) of 500 μm.

The effect of the gap spacing (w) on the effective dielectric constant is also more pronounced in this design. The increase in the effective dielectric constant and effective area is reflected in the very low impedances that can be realizable

(Figure 3.8). This change in impedance with the embedded depth (d) is also larger than that for the PECPW design.

A low impedance line implemented using the embedded structure approach indicated significant decrease in length compared with a surface CPW (SCPW) such as that in figure 2.5. Assuming the lines are electrically short, the line length required to implement identical capacitance values in both architectures are related approximately by the expression shown in Eq. 3.2.

$$\frac{\theta_E}{\theta_S} = \frac{\beta_E \ell_E}{\beta_S \ell_S} \approx \frac{Z_E}{Z_S} \tag{3.2}$$

Where θ is electrical length, β is propagation constant, ℓ is physical length and Z is characteristic impedance with $_E$ and $_S$ representing the embedded and surface architecture respectively.

The ECPW, with dimension shown in Table 3.1 and impedance and effective dielectric constant value in Table 3.2 is fabricated with a SCPW representing a similar capacitance value. They are fabricated on the same wafer and measured using techniques detailed in section 4.4.

CPW	Length (μm)	w (μm)	s+2w (μm)	d (μm)	t (μm)
Surface	1424	10	500	0	3.2
Embedded	701	15	500	35	3.2

Table 3.1. CPW dimensions of Surface CPW and Embedded CPW used in the distributed implementation of different capacitance values.

CPW	Impedance (Z_L) Ω	Eff. Dielectric Const. (ε_e)
Surface	20.90	5.76
Fully Embedded	11.80	8.20

Table 3.2. Simulated [4] impedance and effective dielectric constant values for surface and embedded CPW structures with dimensions in Table 3.1.

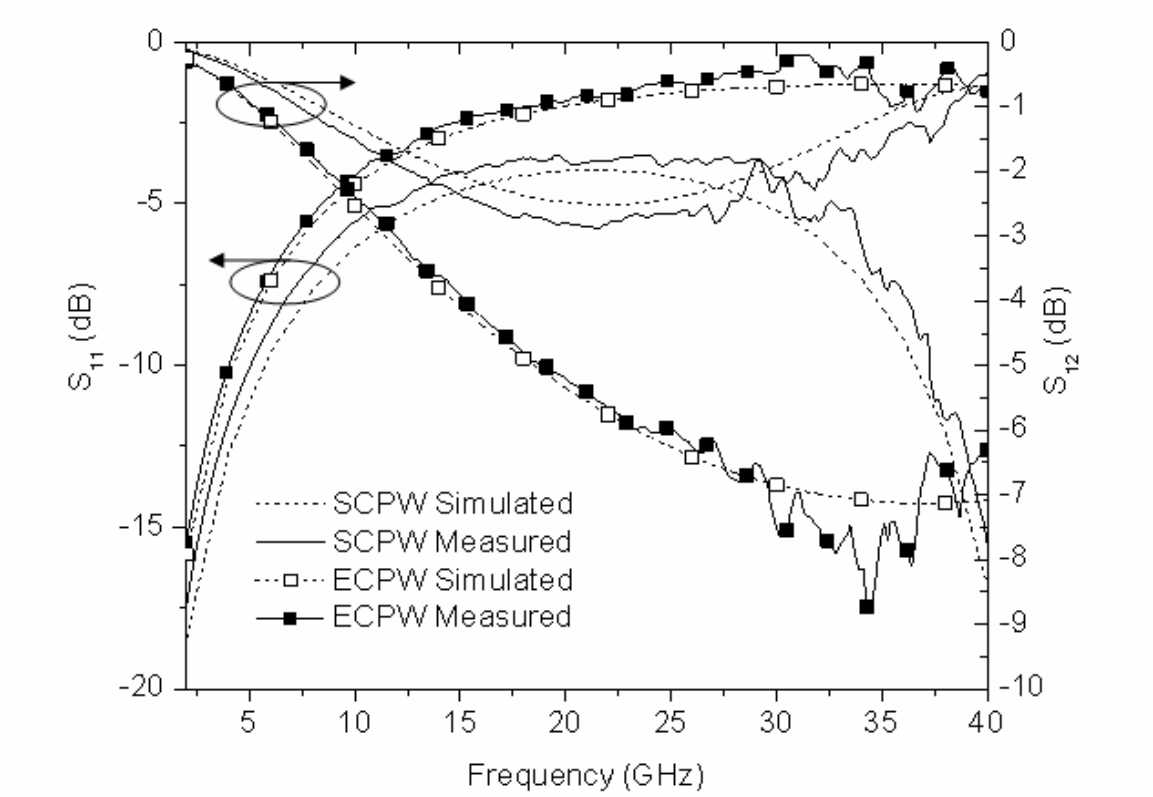

Figure 3.9: Measured and simulated [5] magnitude response for the surface and embedded CPW lines in Table 3.1.

The measured and simulated S_{12} magnitude results for the SCPW and ECPW line in Table 3.1 is shown in Figure 3.9. The measured S_{12} values indicate a difference in line impedance between the two structures. The ECPW line has a larger oscillation or standing wave indicating a greater mismatch with the 50 ohm reference impedance and hence a lower impedance. The low impedance of the

structures is also reflected in the very high S_{11} values. The simulated [5] results accurately predict the behavior of both the SCPW and ECPW below 30 GHz.

3.3 Microstrip Design Methods

The use of high dielectric constant materials is employed in the design of microwave monolithic integrated circuits MMIC. The high dielectric constant value enables the design of reduced size structures. However, low dielectric constants materials are sometimes required to improve the performance of certain structure e.g. antennas. Work done in [6]-[9] uses mixed dielectric approaches and micromachining techniques to obtain low dielectric regions within a high dielectric substrate. The primary focus of the work done by these various authors has being on improving the performance of antenna though it has being used lately in filter design work [10]. In this work, a mixed dielectric substrate material is explored as an approach to three-dimensional design of high frequency or microwave structures.

3.3.1 Bilayer Substrate

Mixed dielectric materials, utilizing a mixture of high dielectric constant substrate and air can significantly lower the effective dielectric constant of structures. It is especially suitable for microstrip structures since its effective capacitance depends on the property of the full substrate thickness. Air is used since it has the lowest loss and dielectric constant value hence resulting in the

lowest possible effective capacitance for the combined substrate. A microstrip structure on a bilayer substrate is illustrated in

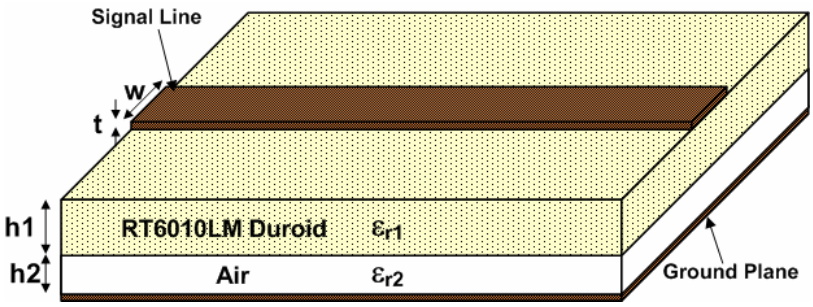

Figure 3.10.

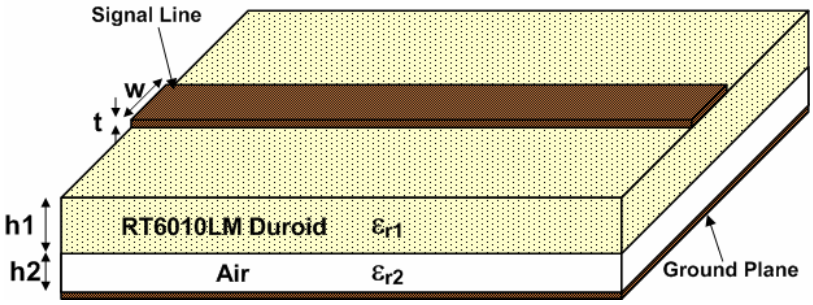

Figure 3.10. Illustration of a microstrip line on a mixed dielectric substrate of duroid and air. The height of the duroid (h_1) and air (h_2) can be varied to obtain various effective dielectric constant values.

The extent to which the dielectric constant is lowered depends on the amount of air present in the combined substrate. Specifically, the height ratio ($h_2/(h_1+h_2)$) of the substrates has a direct correlation with this value. This is illustrated in Figure 3.11 for a duroid (ε_{r1} =10.2) / air (ε_{r2}=1.0) bilayer substrate. The decrease in effective dielectric constant value results in a reduction in the effective capacitance of the microstrip thus an increase in its impedance. Therefore, simply altering the air/dielectric combination can vary the impedance of a microstrip line.

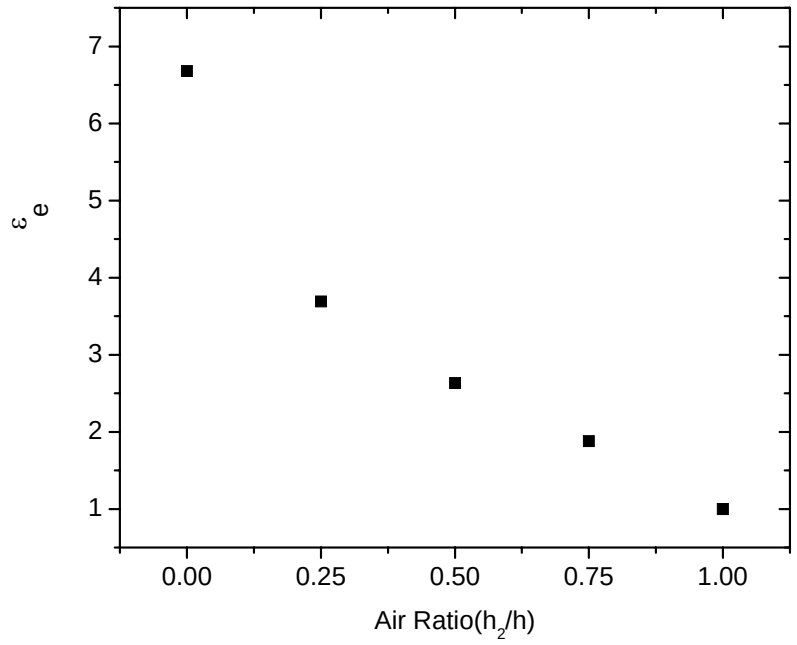

Figure 3.11. Simulated [4] effective dielectric constant variation for a duroid (ε_{r1}) / air (ε_{r2}) bilayer substrate. A microstrip with width equivalent to that of 50 ohms line on full height ($h=h_1+h_2$) duroid was used in simulation.

Figure 3.12 shows the extracted effective dielectric constant value of a fabricated bilayer substrate using a microstrip structure and the method discussed in appendix B3. The structure was fabricated on RT6010LM duroid substrate using a milling machine. The design and fabrication process is detailed in appendix A3. To obtain the effective dielectric constant, the scattering (S) parameters of the structure were measured using a standard microstrip fixture (appendix B1) and measurement setup in appendix B2. A full height duroid microstrip feed attached to both edges of the bilayer substrate was used to launch the test signal into the structure. A microstrip TRL calibration with standards detailed in appendix B.2.1 was performed to shift the reference plane of the fabricated structure to the bilayer region.

The extracted effective dielectric constant for a duroid/air bilayer substrate in Figure 3.12 shows that a 40% air composition can reduce the effective dielectric constant by almost 50%. This change in effective dielectric constant shown in the figure has good agreement with HFSS [5] simulated results.

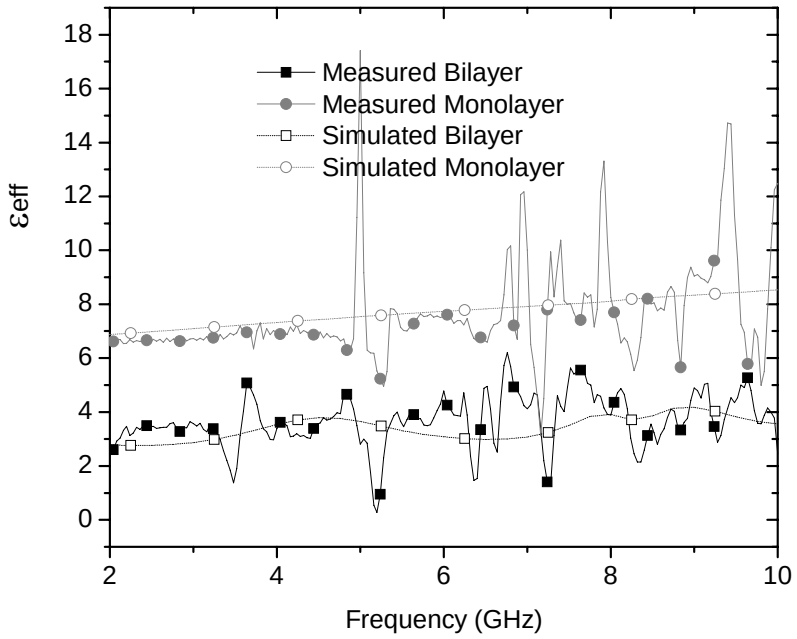

Figure 3.12: Extracted effective dielectric constant from measured and simulated [5] S-parameter phase of 2/3 air/duroid bilayer and duroid monolayer using microstrip line.

The oscillation observed in the simulated bilayer results is due to standing waves generated on the bilayer structures from impedance mismatch between the monolayer feed section (appendix A3) and the bilayer substrate section. The simulated monolayer structure does not have an impedance mismatch hence it is smooth. This result implies that with control of the dielectric composition, the impedance of a microstrip line with a constant conductor width can be varied over a range of values.

3.4 Embedded CPW Filter

3.4.1 Design

To demonstrate the capability of the embedded coplanar waveguide (ECPW) lines for use in compact designs, a 7 section maximally flat filter is designed with a cutoff frequency of 10 GHz and -35 dB stopband attenuation at 20 GHz. A lumped element model for this filter is shown in Figure 3.13 with values shown in Table 3.3.

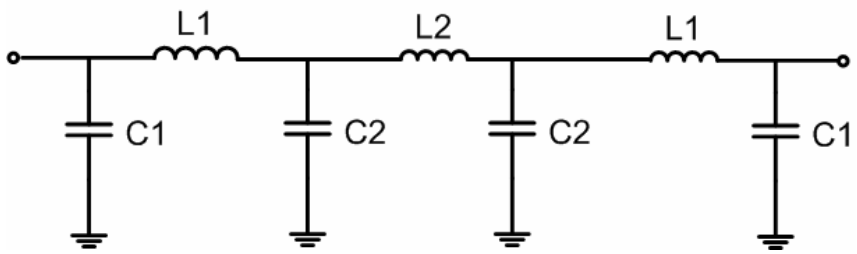

Figure 3.13. Lumped element model of 7 section maximally flat filter.

Component	Value
C1	0.142 pF
L1	0.992 nH
C2	0.574 pF
L2	1.592 nH

Table 3.3. Lumped element values for 7 section maximally flat filter.

N	Component	g_N	$\theta = \beta\ell$ (radians)
1	Capacitor(C1),	0.4450	0.0872
2	Inductor (L2),	1.2470	0.7558
3	Capacitor (C3),	1.8019	0.3532
4	Inductor (L4)	2.0000	1.2121
5	Capacitor (C5)	1.8019	0.3532
6	Inductor (L6)	1.2470	0.7558
7	Capacitor (C7)	0.4450	0.0872

Table 3.4. Normalized values for 7 section maximally flat filter.

The theory behind the design of this type of filter is explained in detail in [11]. The normalized values for the seven section filter are shown in Table 3.4. The electrical length (θ) of each component is obtained from the normalized element values (g_N) of the filter using expressions in Eq. 3.3 and 3.4. They show that shortest possible line length required to implement the inductor is one with the highest impedance whereas for the capacitor is one with the lowest impedance.

$$\left[\beta\ell\right]_{ind.} = \frac{g_{N(ind.)}R_o}{Z_{LINE}} \quad \text{(Inductor)} \tag{3.3}$$

$$\left[\beta\ell\right]_{cap.} = \frac{g_{N(cap.)}Z_{LINE}}{R_o} \quad \text{(Capacitor)} \tag{3.4}$$

where Z_{LINE} is the transmission line impedance and R_o is the reference impedance value.

The low impedance ECPW line with its ability to attain very low impedance is employed in the design of the capacitive lines of the 7 section maximally flat filter. Two design cases are explored using ECPW lines; in the first design referred to as an embedded filter (Figure 4.13) the inductive sections are also implemented using the ECPW making the structure completely embedded. In the second

design case, the inductive sections are designed using the PECPW lines. The filter is thus referred to as a partially embedded filter (Figure 3.15). The dimension of the filter implemented with the two designs is shown in Table 3.5 and Table 3.6 with a SCPW implementation (Figure 3.16) designed as a reference with dimensions shown in Table 3.7. The length of the capacitive line sections for all filters is compensated for open-end effects.

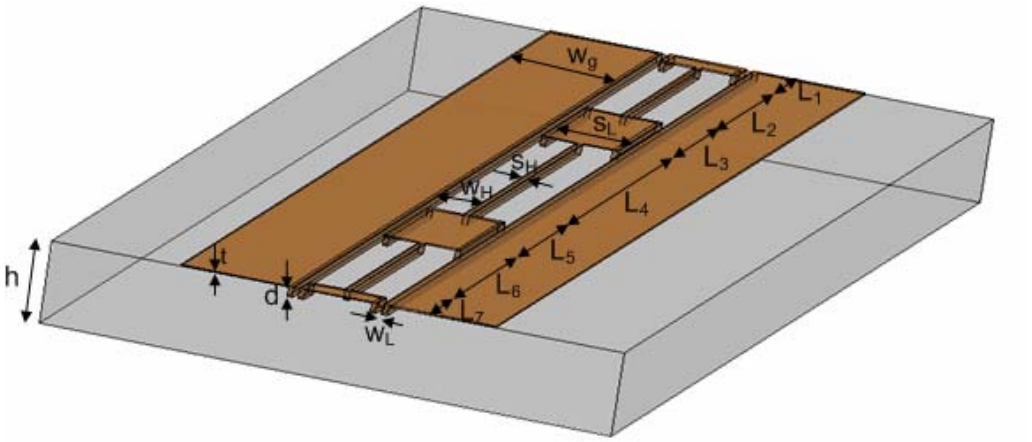

Figure 3.14 Illustration of embedded filter design using inductive and capacitive ECPW lines. The high resistivity silicon substrate has been made transparent and the feed of the structure omitted to highlight the embedded sections of the filter in the substrate. The parameter values of the structure are shown in Table 3.5.

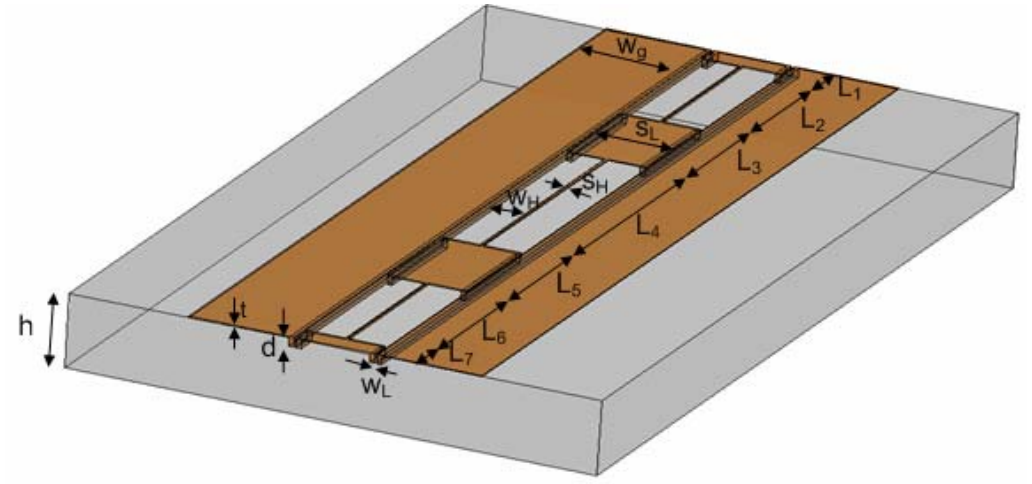

Figure 3.15. Illustration of partially embedded filter designed using embedded capacitive and partially embedded inductive lines. The high resistivity silicon

substrate has been made transparent and the feed of the structure omitted to highlight the embedded sections of the filter in the substrate. The parameter values of the structure are shown in Table 3.6.

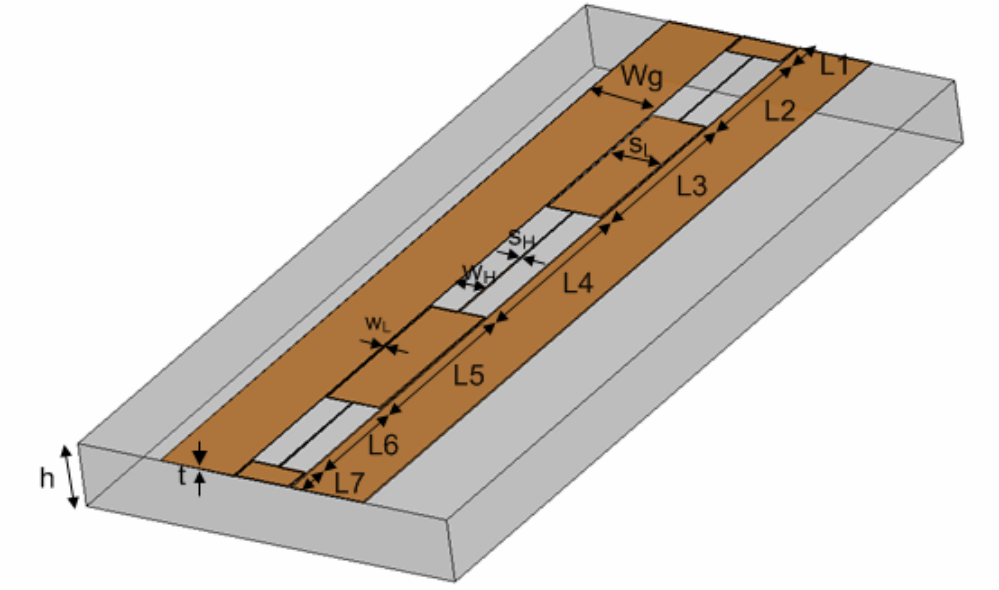

Figure 3.16 Illustration of a surface filter designed using CPW capacitive line and inductive lines. The parameter values of the structure are shown in Table 3.7.

N	CPW Architecture	Length L_N (μm)
1,7	ECPW	141
2,6	ECPW	1300
3,5	ECPW	701
4	ECPW	1900
Total Length (μm)		6384

Table 3.5. Embedded filter section lengths for implementation of maximally flat stepped impedance low pass filter.

N	CPW Architecture	Length L_N (μm)
1,7	ECPW	141
2,6	PECPW	1023
3,5	ECPW	701
4	PECPW	1588
Total Length (μm)		5318

Table 3.6. Partially embedded filter section lengths for implementation of maximally flat stepped impedance low pass filter.

N	CPW Architecture	Length L_N (μm)
1,7	SCPW	229
2,6	SCPW	1007
3,5	SCPW	1424
4	SCPW	1564
Total Length (μm)		6884

Table 3.7. Surface filter section lengths for implementation of maximally flat stepped impedance low pass filter

Filter Design	s_L	s_H	w_L	w_H	w_g	D
Surface	480	10	10	245	630	-
Partially Embedded	470	10	15	235	630	35
Fully Embedded	470	30	15	235	630	35

Table 3.8: Dimensions (μm) of different CPW line architecture used in design of filters.

	Capacitive Line		Inductive Line	
Filter	Impedance (Z_L) Ω	Eff. Dielectric Const. (Ee_L)	Impedance (Z_H) Ω	Eff. Dielectric Const. (Ee_H)
Surface	20.90	5.69	119.30	5.87
Partially Embedded	11.80	8.20	116.80	5.92
Fully Embedded	11.80	8.20	72.30	6.93

Table 3.9: Simulated [4] results of different CPW line architecture used in the design of filters.

The surface and the embedded filter have comparable high to low impedance ratios (Z_H/Z_L) while the partially embedded filter has a ratio approximately 1.6

times greater as shown in Table 3.9. The feed design for the surface filter is shown in Figure 3.17 with dimensions in table Table 3.11.

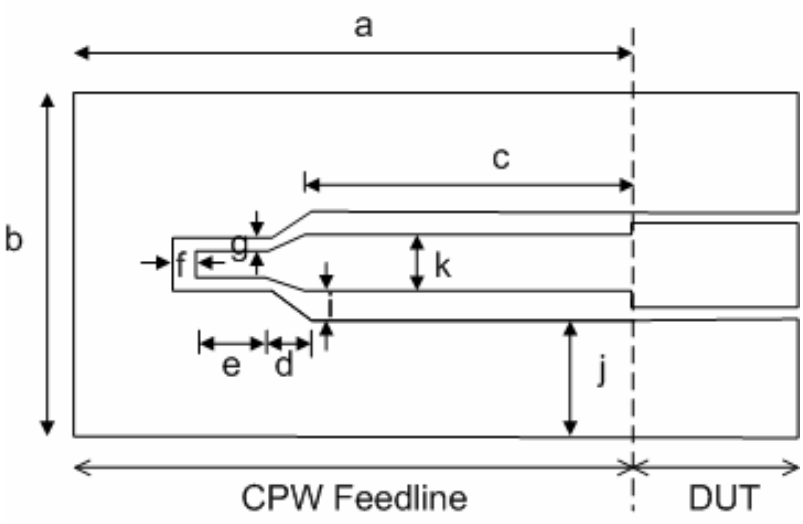

Figure 3.17. 50 ohm surface feed line used to feed surface filter feed design.

Parameters	Surface Feed
a	1705
b	1760
c	500
d	50
e	250
f	150
g	75
i	132
j	630
k	236

Table 3.10. Parameter values in (μm) for surface feedline shown in Figure 3.17 used to feed surface filter.

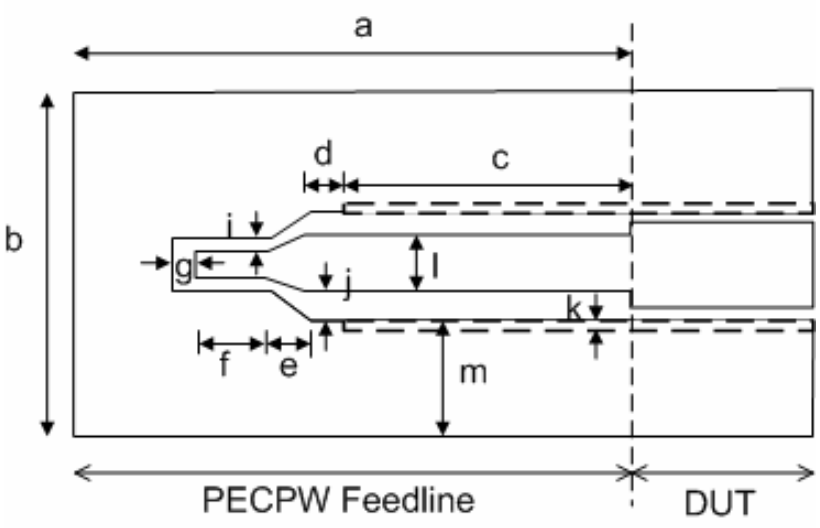

Figure 3.18. 50 ohm partially embedded (PECPW) feed line used to feed embedded and partially embedded filter feed design. Embedded section shown with dotted lines.

Parameters	Partially Embedded Feed
a	1705
b	1760
c	400
d	100
e	50
f	250
g	150
i	75
j	145
k	30
l	210
m	630

Table 3.11. Parameter values in (μm) for partially embedded feedlines in Figure 3.18 used to feed partially embedded and embedded filters.

The embedded section of the ground plane of the feedline is similar to of the embedded CPW line allowing it to be continuous throughout the length of the structure.

3.4.2 Realization of Embedded CPW Line and Filter

3.4.2.1 Microfabrication Approach

The fabrication process of the embedded, partially embedded and surface filters in section 4.4.1 and the CPW lines in section 4.2.2 is discussed in this section. Most of the process utilizes established microfabrication techniques detailed in [12]. A single process designed to utilize the minimum number of masks is used to fabricate the three filter designs and CPW lines. It consists of two sequential parts: (1) the embedded sections and (2) the surface structure.

The fabrication process flow is shown in Figure 3.19. Deep reactive ion etching (DRIE) is used to etch vertical trenches with minimum sidewall sloping following a transfer of the embedded circuit pattern to the wafer through a photolithographic process. A conformal electroplating process similar to that in [13] is then used to completely fill the trenches with copper and chemical mechanically polished (CMP) to smoothing surface. This is the most critical step of the fabrication process. The process parameters have to be adjusted to prevent the formation of voids in the center of the embedded sections. The parameters used for this process are detailed in appendix A. The SEM picture in Figure 3.20 shows the top view of the embedded section of a filter at the completion of the CMP process. Standard surface electroplating is used to create

the surface structure above the embedded structure followed by a back etching process to remove the seed layer.

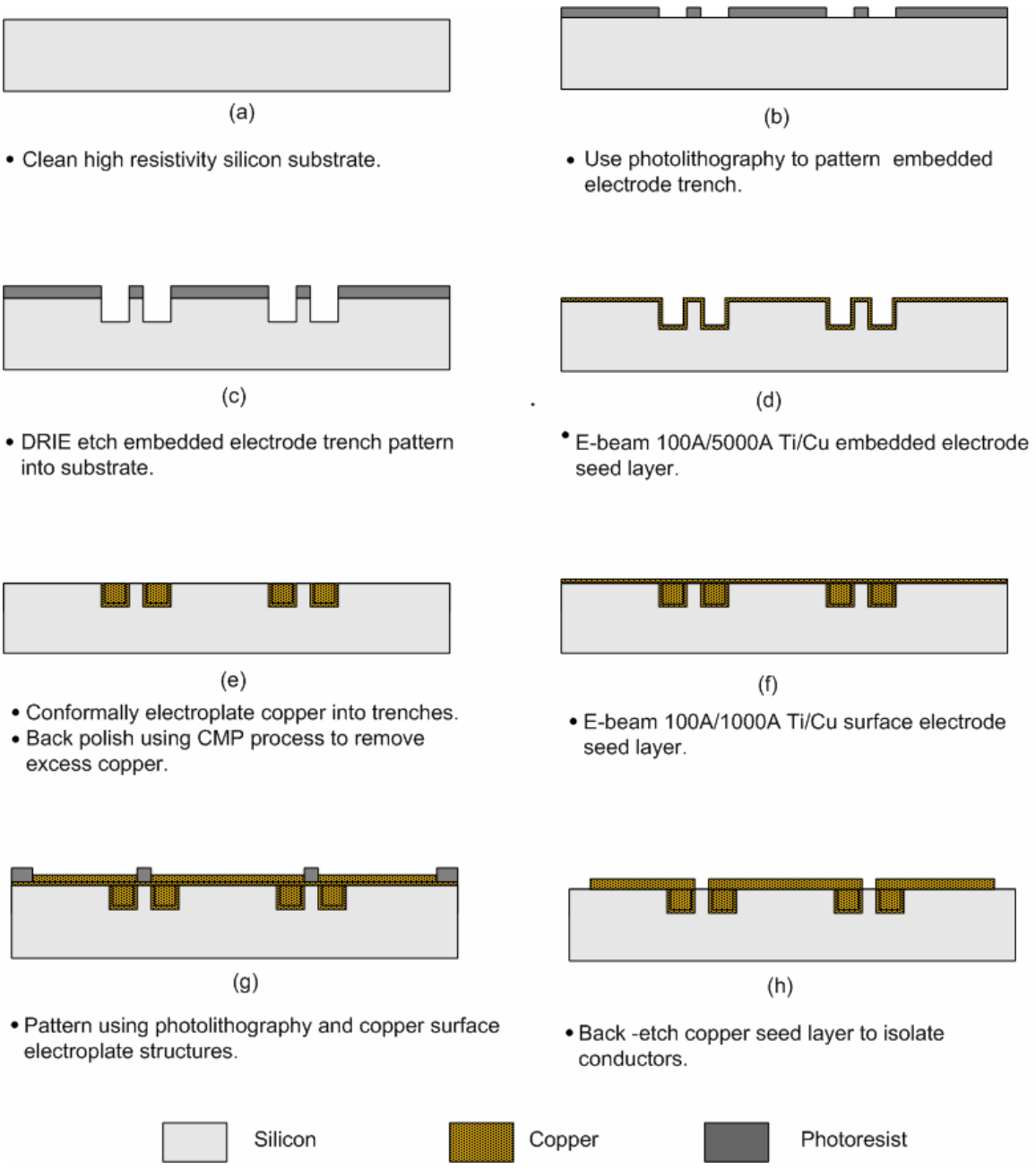

Figure 3.19: Fabrication process flow for embedded filter showing the major steps in the process.

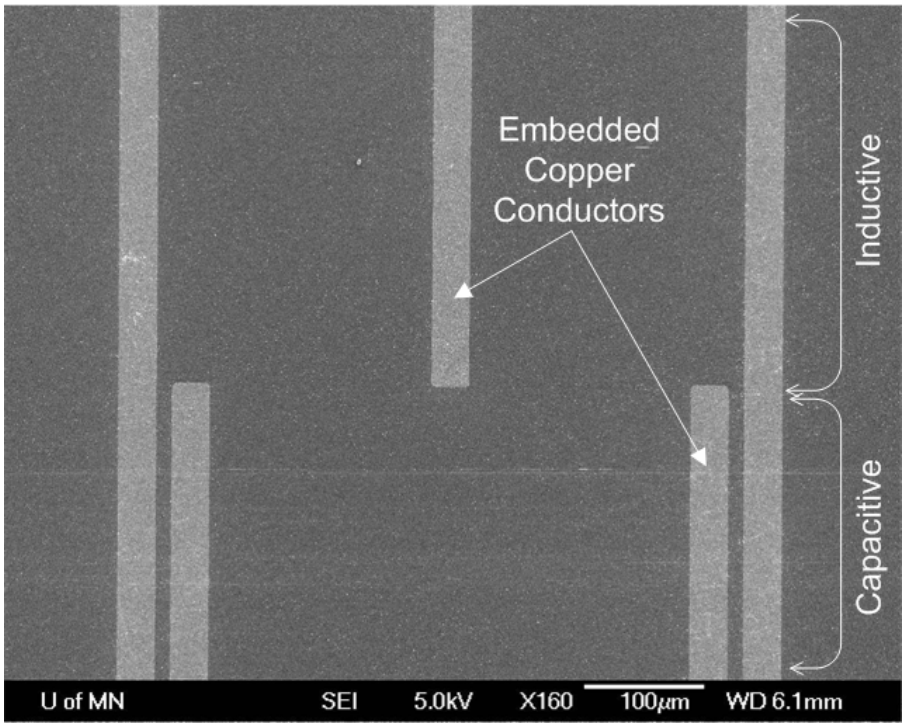

Figure 3.20. SEM picture of the embedded section of an embedded filter after Chemical mechanical polishing showing both inductive and capacitive sections.

3.4.2.2 Substrate Preparation

A single-side polished high-resistivty (> 2000 ohm-cm) silicon substrate is used for the filters and CPW structures. The bare wafer is cleaned to remove organic contaminants and native oxide build-up that accumulate on the substrate. The wafer thickness needs to be relatively constant across the wafer as this greatly affects the result of the chemical mechanical polishing process (CMP). Variation of a few microns (+/- 5μm) is usually acceptable.

3.4.2.3 Deep Reactive Ion Etching

This process uses ion bombardment to etch vertical trenches in the silicon substrate materials. The process is non-selective; therefore it etches the

substrate as well as any materials on it. To protect the surface of the wafer requires a thick masking layer that can endure constant bombardment for the required etch duration. In order to maintain a vertical profile, the sidewalls of the etched trenches are constantly coated during the etching process to prevent stray ions from etching them out. This is necessary to maintain the uniformity of the final gap spacing of the CPW capacitance of the embedded and partially embedded filters.

3.4.2.4 Conformal Copper Electroplating

This process is designed to enable the complete filling of the etched trenches in the substrate using electroplating as shown in Figure 3.19. The process utilized a forward and reverse current pulse cycle. Copper is deposited on the wafer during the forward pulse cycle and etched during the reverse pulse cycle. Each forward cycle deposits more copper than is removed in the reverse cycle resulting in a net accumulation of copper in the trench. The duration of each of the forward and reverse pulse as well as the current values are critical parameters for a void free process. The voids are usually generated when the accumulation copper at the entrance is not etched at a sufficient speed by the reverse pulse. The built up limits the circulation of electroplating solution in the trench and finally closes the entrance of the trench. When the appropriate parameters are used the trench is completely filled as shown in the SEM in Figure 3.21.

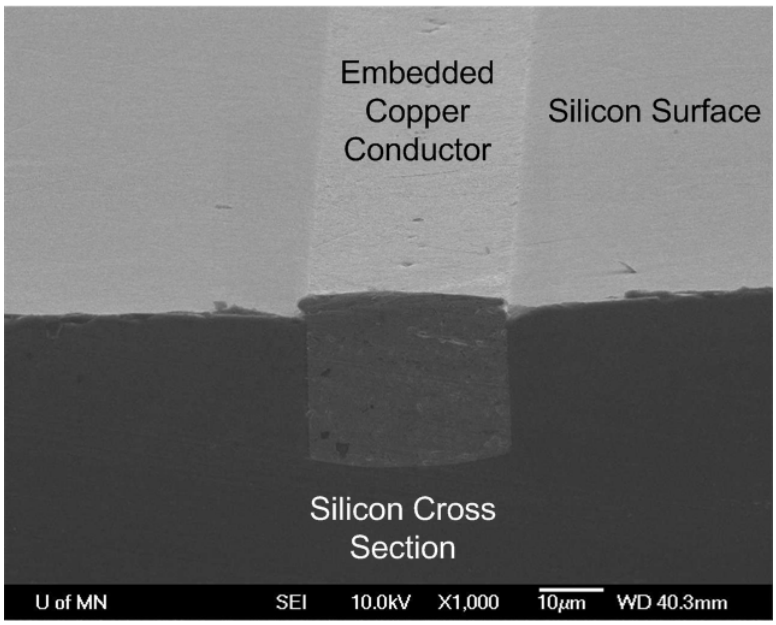

Figure 3.21. SEM of completely filled copper embedded section in high resistivity silicon substrate. Trench was filled using conformal electroplating process.

3.4.3 Characterization, Result and Analysis

3.4.3.1 Characterization Approach

An on-wafer testing approach using a network analyzer and probe station (shown in Appendix B.1.2) is used to measure the S parameters of the fabricated structures. Through-Reflect-Line (TRL) calibration standards fabricated on the substrate and detailed in appendix B are used to calibrate the analyzer using the NIST algorithm. The calibration shifts the measurement reference plane eliminating the feed lines of the structures from the measured result. The substrate is isolated from the grounded chuck of the probe station using an air

spacer to prevent the excitation of grounded coplanar waveguide modes on the feedlines of the structure.

3.4.3.2 Result and Analysis

The measured results of the fabricated surface, partially embedded and embedded CPW filter are shown in Figure 3.22.

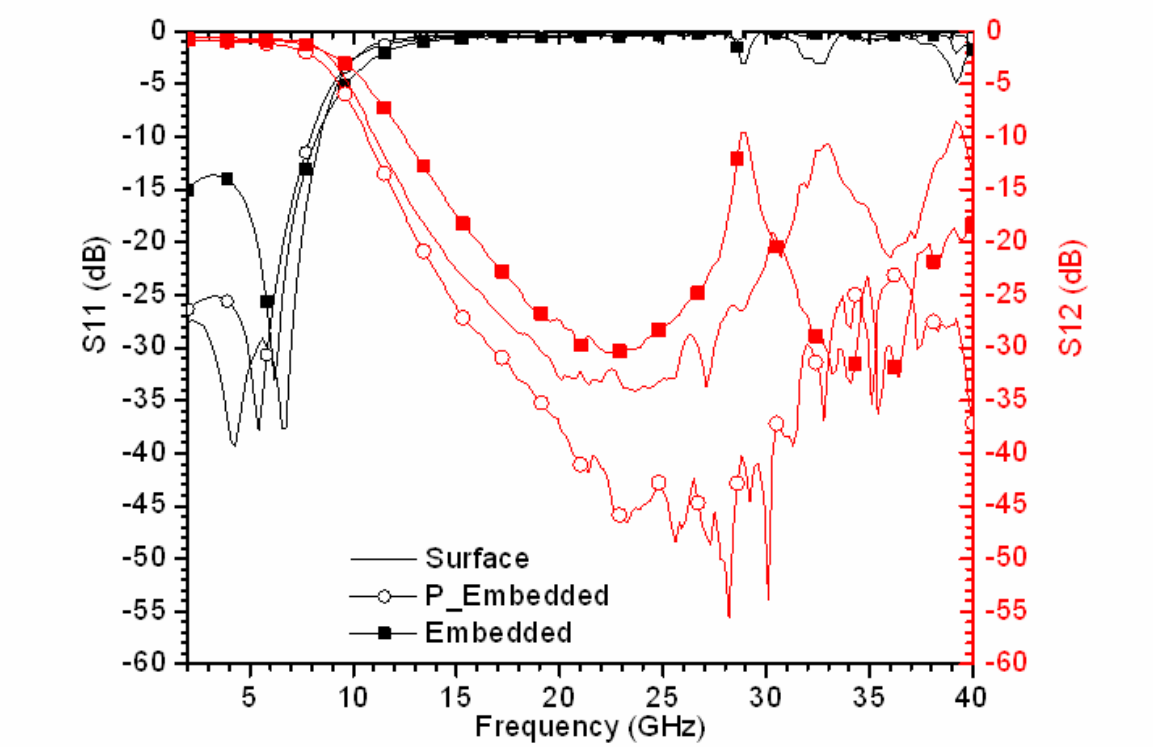

Figure 3.22: Measured S-parameter results of a stepped impedance filter implemented in three different CPW architectures, surface, partially embedded and embedded.

The results show that the performance of the filter is dependent on the implemented CPW architecture. Simulated [5] results show good agreement with measured filter responses for the different filters as shown in Figure 3.25 to Figure 3.23. This shows that HFSS [5] can be used to accurately predict the behavior of devices designed.

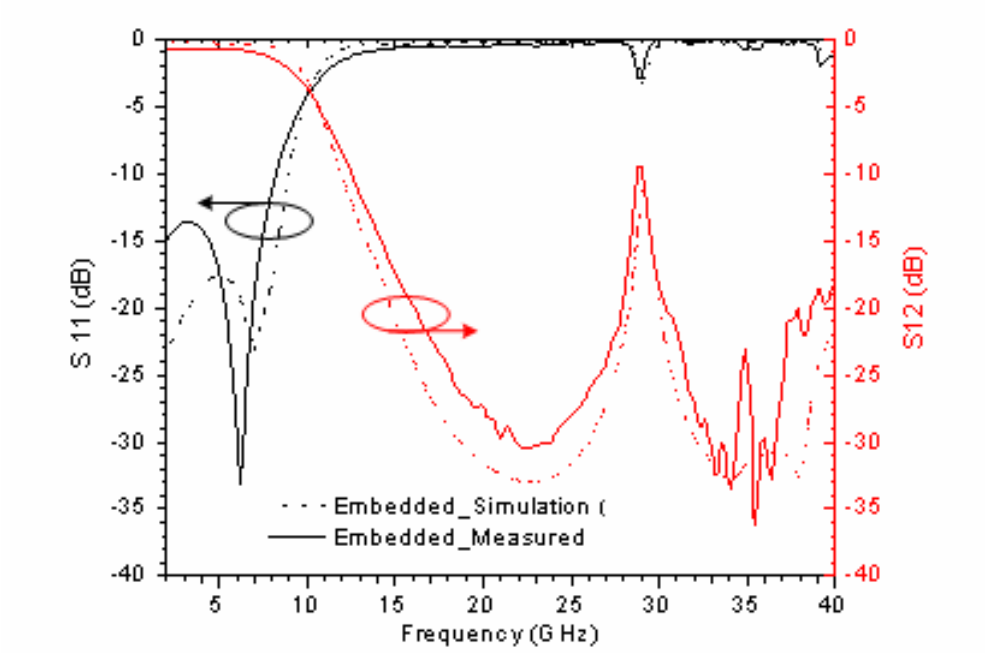

Figure 3.23: Measured and simulated [5] result of embedded filter. This filter has ECPW inductive and capacitive lines with an impedance ration similar to the surface structure with results shown above.

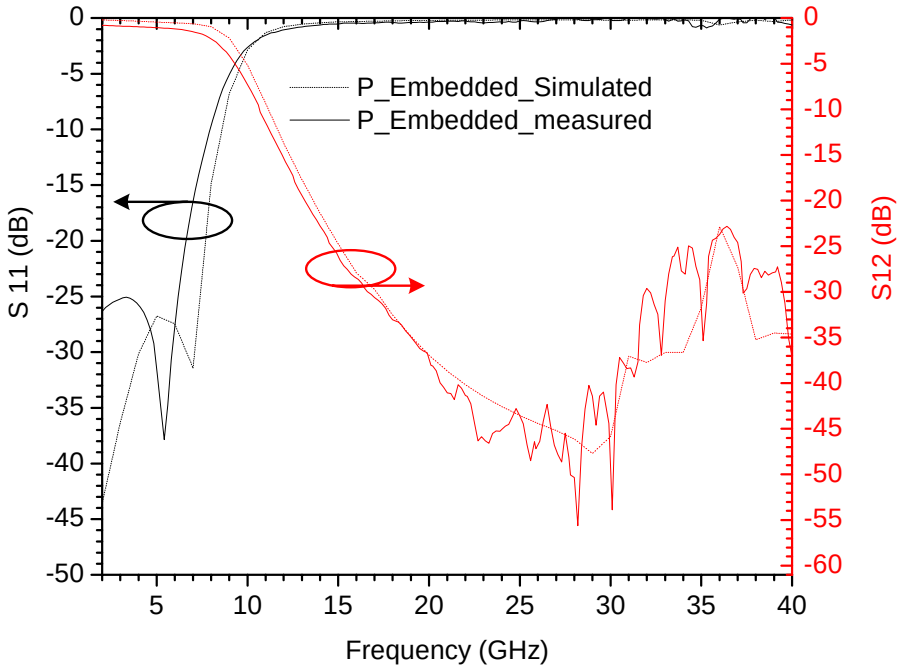

Figure 3.24: Measured and simulated [5] results of partially embedded filter. The filter has a low to high impedance ratio similar to that of the fully embedded structure.

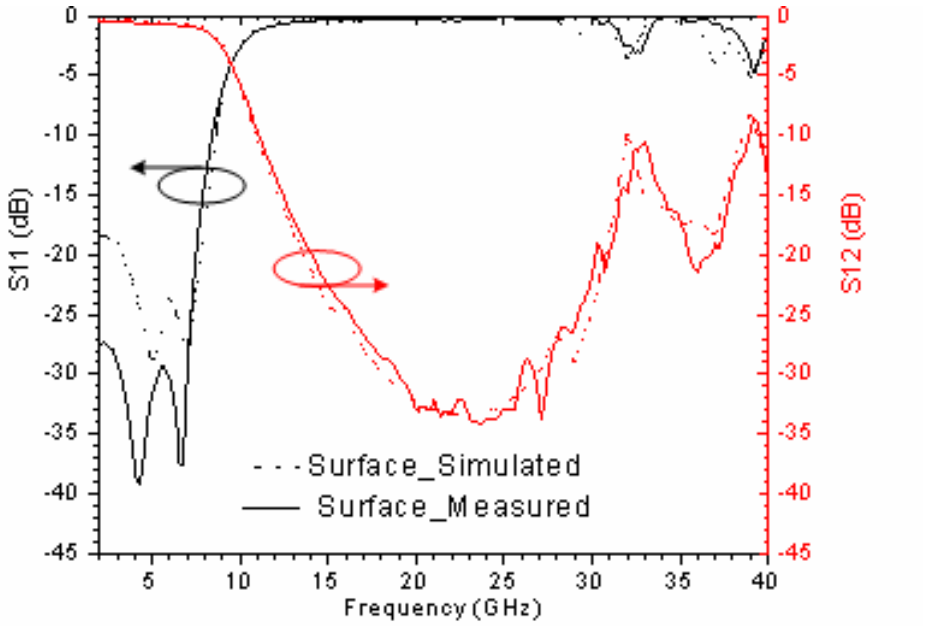

Figure 3.25: Measured and simulated [5] results of surface filter. The filter has a low to high impedance ratio similar to that of the fully embedded structure.

The partially embedded filter has the best stopband performance; lower than the surface and embedded filter architectures. It has a passband attenuation that is comparable to that of the surface and embedded filters. Since this structure has less parasitics than both the surface and embedded filters, the parasitic pole is lower than that of the surface and the embedded that have similar poles. The high level of the poles in the embedded and surface filters can be associated with the excess parasitic capacitance in the inductive section of the embedded filter and the excess inductance in the capacitive section of the surface filter. Another improvement in the partially embedded structure over the surface and embedded is the 23 % reduction in length. While the embedded inductor does not offer any improvement in stopband performance it offers an 8% reduction in length. The results show that use of embedded low impedance line in the design of the

partially embedded filter not only improves performance by minimizing parasitics but also reduces the physical length of the filter.

3.5 Bilayer Microstrip Filter

3.5.1 Design

The use of machined materials in the design of microstrip based filters with improved performance has recently being explored by several authors [15]-[18]. Several of these designs have being developed using the method of forbidden band and referred to as photonic band gap structures. Some of the structures have also being implemented using other transmission structures such as microstrip [15], [16] and CPW [17]. The architecture of the structures in CPW for example is quite simple with repetitive inductive and capacitive impedance elements. Such a structure makes a good candidate for a bilayer substrate microstrip filter design in which the impedance a standard microstrip could be varied by inserting isolated bilayer substrate region along the microstrip. In this mixed dielectric filter approach, air slots are introduced into local regions of the substrate to create high impedance regions in the structure while maintaining the profile of the signal line on the surface as shown in Figure 3.26.

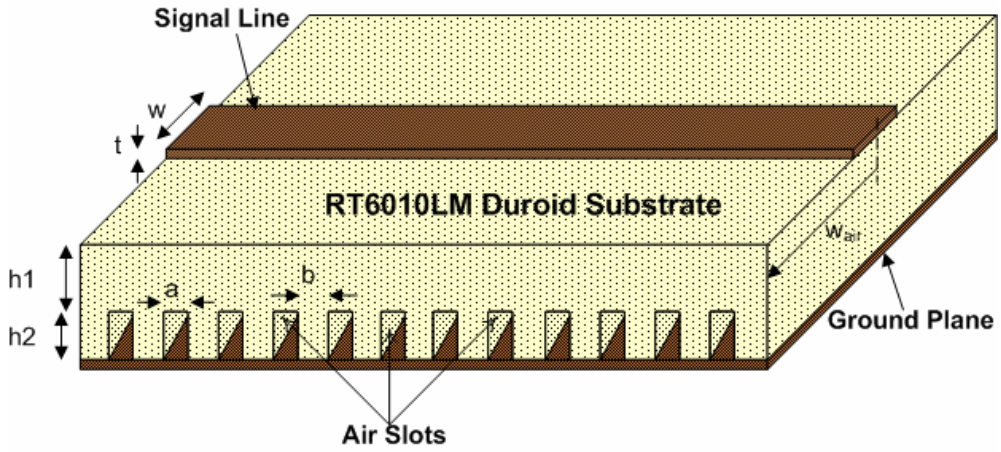

Figure 3.26. Schematic of a microstrip mixed dielectric photonic bandgap filter simulated in HFSS.

3.5.2 Simulation and Analysis

Analysis of the structure in Figure 3.26 with 12 air slots is performed using Ansoft HFSS [5] to evaluate the feasibility of the structure. Duroid substrate (RT6010LM) with dielectric constant of 10.2 is used in the design. The effect of the mixed dielectric composition on the performance of the structure is explored by varying the height ratio (h_2/h_1) of the two substrates. The dimension of two variations of the 12 slot design simulated is shown in Table 3.12.

Parameters	Variation 1 Dimension (mils)	Variation 2 Dimension (mils)
w	22	22
t	1.4	1.4
a	100	100
B	100	100
h_2 (air)	12.5	22.5
h_1 (duroid)	12.5	2.5
w_{air}	800	800
Total Length	2500	2500

Table 3.12. Dimension of simulated [5] 12 slot mixed dielectric substrate filter structure designs with different bilayer dielectric height (h_1/h_2) ratio.

Simulations were also performed for a 6 slot design with similar dimensions and h_2/h_1 variations shown in Table 3.13. The width (w) of the signal line in both cases is such that the section of the structure on full height duroid has a 50 Ω characteristic impedance.

Parameters	Variation 1 Dimension (mils)	Variation 2 Dimension (mils)
w	22	22
T	1.4	1.4
a	100	100
b	100	100
h_2 (air)	12.5	22.5
h_1 (duroid)	12.5	2.5
w_{air}	800	800
Total Length	1300	1300

Table 3.13. Dimension of simulated [5] 6 slot mixed dielectric substrate filter structure designs with different bilayer dielectric height (h_1/h_2) ratio.

It is observed that a low pass filtering response can be obtained with classical photonic bandgap structure repeatability. The stopband in Figure 3.27 and Figure 3.29 demonstrate a symmetric characteristic. For a given design, doubling the number of periodic sections causes significant improvement in the stopband response, nearly doubling the isolation. For designs based on different air / duroid (h_2/h_1) ratios, the bandwidth is increased by increasing the air composition of the bilayer regions. The return loss shown in Figure 3.28 and Figure 3.30 is less symmetric as the air / duroid ratio of the bilayer substrate is increased.

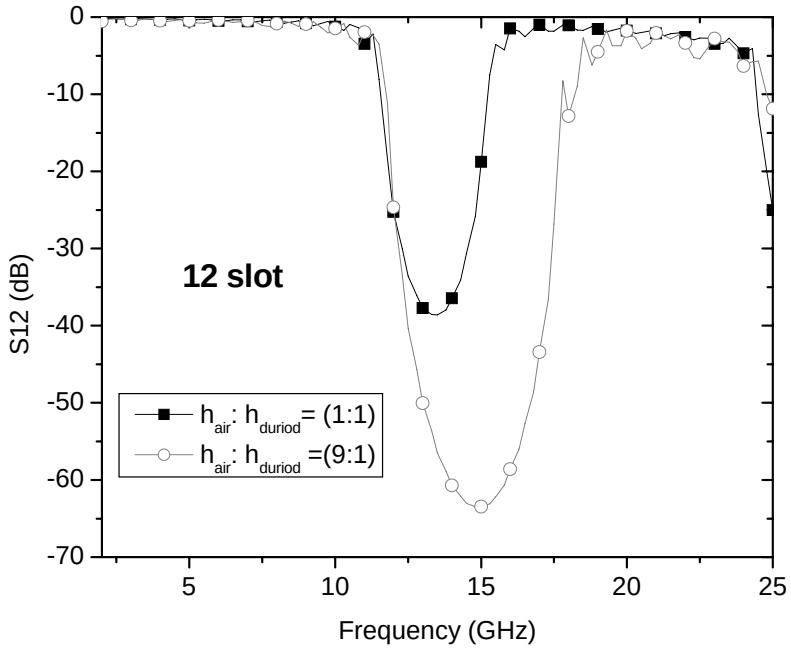

Figure 3.27. Simulated [5] insertion loss response for a 12 slot photonic band gap filter structure design in a microstrip architecture using mixed dielectric substrate.

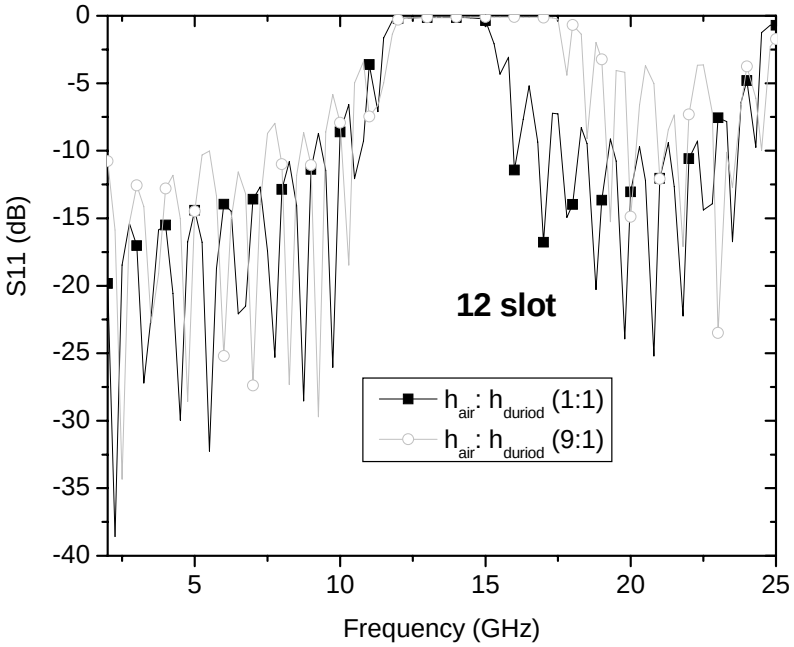

Figure 3.28. Simulated [5] return loss response for a 12 slot photonic band gap filter structure design in a microstrip architecture using mixed dielectric substrate.

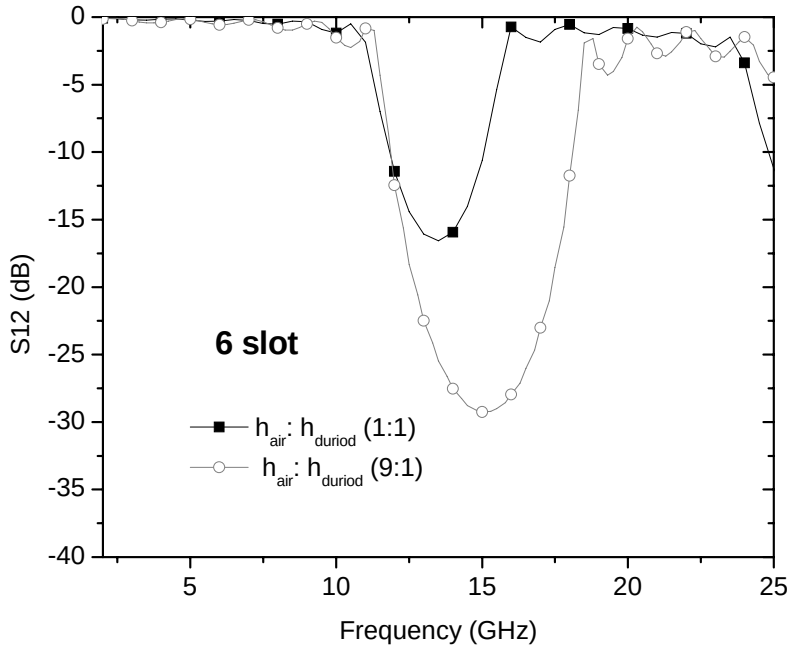

Figure 3.29. Simulated [5] insertion loss response for a 6 slot photonic band gap filter structure design in a microstrip architecture using mixed dielectric substrate.

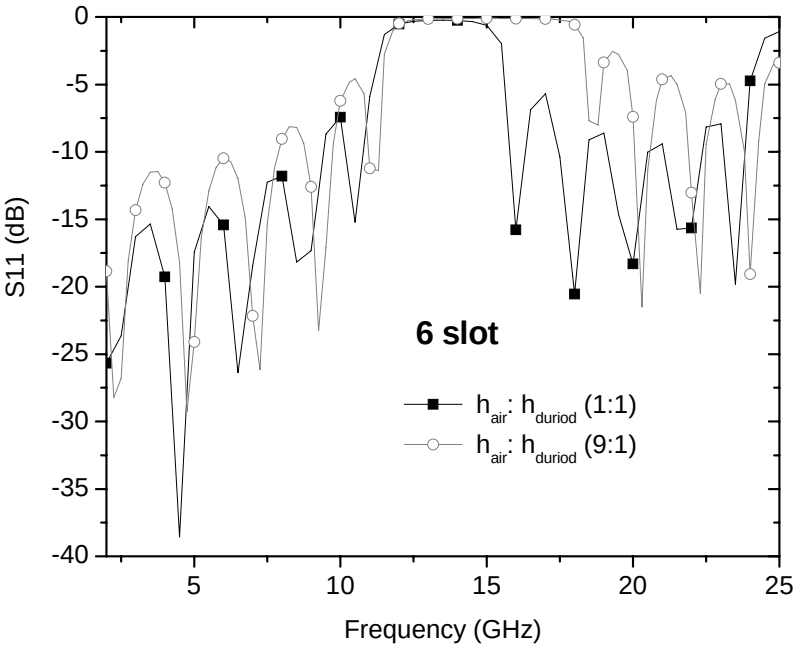

Figure 3.30. Simulated [5] return loss response for a 6 slot photonic band gap filter structure design in a microstrip architecture using mixed dielectric substrate.

3.6 Summary

A novel embedded coplanar waveguide has been introduced. Work with the embedded CPW shows it to be more efficient in the implementation of capacitive lines but not as effective for inductive line design. Therefore hybrid designs using surface inductive section produce the best results. Its capability for compact designs is also demonstrated with a maximally flat filter producing a 23% reduction in filter length for the hybrid design and 8% for an embedded design compared to a surface filter. The use of embedded low impedance lines in the hybrid filter design also improved the stopband characteristic by 10dB compared to a surface filter. This novel approach can be a useful approach in the development of multi-layer circuits for MMIC applications.

The use of mixed dielectric material to lower the effective dielectric constant of a material thus altering the impedance of transmission line structures on the substrate is investigated using duroid / air substrate. Simulation results show that this can effectively be used in the design of structures such as a filter by merely altering the substrate underneath the transmission line.

Chapter 3 References

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Chapter 4: Test Methods for Embedded Designs in Low Resistivity Substrates

4.1 Introduction

Appropriate test methods and results are important in evaluating the performance of fabricated Radio Frequency (RF) devices. Physical structures such as cables and connectors are used to connect the device to the measurement or testing system. In order to solely characterize the device, calibration is done to eliminate or minimize the effects of connection and/or interface as well as the measurement system.

Several well establish calibration methods exist in the evaluation of RF devices. These calibration methods include Through-Reflect-Line (TRL) [1]-[4], Load-Reflect-Match (LRM) [5], [6] and Short-Open-Load-Through (SOLT) [5], [7]. These methods use known device standards as references to compensate the measurement system for parasitics. The TRL calibration method is the most accurate of the three but is however impractical at low frequencies due to the length of the standards required. The LRM and SOLT standards perform well across the band but are less capable of eliminating parasitics such as interface parasitics. The illustration in Figure 4.1 shows the measurement reference plane using a generic device under test (DUT) for the different calibration methods. The TRL calibration shifts the measurement reference plane past the DUT feed providing a more accurate measured response of the DUT.

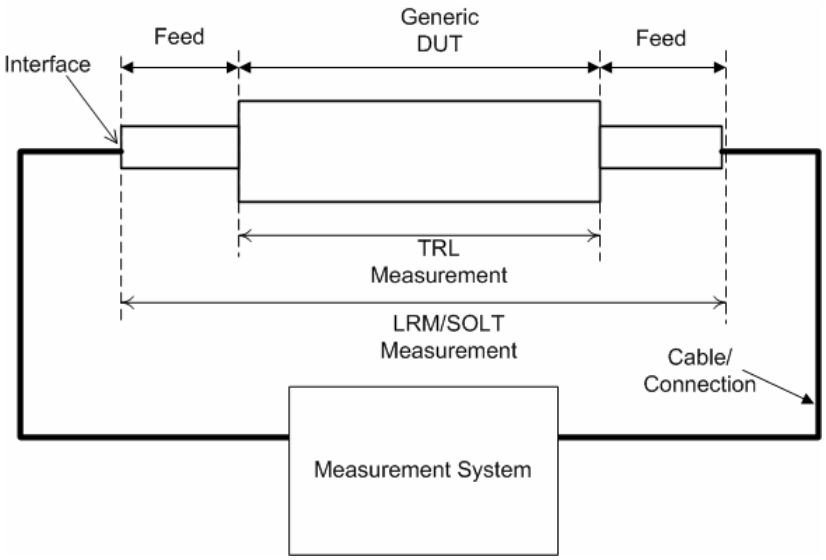

Figure 4.1. Illustration of the reference planes of LRM/SOLT and TRL calibration.

When characterization of integrated devices such as those in semiconductor material is required, the effects of additional interface parasitics such as test pads can overwhelm the measured device response. If the devices to be characterized are surface devices on high resistivity substrate and operate at relatively high frequencies, the TRL calibration can be used to eliminate contact parasitic effects. When these devices are on lossy substrates and operate at lower frequencies, broadband methods such as TRL and SOLT have to be used. In the case of embedded devices, an appropriate interface that enable proper connection with the device also has to be utilized. This work explores the characterization of low frequency embedded devices using standard measurement equipment and modified interface approaches to accomplish this task. The DUT characterized in this work is this work is detailed in section 4.3.

4.2 Properties of Low Resistivity Substrates

4.2.1 Slow-wave propagation in MIS Structures

Transmission line interconnect structures fabricated with a metal-insulator-semiconductor (MIS) architecture as illustrated in Figure 4.2 can support multiple modes of wave propagation; a skin effect mode, dielectric Quasi-TEM (DQTEM) mode and slow-wave mode [10]. The mode of propagation depends on the semiconductor resistivity, insulator thickness, circuit dimension and frequency of operation.

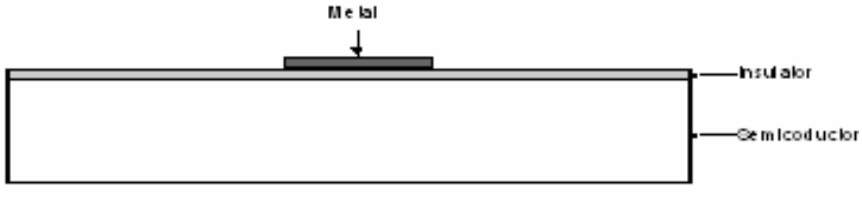

Figure 4.2. Illustration of a (metal-insulator-semiconductor) MIS structure architecture.

The skin effect mode occurs when the skin depth becomes much smaller than the thickness of the semiconductor substrate. This usually happens at high frequencies and low substrate resistivity. The DQTEM mode, the desired mode of operation for most transmission lines, usually occurs when the operating frequency and substrate resistivity are relatively high. In this mode, the electric and magnetic fields are evenly distributed. At low frequencies and low substrate resistivity values, a greater portion of the electric field becomes confined to the insulator layer as illustrated in while the magnetic field distribution remains constant giving rise to a slow-wave mode. The excitation of the slow-wave mode

results in a reduction in the velocity of the propagating signal and greater attenuation due to substrate resistance.

4.2.2 Loss Properties of Low Resistivity Silicon Substrate

The effect of substrate resistivity on transmission lines fabricated on silicon substrates compared with other substrates such as GaAs was discussed in chapter 2.4. Low-resistivity or CMOS silicon with its high conductivity is ideal for fabricating active circuits such as transistor; however, electric and inductive coupling to it creates excessive loss in passives structures [15]. In a passive structures such as an inductor fabricated on high resistivity silicon for example, only substrate loss due to electric coupling is present. On low resistivity or CMOS silicon however, the magnetic field of the structure generates a force on the free ions in the substrate creating an additional resistance and avenue for loss.

4.3 Case Study: Embedded Inductor

The embedded DUT (E-DUT) used in this work is a three dimensional inductor with similar architecture and fabrication process to that in [8] and [9] but differ in its details. This structure is a 15-turn square inductor with an outer dimension of 3mm×3mm and total length of 13.6 cm. It is completely buried in low resistivity silicon substrate (1-10 ohm-cm) as illustrated in Figure 4.3.

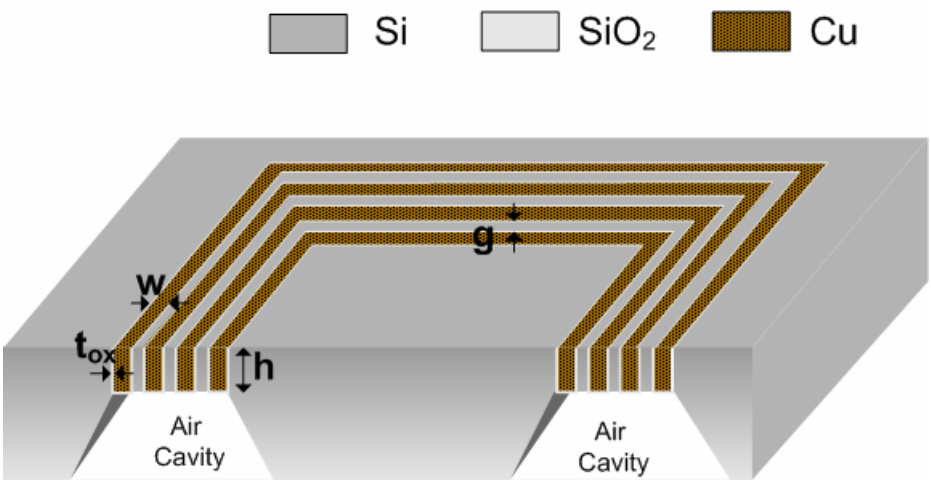

Figure 4.3. Schematic view if three dimensional embedded inductor with air cavity etched underneath copper conductors.

The copper conductors of the inductor are isolated from the conductive silicon substrate by a layer of silicon dioxide with thickness (t_{ox}) of ~ 2.5 μm. The conductors have a cross-sectional area of 30μm (w) × 50μm (h) with a layer of silicon between two oxide layers separating adjacent inductor turns as shown in the SEM in Figure 4.4.

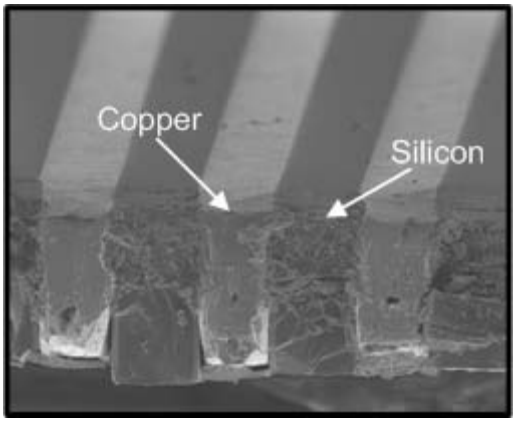

Figure 4.4. SEM picture of cross-sectional view of embedded inductor

The bulk silicon underneath the conductors is selectively etched to reduce parasitic capacitances, thereby increasing the self-resonance frequency of the structure. This also minimizes the magnetic coupling loss due to the substrate of the structure.

A combination of finite element method (FEM) quasi-static analysis and equivalent lumped element circuit modeling is used to simulate the structure. The self-inductance and resistance of each turn as well as the mutual inductance between turns is determined using an electromagnetic field simulator [10]. Although the self and mutual inductance can be determined using methods such as that by Greenhouse [11], the resistance has to be extracted from field simulations results to account for eddy current effects. The loss due to eddy currents in manifested in the form of skin and proximity effect depending on the geometry and frequency of operation of the structure. Skin effect causes current to flow mostly on the surface of the conductor while proximity effect causes current to flow mostly on a single side of the conductor (inner side of the inner turns and outer side of the outer turn). A three-dimensional (3D) simulation of the structure requires a simulation mesh of millions of tetrahedral to account for skin and proximity effects, therefore a two-dimensional (2D) approach is employed. A 360^{O} sweep of the 2D cross-section of the structure is simulated with a refined mesh. Since the inductor is not exactly axisymmetric, concentric cylindrical ring are used to represent the inductor turns in the simulation. The rings have the same width (w) as the inductor coils and separated by the gap spacing (g) of the inductor.

The lumped element model for a few turns of the inductor is shown in Figure 4.5.

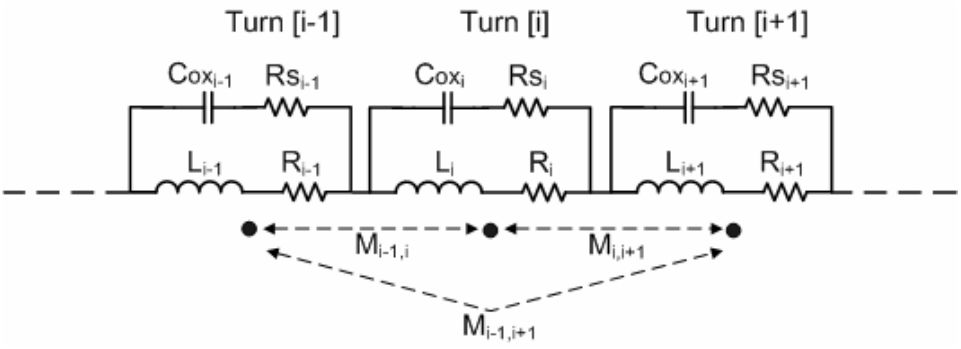

Figure 4.5. Lumped element model for 3D embedded inductor illustrated in Figure 4.3.

Cox_i is the oxide capacitance between two consecutive inductor turns while Rs_i is the resistance of the silicon between the oxide layers separating two consecutive inductor turns. L_i and R_i are the self inductance and resistance of individual inductor turns and $M_{i,j}$ is the mutual inductance between two inductor turns. Cox_i and Rs_i are calculated from geometrical parameters while L_i, R_i and $M_{i,j}$ are determined using electromagnetic simulation [10]. The results are then used to solve the equivalent circuit model equation with [11]. The capacitance is not taken into effects as its value is relatively small compare with resistance at the frequencies being considered. The resistance of each turn R_i is computed from the power dissipated in the turn due to the total current flow in it including eddy currents. Since eddy currents are frequency dependent, the values are determined at set frequency points and the quality factor (Q) of the inductor at these points calculated using the formula in Eq. 4.3.

$$Q = \frac{\left|\mathrm{Im}(Zin)\right|}{\left|\mathrm{Re}(Zin)\right|} \tag{4.3}$$

where Z_{in} is the input impedance at one terminal of the equivalent circuit with the other grounded. The inductance is obtained from the imaginary part of Z_{in} and the resistance from the real part of Z_{in}. The simulated Q and inductance as well as the resistance are shown in Figure 4.6 and Figure 4.7 respectively.

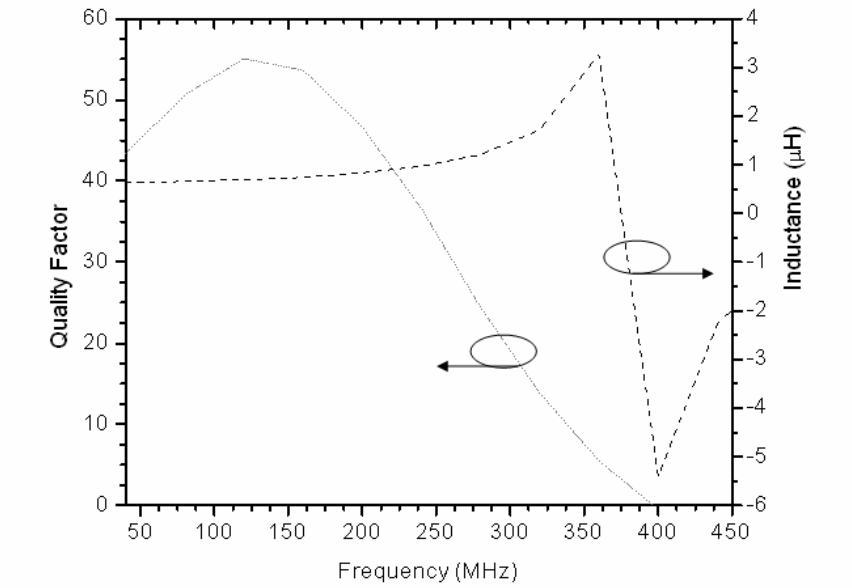

Figure 4.6. Simulated equivalent circuit quality factor and inductance for a 15 turn, 3mm×3mm embedded inductor. The inductor has a conductor width (w) of 30 μm spacing (g) of 20μm, depth (h) of 50 μm and oxide thickness of 2.5 μm.

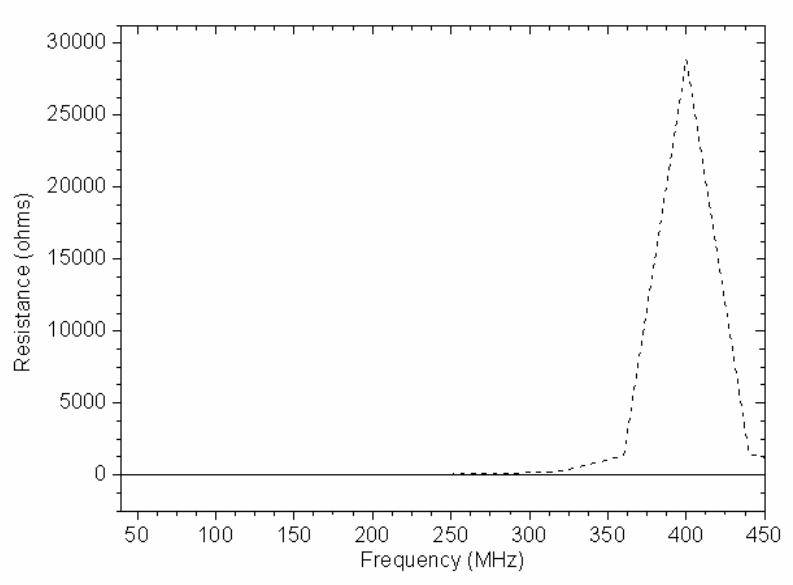

Figure 4.7. Simulated equivalent circuit resistance for a 15 turn, 3mm×3mm embedded inductor. The inductor has a conductor width (w) of 30 μm spacing (g) of 20μm, depth (h) of 50 μm and oxide thickness of 2.5 μm.

4.4 Low Frequency Test Methods in Low Resistvity Silicon

Calibration standards such as TRL, LRM and SOLT calibration are utilized in standard RF and Microwave testing of circuits. As mentioned in section 4.1, TRL calibration provides more accurate results than SOLT and LRM calibration as it removes the parasitics due to the measurement interface. At very low frequencies (hundreds of mega hertz), TRL is not practical thus SOLT or LRM calibration is used. Two main approaches utilizing on-wafer integrated feeds and discrete feeds are explored in the characterization of the E-DUT in 4.3 with fabrication details in appendix B using SOLT scattering (S) parameter and impedance measurement techniques. Two categories of approach are examined, a discrete and an integrated. One of the discrete feeding approaches (PC board) utilizes an impedance measurement technique while the other (duroid

substrate) utilizes the S parameter measurement technique. The integrated utilizes the S parameter technique.

4.4.1 PC Board Discrete Testing

4.4.1.1 Interface

This method of testing is a simple, low frequency (tens of Mega Hertz) approach based on impedance measurement. The E-DUT is attached to a piece PC board with metalized copper strips and the input and output connected to the PC board via wire bonds as shown in Figure 4.8. The PC board and E-DUT is connected to the HP impedance analyzer using short copper wires attached to the PC board using solder.

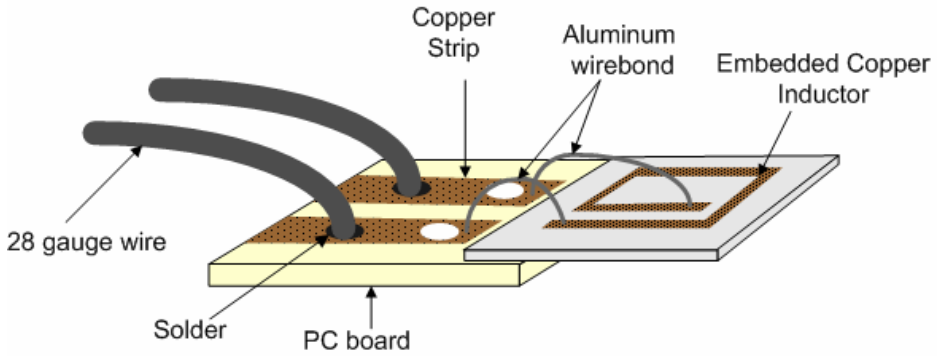

Figure 4.8. Illustration of PC board discrete testing interface with input and output port of 3D embedded DUT attached to copper strips on board using wirebonds. A length of 28 gauge wire used to interface with measurement system is soldered to each of the copper strips.

4.4.1.2 Measurement Approach

The device being characterized in this case does not only contain the E-DUT but also the wirebonds, copper strip and 28 guage wires. This device is connected to the Agilent 4395A network/spectrum/impedance analyzer through an Agilent 16092A spring clip fixture (Appendix B) as shown in Figure 4.9.

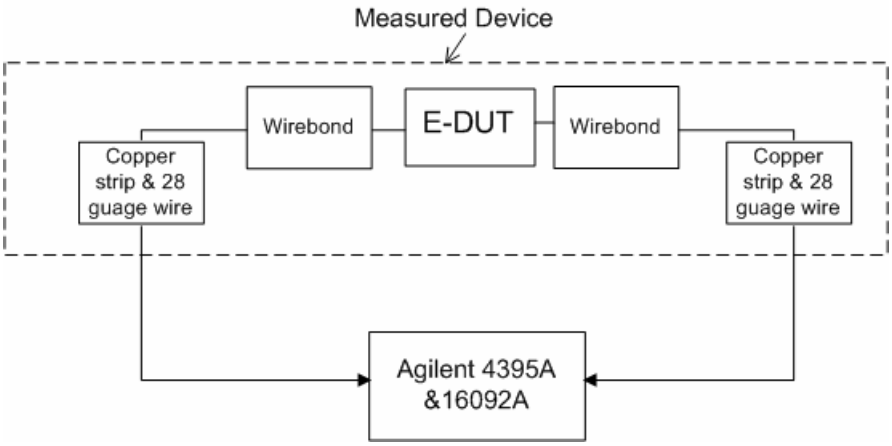

Figure 4.9. Illustration of measurement system for PC board testing of DUT.

The Agilent 16092A measurement fixture and 4395A impedance analyzer (frequency range of 10-500 MHz) is calibrated using a method similar to the SOLT but with a short and an open calibration standard only. The interface with the E-DUT establishes a good DC connection however stray capacitance and resistance are introduced into the measurement setup from the copper strips, wirebonds and extra wires attached to the E-DUT (illustration in Figure 4.9). The impedance analyzer measures the impedance of the device including from which it extracts the effective resistance, inductance and quality factor(Q).

4.4.2 Duroid Substrate Testing

4.4.2.1 Interface

In this case, the E-DUT is attached in series using aluminum wirebonds to a separate duroid fixture with CPW lines as shown in Figure 4.10. The parameter values for Figure 4.10 are shown in Table 4.1.

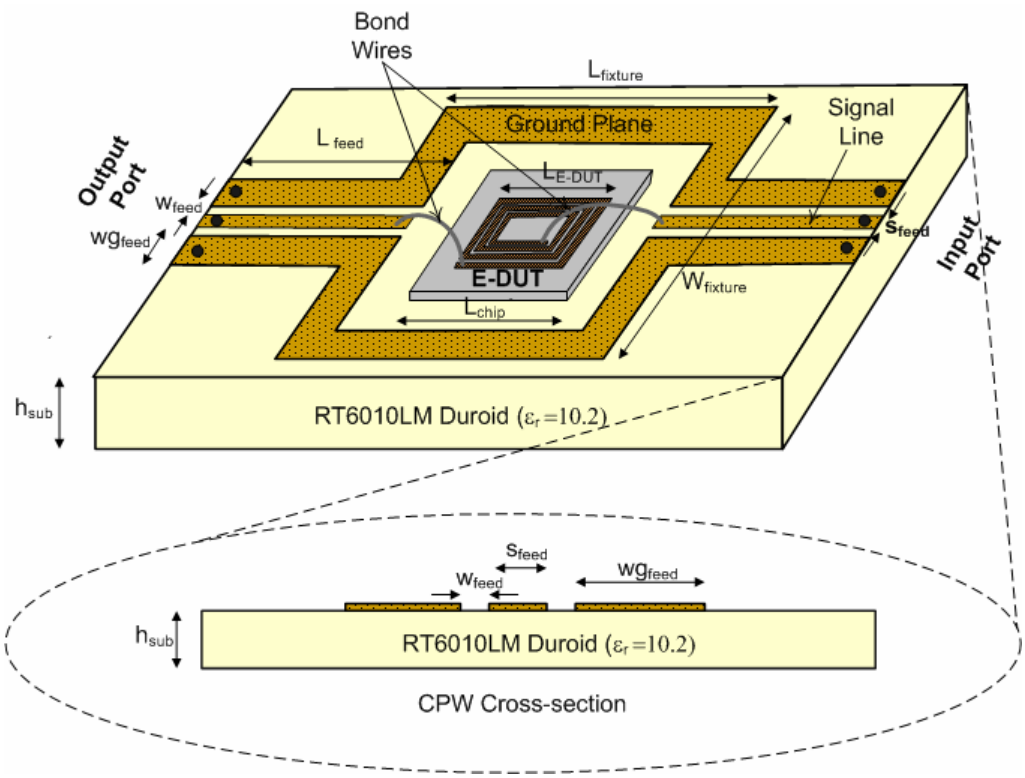

Figure 4.10. Illustration of duroid fixture with CPW feedlines designed to interface with 1250 μm pitch G-S-G cascade probes. E-DUT is attached is series using aluminum wirebonds to the CPW lines of the fixture.

Parameter	Dimension
L_{E-DUT}	3 mm
L_{chip}	~230 mils
s_{feed}	24 mils
w_{feed}	10 mils
wg_{feed}	54 mils
L_{feed}	400 mils
$L_{fixture}$	360 mils
$W_{fixture}$	560 mils
h_{sub}	25 mils

Table 4.1. Dimensions of duroid fixture measurement setup shown in Figure 4.10 and Figure 4.11.

The fixture is designed with 50 ohm CPW lines and a continuous ground plane on both sides. It is milled using a ProtoMat C60 milling machine (appendix A3) on RT6010LM duroid substrate with single-side 1/2 oz copper cladding. The dimensions of the CPW shown in Figure 4.10 are such that it can be easily fabricated with high repeatability and probed using 1250 μm pitched CPW probes. Having the E-DUT completely isolated from the feeding structure (on low loss substrate with loss tanget of 0.0023) minimizes the possiblilty of interaction between the test signal and the silicon substrate resulting in minimum loss. The duroid fixture adds unwanted parasitics to the measured result, therefore the fixture in Figure 4.11 is fabricated with similar dimensions to be used in extracting these effects from the measured response. The extraction process is discussed in section 4.5.

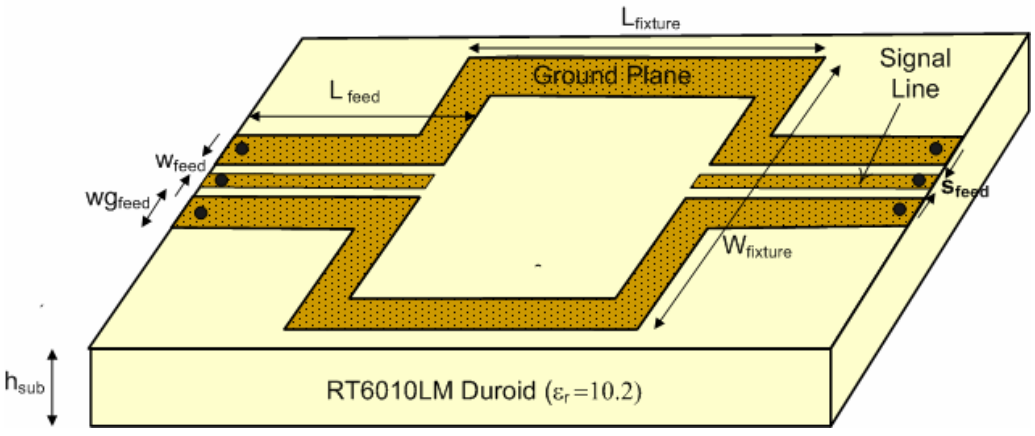

Figure 4.11. Illustration of duroid fixture with CPW feedlines designed to interface with 1250 μm pitch cascade probes. No E-DUT is attached to the fixture in this case.

4.4.2.2 Measurement Approach

The method of testing employed is based on S parameter measurement. The S parameters are measured using a SOLT calibration standard with the DUT on an air spacer as shown in Figure 4.12.

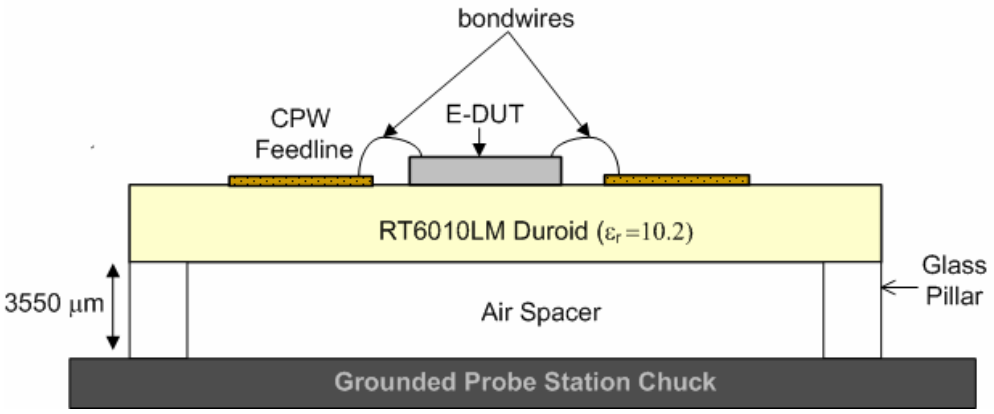

Figure 4.12. Setup for probes station measurement of S parameter of DUT on duroid fixture.

Measurement is done at identical frequency points for both structures shown in Figure 4.10 and Figure 4.11 with a HP 8510 C network analyzer on the probe station (Appendix B.1.2). Cascade probes with 1250μm pitch cascade are used to interface with the CPW lines on the duroid fixture.

4.4.3 Integrated Testing

4.4.3.1 Interface

This is the most repeatable testing approach with gold feedlines printed directly on a thick layer of oxide (~2.5 μm) on the conductive substrate using a lift-off technique (detailed in appendix A.1.2), as illustrated in Figure 4.13.

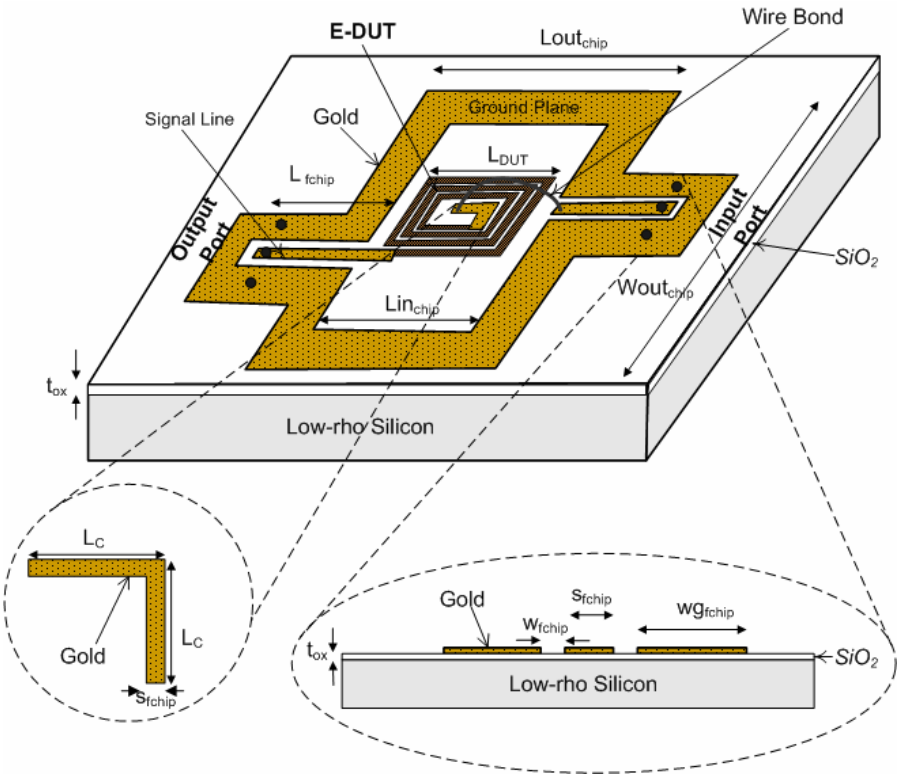

Figure 4.13. Illustration of the integrated CPW feedline fixture with E-DUT shown in the center of the structure. The feedline connects to the E-DUT directly at the output port while a wire bond is used as an airbridge to connect to it at the input port. The feedline structure is made of 1.5 μm thick gold.

Parameter	Dimension (mm)
L_{DUT}	3.000
s_{fchip}	0.080
w_{fchip}	0.050
wg_{fchip}	0.230
L_{fchip}	0.500
Lin_{chip}	4.000
$Lout_{chip}$	4.460
$Wout_{chip}$	8.800
t_{ox}	0.0025
L_C	0.79

Table 4.2. Dimension for on-wafer fixtures and DUT shown in Figure 4.13 and Figure 4.14.

The CPW feedlines of the integrated fixture are designed with an enclosed ground plane to maintain ground plane continuity. An L-shaped section is added to the center of the structure to facilitate the wire bonding process is used to form an air bridge.

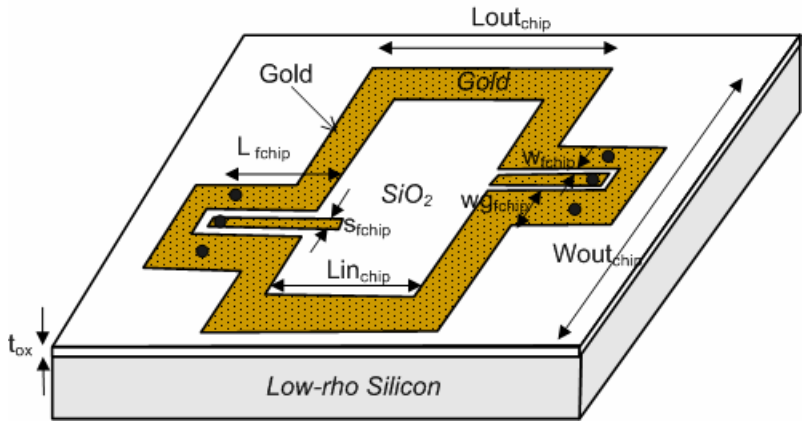

Figure 4.14. Illustration of the integrated CPW feedline fixture without E-DUT. The feedline structure is made of 1.5 μm thick gold.

The oxide layer of the CPW feedline (cross-section of Figure 4.13) gives rise to a MIS structure that is more lossy compared to the duroid feedline used in the previous section. As in the previous section, a separate fixture shown in Figure 4.14 is fabricated to facilitate in the extraction of parasitics from the measured E-DUT response. T

4.4.3.2 Measurement Setup

This method of testing is also based on S-parameter measurement. Measurement is done on-wafer using a probes station and the HP 8510 C network analyzer (Appendix B.1.2). The S-parameters of the E-DUT are measured with a SOLT calibration standard using 150 μm pitched CPW Cascade

Microtech probes to interface with gold CPW lines printed on the substrate. An air spacer similar to that shown in Figure 4.12 was used to measure the S-parameters of both devices in Figure 4.13 and Figure 4.14 at identical frequency points.

4.5 Results and Discussion

In order to obtain the DUT response from the measured SOLT S-parameter result for the duroid fixture and integrated on-wafer feedline measurement approach, the feed structure is extracted using an extraction technique similar to that detailed in [15]. The measured S-parameter result obtained for the fixture with and without the E-DUT is represented by the equivalent π-network circuits shown in Figure 4.15 (a & b) and Figure 4.16 (a & b) for the duroid fixture and integrated fixture measurement setup respectively.

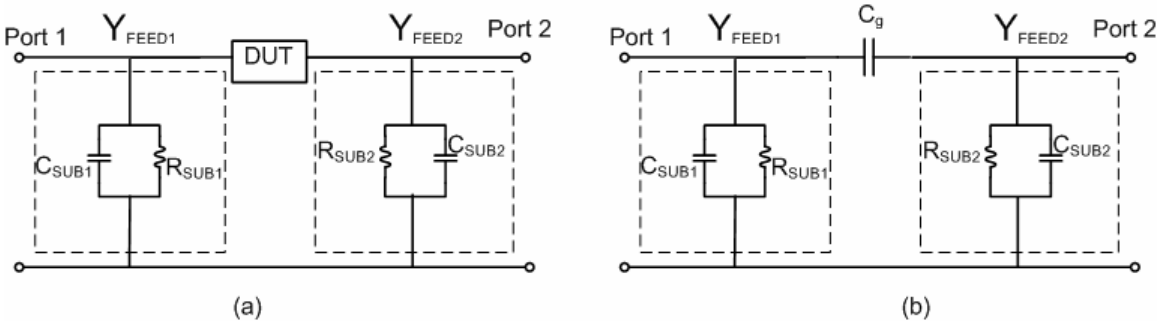

Figure 4.15. Circuit model representation of measured response (a) with and (b) without E-DUT using duroid CPW feedline fixture in section 4.4.2. DUT consist of the E-DUT and bondwires used to attach it to the fixture.

The substrate loss of the feedlines at port 1 and port 2 is represented as R_{SUB1} and R_{SUB2} and the capacitive coupling to the substrate as Cf_{SUB1} and Cf_{SUB2}. C_g represents the gap capacitance between port 1 and port 2 of the duroid fixture

when the E-DUT is not present. The DUT in Figure 4.15(a) consists of the E-DUT and the two wirebonds used to attach it to the duroid fixture.

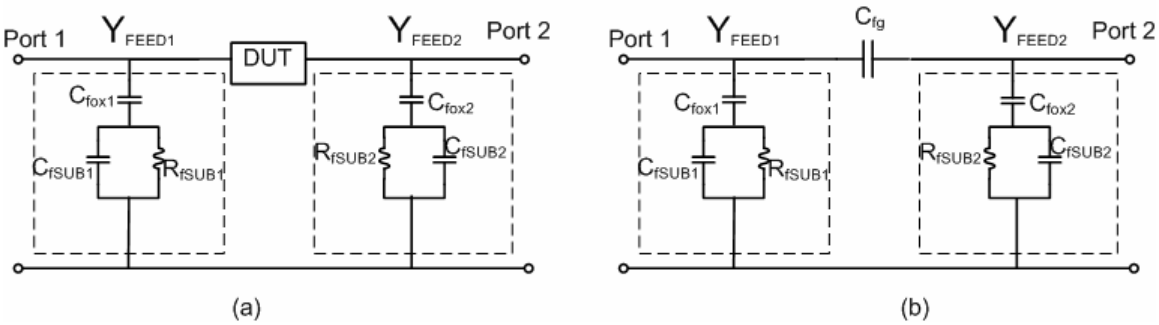

Figure 4.16. Circuit model representation of measured response (a) with and (b) without E-DUT for integrated CPW feedlines fixture in section4.4.3. DUT consists of single bondwire and on-wafer L-shaped high impedance line.

The substrate loss of the feedlines at port 1 and port 2 is represented as R_{fSUB1} and R_{fSUB2} and the capacitive coupling to the substrate as C_{fSUB1} and C_{fSUB2}. The capacitive coupling to the oxide at port 1 and 2 are represented by C_{fox1} and C_{fox2} while C_{fg} represents the gap capacitance between port 1 and port 2 of the integrated fixture when the E-DUT is not present. The DUT in Figure 4.16(a) consist of the E-DUT, the wirebond air bridge and the L-shaped high impedance line in the center of the E-DUT structure.

The admittance of the feeding structure at port 1 and port 2 for the measured fixture without the E-DUT is determined at specific frequencies using the measured S-parameter and the expression in Eq. 4.4 and Eq. 4.5 respectively.

$$Y_{FEED1}(\omega_i) = Y_{ref11}(\omega_i) + Y_{ref12}(\omega_i) \tag{4.4}$$

$$Y_{FEED2}(\omega_i) = Y_{ref22}(\omega_i) + Y_{ref21}(\omega_i) \tag{4.5}$$

where Y_{ref} is the measured admittance of the feedline fixtures without the E-DUT.

This result is used to extract the feed lines response from the measured results of the DUT and feed structure using a cascaded T-network approach (Figure 4.17) and Eq. 4.6 and 4.7.

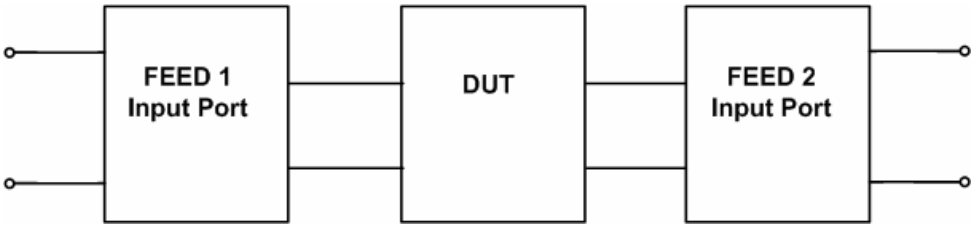

Figure 4.17. Cascade representation of DUT and feed Structure in Figure 4.15 and Figure 4.16.

$$T_{ind}(\omega_i) = T_{FEED}(\omega_i) \cdot T_{\pi}(\omega_i) \cdot T_{FEED}(\omega_i) \tag{4.6}$$

$$T_{\pi}(\omega_i) = T_{FEED}^{-1}(\omega_i) \cdot T_{Ind}(\omega_i) \cdot T_{FEED}^{-1}(\omega_i) \tag{4.7}$$

The extracted DUT parameters are used to determine the quality factor of the structure using Eq. 4.8. The inductance and resistance are obtained from the imaginary and real parts of $Y_{\pi 11}$ respectively.

$$Q(\omega_i) = \frac{\mathrm{Im}\left(\frac{1}{Y_{\pi 11}(\omega_i)}\right)}{\mathrm{Re}\left(\frac{1}{Y_{\pi 11}(\omega_i)}\right)} \tag{4.8}$$

where $Y_{\pi 11}$ is admittance parameter obtained from the extracted T-parameters of the DUT T_{π}.

The extracted result for the Q of the DUT using different test set-ups shown in Figure 4.18 - Figure 4.19 indicate that the PC board test method is overwhelmed by parasitic capacitances that cause its resonance frequency to decrease by a factor of four compared to the duroid and integrated fixture setups. The copper

strip on the PC board is a major source of this capacitance. While the resonance frequency of the duroid fixture and integrated testing are similar, the quality factor of the integrated testing is almost half that of the duroid fixture setup. This difference in Q can be attributed to an increase in resistance for the integrated setup (as extracted inductance (Figure 4.20) for both is similar) as is clearly shown in the inset in Figure 4.19. This resistance increase is caused by resistance of the high impedance line used to facilitate the bonding process in the integrated approach. Its effect is significant due to its length and the loss properties of the substrate.

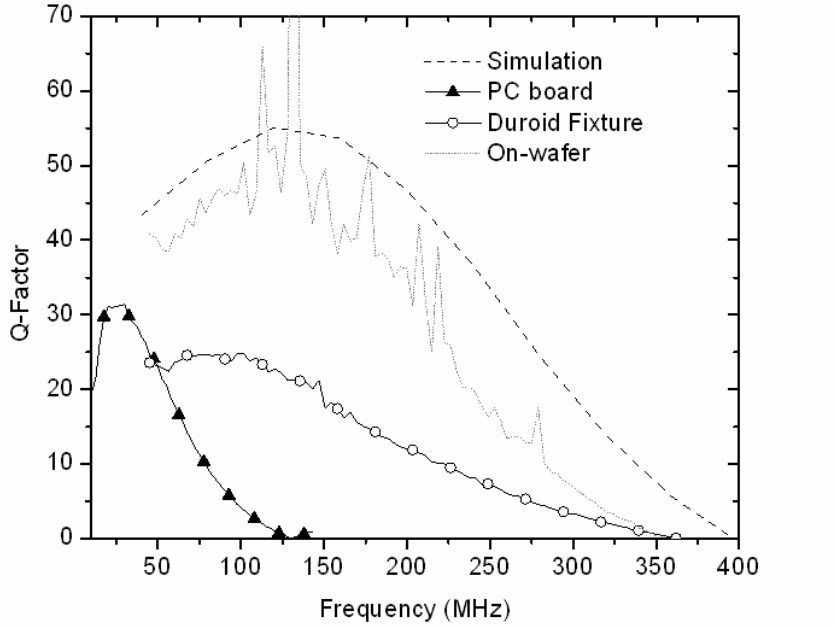

Figure 4.18. Quality factor of E-DUT obtain using the PC board with measurement, duroid with bondwires and integrated fixture approach with bondwire and high impedance line.

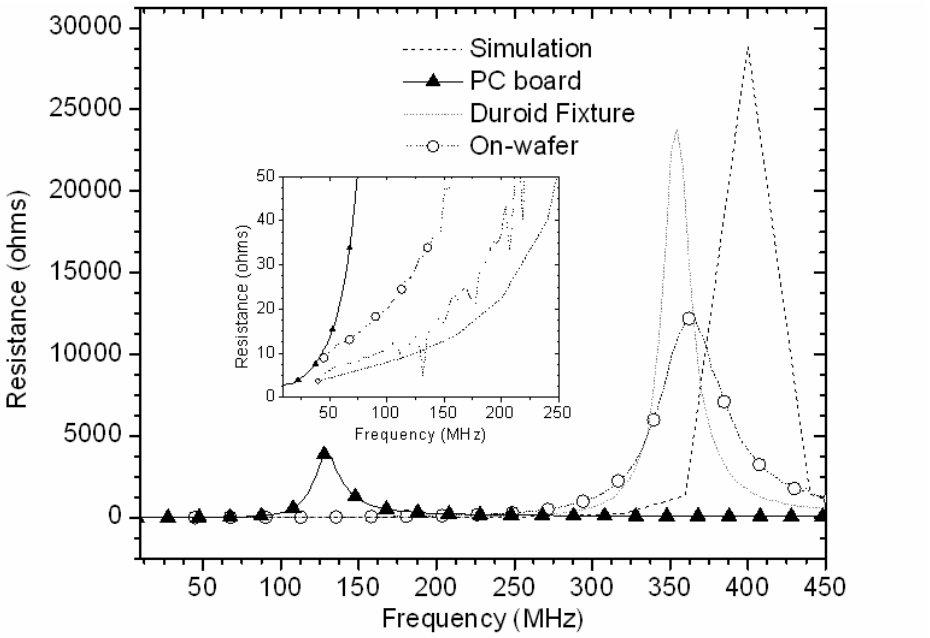

Figure 4.19. Extracted resistance of E-DUT obtain using the PC board with measurement, duroid with bondwires and integrated fixture approach with bondwire and high impedance line.

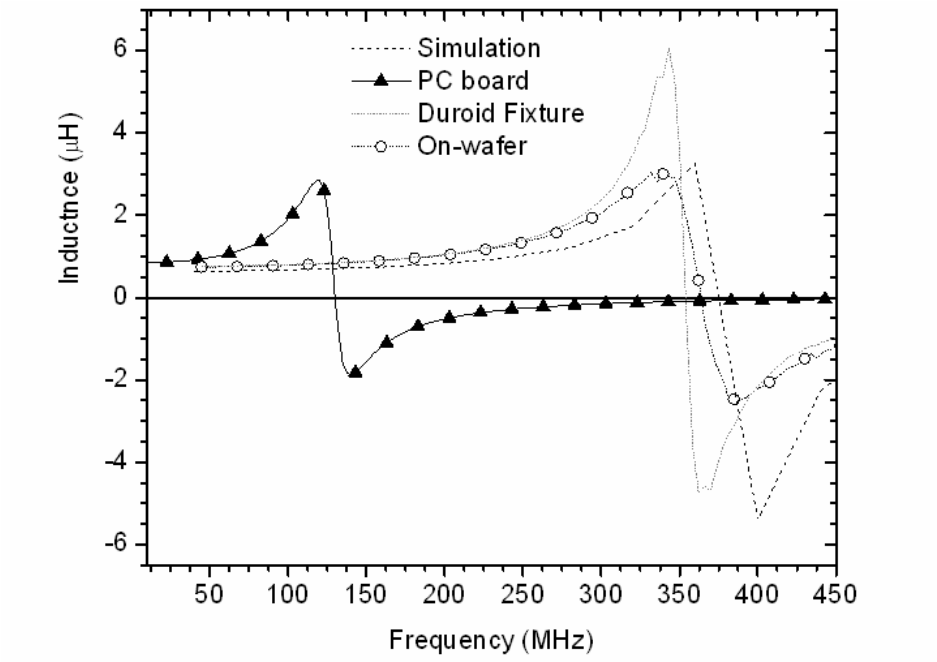

Figure 4.20. Extracted inductance of E-DUT obtain using the PC board with measurement, duroid with bondwires and integrated fixture approach with bondwire and high impedance line. Measured and extracted inductance values for DUT using PC board, duroid and integrated fixture approach.

The inductance value extracted using all three methods are quite similar. The PC board result is about 0.05 μH higher than the duroid and on-wafer due to the extra wires present in the result.

The Q factor simulation result closely follows the extracted result obtained using the duroid fixture. The inductance and resistance are a little lower than the extracted values as they do not include bondwires and are only a geometrical approximation of the actual structure.

4.6 Summary

Three different approaches to characterize low frequency E-DUTs on lossy substrates have been explored. While an integrated approach offers the most repeatability and the option of batch processing, parasitics loss can significantly degrade the result obtain using this method. The duroid fixture test approach provides a suitable method for characterizing embedded devices. Repeatability is a concern and it is only feasible in low volume testing. The PC board approach overwhelms the results with parasitic effects and is therefore unsuitable in testing such devices.

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Chapter 5: Conclusion and Future Work

5.1 Conclusion

This thesis has successfully demonstrated the viability of the embedded conductor design approach to attain size reduction in passives. It has also introduced the concept of mixed material design for board level application.

The embedded approach for low impedance lines demonstrated on high resistivity silicon using CPW lines achieved approximately 50 % reduction in length compare with a surface structure. A stepped impedance filter designed using embedded CPW lines achieved a 23 % reduction in length compared to a surface CPW implementation. Improvement in performance was also demonstrated with an increase in stopband attenuation of 10dB over a surface structure.

The mixed material approach demonstrated with duroid/air achieved approximately 50% reduction in effective dielectric constant with a 40% air composition. Simulation results demonstrated that it could be used in the development of three-dimensional passives such as filters.

Also demonstrated is this ability to characterize embedded passives in lossy substrates. The discrete test method using an isolated fixture to interface with the device produced the best result. Though the use of an integrated test fixture offers very good repeatability, the sensitivity of the approach to the interface design severely limited the achievable results.

5.2 Future Work

The next step in the embedded conductor design is to consider further improvement in length reduction with the used of conductors that are embedded between two substrate layers. Combinations of this approach with techniques such as folded inductors should also be used to achieve further size reduction.

Exploration of a reduction in the length of mixed dielectric designs using a folding technique that maintains the basic property of the device should be investigated. This should be succeeded by fabrication and verification of the performance of such structures.

The On-wafer measurement approach should be further explored with the use of air bridges to connect to the innermost turn of the inductor structure to verify testability.

Appendices

Appendix A: Fabrication

Introduction

The fabrication and suggested fabrication approach for all circuits presented in this thesis are detailed below in this appendix. Some of the structures make use of similar process and it is so noted when this occurs.

A1. Embedded Inductor Fabrication

The original embedded inductor process was developed by Tingrui Pan and Antonio Baldi of the Electrical Engineering Department at the University of Minnesota (U of MN). While the original lift-off process recipe was developed by Kevin Roberts of the Nanofabrication Center (NFC) at the University of Minnesota. All fabrication was done as the Nanofabrication Center (NFC) facility at the U of MN, Minneapolis Campus.

Number of Masks = 3

Name of Masks: Inductor Geometry (1) Backside oxide Etch (2) On-wafer Feedline (3)

A1.1 Embedded Metallization Process

1. Clean new wafers
    a. RCA clean single-sided polished wafer to remove organic contaminants.
2. Define Inductor geometry with Reactive Ion Etch

a. Solvent clean wafer with Acetone(ACE) / Isopropanol(IPA) (3min/3min).
b. Rinse in DI water (3 cycles) and spin dry.
c. Dehydrate bake in 150^{o}C oven for 20 min or on 115^{o}C hot plate for 2 min.
d. Vapor prime in HDMS for 3 min.
e. Coat frontside of wafer with 5.5 μm of Shipley 1045 photoresist (PR).
    i. Spin Shipley 1045 PR at 3.5 k rpm for 40 sec (~ 5.5 μm).
    ii. Softbake in 105^{o}C oven for 10 min or on 105 ^{o}C hotplate for 30 sec.
f. Expose PR using Karl Suss MA6 Aligner for 35 sec at 12 W/cm^2 power.
g. Immerse in Shipley 351:H_2O 1:5 developer for 75 sec with slight agitation.
h. Rinse in DI water (3 cycles) and dry with N_2 gun.
i. Inspect under microscope to ensure resist developed properly, if not immerse in Oxygen (O_2) asher for 45 sec (250 mtorr O_2 flow and 250 mW power) to ensure residual resist is completely removed. Repeat as needed.
j. Hard bake in 120^{o}C oven for 20 minutes or on 120^{o}C hotplate for 60 sec.

k. Etch inductor geometry into wafer using BOSCH process in Deep Reactive Ion Etcher (DRIE). Duration of etch depends on required depth of inductor.

l. Remove PR using ACE / Methanol (MET) / IPA (3min/3min/3min).

m. Rinse in DI wafer (3 cycles) and dry with N_2 gun.

3. Create thermal oxidation layer

    a. Solvent clean wafer ACE / IPA (3min/3min).

    b. Rinse in DI water (3 cycles) and spin dry.

    c. Dehydrate bake in 150^{o}C oven for 20 min or on 115^{o}C hot plate for 2 min.

    d. Load wafer in quartz boat and into Oxidation tube.

    e. Using Recipe STM-1150 (NFC, U of MN) grow 2.4 μm thick wet thermal oxide at 1150^{o}C.

    f. Measure thickness of oxide at several locations of wafer using Ellipsometer.

4. Sputter Titanium (Ti) / Copper (Cu) Seed Layer

    a. Solvent clean wafer ACE / IPA (3min/3min).

    b. Rinse in DI water (3 cycles) and spin dry.

    c. Dehydrate bake wafer in 150^{o}C oven for 20 minutes or on 115^{o}C hot plate for 2 minutes.

    d. Deposit 100A/5000A of Ti/Cu seed layer using AJA RF/DC Sputterer (U of MN).

5. Reverse Pulse Copper Electroplating Process

a. Prepare Electroplating Solution (1 Liter) Technic Copper CU 2300:
    i. 600 ml of DI water.
    ii. 75g of electronic grade Copper Sulphate ($CuSO_4$).
    iii. 100 ml of C.P. grade concentrated Sulphuric acid (H_2SO_4).
    iv. 0.19 ml of C.P. grade concentrated Hydrochloric acid (HCl).
    v. 5 ml of TECHNIC Cu 2300 Brightener.
    vi. 7.5 ml of TECHNIC Cu 2300 Carrier.
b. Position platinum electrode and secure on one side of electroplating tank.
c. Pour electroplating solution into electroplating tank using a 1μm polypropylene filter cartridge. Use a magnetic stirrer to stir solution at a constant rate throughout the electroplating process to keep ion concentration in solution uniform.
d. Electroplate on a dummy wafer coated with Ti/Cu seed layer (Perform whenever freshly mixed solution is being used).
    i. Insert dummy wafer into electroplating fixture and clamp down using electrodes contacts. Position in tank and secure directly across from platinum electrode (anode).
    ii. Connect positive terminal of PULSE POWER SUPPLY (DYNATRONIX DuPRO -1-3) to platinum anode and negative terminal to wafer fixture electrodes.

iii. Allow wafer to seat in solution for 1 min to remove copper oxide buildup on surface of wafer.

iv. Turn ON power supply with forward pulse of duration, 1ms and current supply at 300 mA (current density =15mA/cm^2) and electroplate for 60 min.

v. Turn pulse power supply OFF, remove and rinse fixture and dummy wafer.

vi. Remove dummy wafer from holder and dry with N_2 gun.

e. Insert wafer sample into fixture, turn pulse power supply ON with forward pulse of duration 1ms and current of 300 mA (current density =15mA/cm^2) and forward electroplate for 15 minutes.

f. Switch OFF pulse power supply. RESET with forward pulse of duration of 1ms and current of 300 mA (current density =15mA/cm^2) and reverse pulse duration of 3ms and current of 150mA (current density 2.5 mA/cm^2).

g. Switch ON pulse power supply and electroplate for 2.0 hours.

h. Remove wafer from fixture and rinse in DI water. Dry immediately with N_2 gun.

i. Inspect electroplating in trenches using microscope to ensure uniformity in coverage.

j. Re-insert wafer into fixture, place into electroplating solution, electroplate until trenches are completely filled. Rotate wafer by 180^o approximately halfway through the process to maintain

uniformity in electroplating. Total electroplating time for etched trenches with 30 μm width is 8.5 to 9.0 hours.

k. Remove wafer fixture from solution, rinse in DI wafer (3 min). Then remove the wafer from fixture and rinse again in DI water (3 min). Dry immediately with N_2 gun.

6. Chemical Mechanical polishing of Cu to smoothing surface

   a. Prepare Chemical Mechanical Polishing (CMP) Solution (1 gallon).

      i. 3450 ml of DI water into appropriate container.

      ii. 50 ml of nitric acid (HNO_3).

      iii. 3.5 g of Benzotrizole.

      iv. 45 g of 1 μm Deagglomerated Alpha Alumina (Al_2O_3).

   b. Polish excess copper on surface of wafer using Lapping Machine and CMP solution. Polish until inductor structures are completely visible.

   c. Immerse wafer immediately in acetone for 10-20 min to remove CMP residue.

   d. Rinse wafer with IPA and DI water (3min/3cycles) and dry with N_2 gun.

A1.2 On-wafer Feedline Process using Lift-off Resist (LOR) 20B

1. Define Feedline Geometry with Lift-off Resist (LOR) 20B process

   a. Rinse wafer in DI wafer (3cycles) and dry with N2 gun.

b. Dehydrate bake in 150^{o}C oven for 20 min or on 115^{o}C hot plate for 2 min.

c. Coat frontside of wafer with 5.5 μm of Shipley 1045 photoresist (PR).

    i. Spin MicroChem LOR 20B resist at 1000 rpm for 45 secs (~3. 7 μm).

    ii. Softbake LOR on 170 ^{o}C hotplate for 2 min.

d. Coat frontside of wafer with 1.3 μm of Shipley 1813 photoresist (PR).

    i. Spin Shipley 1813 PR at 3.5 k rpm for 30 sec (~ 1.3 μm).

    ii. Softbake in 105^{o}C oven for 10 min or on 105 ^{o}C hotplate for 60 sec.

e. Expose PR using Karl Suss MA6 Aligner for 6 sec at 12 W/cm^2 power.

f. Immerse in Shipley 351:H_2O 1:5 developer for 25 sec with slight agitation.

g. Rinse in DI water (3 cycles) and dry with N_2 gun.

h. Oxygen (O_2) ash for 2min in vertical position (250 mtorr O_2 flow and 250 mW power) to ensure residual resist is completely removed.

i. Hard bake double layer resist on 180^{o}C hotplate for 3 min.

j. Immerse in AZ Electronic Material 400K:H_2O 1:4 developer for 90 sec to develop LOR 20B resist.

k. Oxygen (O_2) ash for 2min in vertical position (250 mtorr O_2 flow and 250 mW power) to ensure residual LOR 20B resist is completely removed.

2. E-beam 100A/15000A of Ti/Au metal layer using CHA E-beam (U of MN).
3. Metal Layer Lift-off
    a. Immerse wafer vertically into MicroChem EBRPG solvent at 60^{o}C.
    b. Immerse in ACE / Methanol (MET) / IPA (3min/3min/3min).
    c. Rinse in DI water (3 cycles) and dry with N_2 gun.

A1.3 Bulk Silicon Micromachining

1. Backside Oxide Etching
    a. Vapor prime wafer in HDMS for 3 min
    b. Coat backside of wafer with 5.5 μm of Shipley 1045 photoresist (PR). See (2e).
    c. Coat frontside of wafer with 5.5 μm of Shipley 1045 photoresist (PR). See (2e).
    d. Expose PR with Karl Suss MA6 Aligner for 35 seconds at 12 W/cm^2 power.
    e. Immerse in Shipley 351:H_2O 1:5 developer for approximately 75 sec with slight agitation.
    f. Rinse in DI water on removal and inspect.
    g. Plasma etch residual PR on wafer in O_2 asher for 45 sec.
    h. Etch backside oxide on wafer using BOE (1:10 HF:H_2O).

i. Remove resist using ACE/MET/IPA (3min/3min/3min). Rinse in DI water (3 cycles) and dry with N_2 gun.

2. Wet Etching of Bulk Silicon
    a. Prepare Potassium Hydroxide (KOH) solution, with concentration 45% at 80 ^{o}C.
    b. Insert wafer in wet etch fixture. Ensuring fixture is properly sealed, insert into KOH bath and allow most of the bulk silicon underneath inductor structure to etch.

    Note: This fixture is designed to protect one side of the wafer in the KOH bath.

    c. Remove wafer from fixture, rinse with DI water and dry with *LOW PRESSURE* N_2 gun to prevent breakage of silicon membranes on inductors.
3. Dry Etching of Remaining Silicon Substrate
    a. Use BOSCH process in DRIE, etch the remaining silicon in KOH etched trench on the backside of wafer.

A2. Embedded CPW Line and Filter Fabrication

The fabrication process for the embedded filter makes use of 2 masks. The first mask is used to create embedded sections of copper in the substrate. The second mask is then use to create a surface structure over the embedded sections.

Number of Masks = 2

Mask Names: Embedded Section (1) Front Feedline (2)

A2.1 Embedded Metallization Process

1. Clean new wafers
    a. RCA clean single-sided polished high resistivity wafer to remove organic contaminants.
2. Define Embedded geometry with Reactive Ion Etch
    a. Using process in A1.1.2 etch geometry of embedded sections of filter into silicon substrate using the Plasmatherm SLR-770 Deep Trench Etcher.
3. Sputter Titanium (Ti) / Copper (Cu) Seed Layer
    a. Using process in A1.1.3 deposit 100A/5000A Ti/Cu seed layer on DRIE etched substrate.
4. Reverse Pulse Copper Electroplating Process

a. Reverse Pulse Electroplate copper into etched trenches with Ti/Cu seed layer using process in A1.1.4.

5. Chemical Mechanical polishing of Cu to smoothing surface
    a. Prepare Chemical Mechanical Polishing (CMP) Solution (1 gallon).
        v. 3450 ml of DI water into appropriate container.
        vi. 50 ml of nitric acid (HNO_3).
        vii. 3.5 g of Benzotrizole.
        viii. 45 g of 0.3 μm Deagglomerated Alpha Alumina (Al_2O_3).
    e. Polish excess copper on surface of wafer using Lapping Machine and CMP solution. Polish until inductor structures are completely visible.
    f. Immerse wafer immediately in acetone for 10-20 min to remove CMP residue.
    g. Rinse wafer with IPA and DI water (3min/3cycles) and dry with N_2 gun.

A2.2 Surface Electroplating

Sputtering Titanium (Ti) / Copper (Cu)/ Titanium (Ti) Seed Layer

Solvent clean wafer ACE / IPA (3min/3min).

Rinse in DI water (3 cycles) and spin dry.

Dehydrate bake wafer in 150^{o}C oven for 20 minutes or on 115^{o}C hot plate for 2 minutes.

a. Deposit 100A/5000A/100A of Ti/Cu seed layer using CHA E-beam (U of MN).

2. Define Surface Circuits

a. Vapor prime wafer in HDMS for 3 min

b. Coat frontside of wafer with polished embedded sections with 5.5 μm of Shipley 1045 photoresist (PR). See (2e).

c. Expose PR with Karl Suss MA6/BA6 Aligner for 35 seconds at 12 W/cm^2 power.

d. Immerse in Shipley 351:H_2O 1:5 developer for approximately 75 sec with slight agitation.

e. Rinse in DI water on removal and inspect.

f. Plasma etch residual PR on wafer in O_2 asher for 45 sec.

g. Etch backside oxide on wafer using BOE (1:10 HF:H_2O).

h. Remove resist using ACE/MET/IPA (3min/3min/3min). Rinse in DI water (3 cycles) and dry with N_2 gun.

3. Electroplate Surface Circuits

Etch top titanium seed layer by immersing in Transene Titanium etchant type TFT.

a. Prepare electroplating solution using process in A1.1.5 (a-d).

b. Insert wafer sample into fixture, turn pulse power supply ON with forward pulse of duration 1ms and current density of $5mA/cm^2$ and forward electroplate for 50 minutes (~ 5μm).

c. Remove wafer fixture from solution, rinse in DI wafer (3 min). Then remove the wafer from fixture and rinse again in DI water (3 min). Dry immediately with N_2 gun.

4. Back-etch Ti/Cu Seed layer
    a. Etch Cu seed layer by immersing in Copper Etchant APS-100 (Transene Inc.).
    b. Etch bottom Ti seed layer by immersing in Titanium Etchant type TFT (Transene Inc.).
    c. Rinse wafer with DI water (3cycles) and dry with N_2 gun.

A3. Fabrication of Bilayer Microstrip Line

The bilayer microstrip was fabricated using a 50 mil thick Rogers RT6010LM substrate with a relative dielectric constant of 10.2. The metallization on the substrate was rolled copper with a thickness of 1.4 mils. The bilayer substrate microstrip shown in figure was fabricated with a microstrip feed to enable it to be measured using a standard microstrip fixture. An illustration of the fabricated structure is shown in figure.

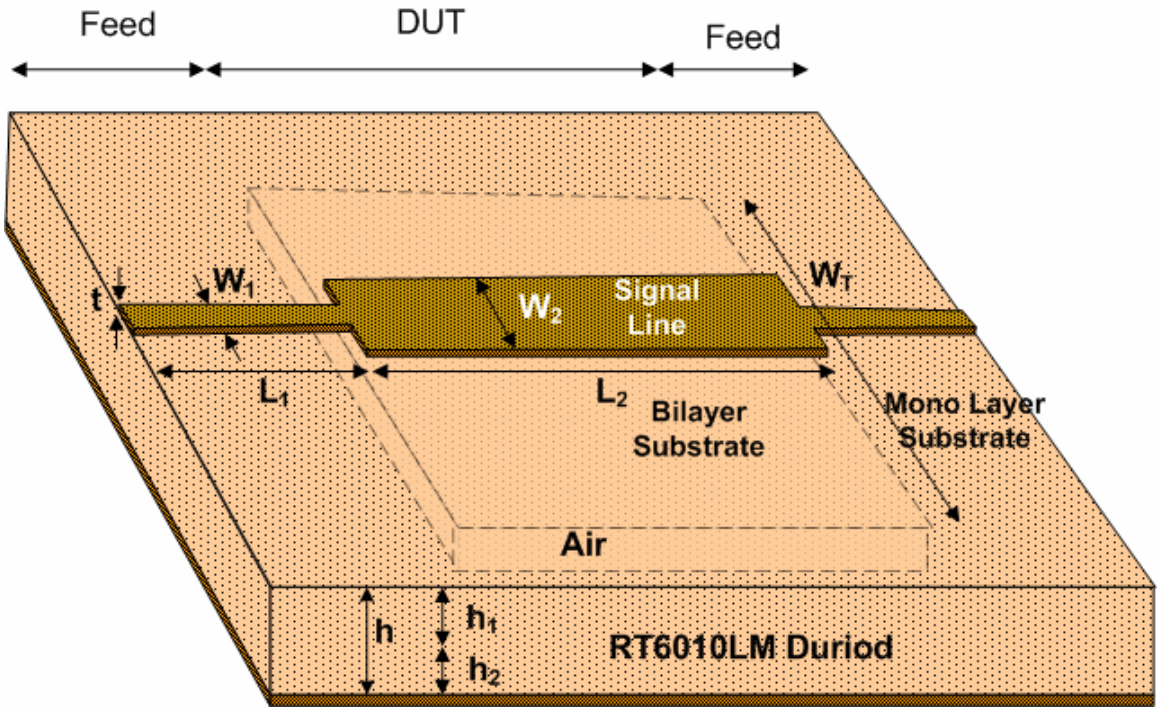

Figure A 1 : Illustration of bilayer microstrip (DUT) fabricated with microstrip feedlines for standard microstrip interface measurement using ProtoMat C60 milling machine.

The parameter values of the fabricated structure in Figure A 1 are shown in Table A 1.

Parameter	Value (mils)
W_1	44
W_2	126
L_1	394
L_2	788
h	50
h_1	21
h_2	29
t	1.4
W_T	788

Table A 1. Parameters of fabricated duroid /air dielectric substrate microstrip line in Figure A 1.

The full miocrostrip regions or feed on the edges were designed to so that the signal could be launched into the bilayer microstrip structure (DUT in Figure A 1) using a standard microstrip testing fixture shown in appendix [B-]. The full height duroid can withstand the clamping force of the microstrip fixture (appendix B1).

The fixture is fabricated using a Promat C60 milling machine shown in Figure A 2. The signal line on the top of the substrate is milled using the milling machining and remaining copper on topside of the substrate remove. The substrate is then flip with a guiding structure ensuring geometrical accuracy is maintained. An air cavity is milled into the backside of the substrate using the milling machine. Copper tape is placed on the backside of the substrate to serves as a ground plane as illustrated in Figure A 3.

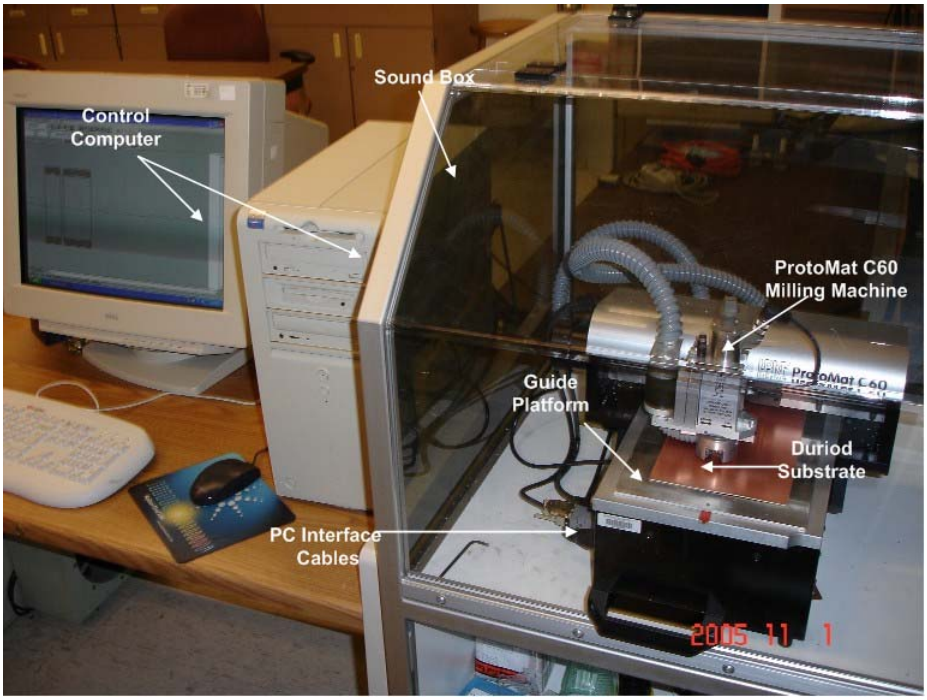

Figure A 2: Setup used for milling devices showing computer controlled ProMat C60 milling machine.

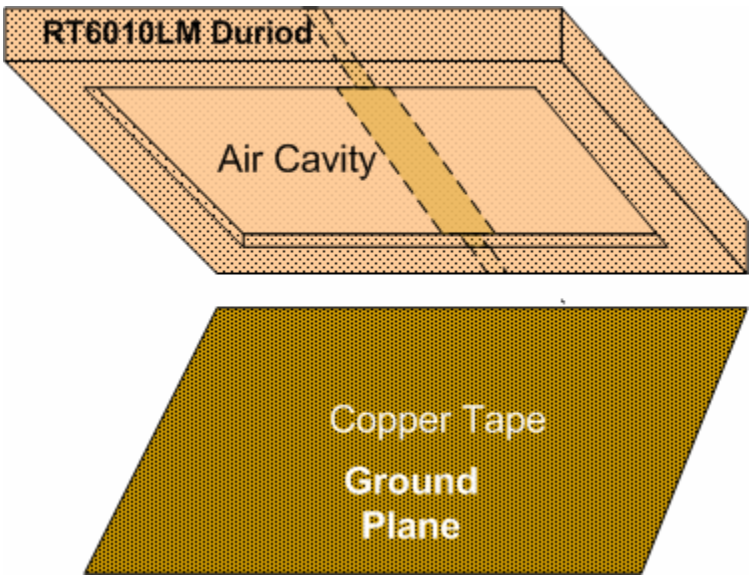

Figure A 3: Illustration of fabricated duroid/air bilayer microstrip assembly

The S-parameter of the structure was measured using an HP 8510 network analyzer and microstrip fixture calibrated with a TRL calibration standards discussed in section 2.3 of appendix B. The effective dielectric constant of the bilayer substrate was extracted from the measure results using technique discussed in section 3 of appendix B.

APPENDIX B: TEST and MEASUREMENT

B.1 Test Equipment

B.1.1 Microstrip Test Fixture

The microstrip test fixture shown below in figure B.1.1 was used to interface all microstrip based DUTs with the HP8510 network analyzer. The Inter-Continental Microwave (ICM) fixture (Model No. WK-3001-B) with 3.5mm connectors is design to operate from DC to 26.5 GHz.

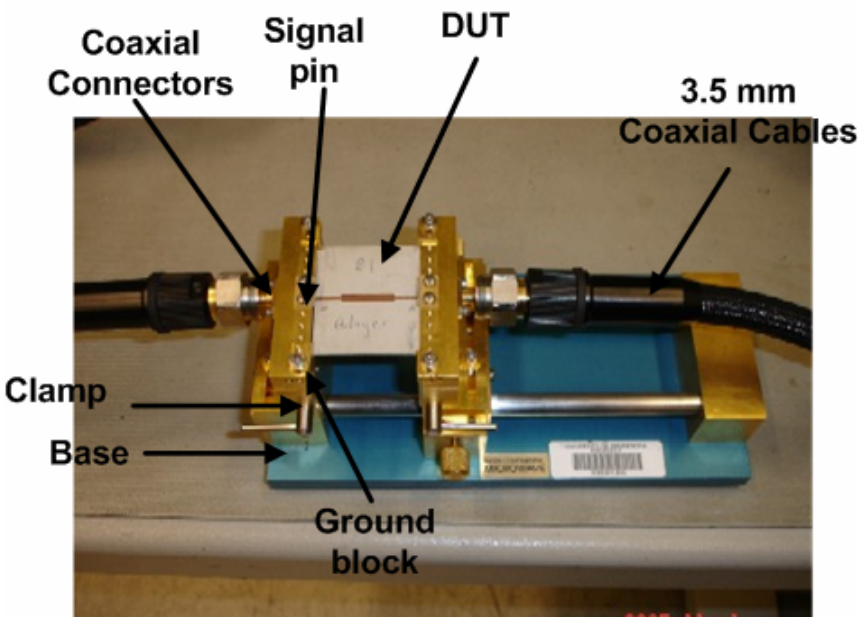

Figure B. 1. Intercontinental Microwave (ICM) fixtures used to interface microstrip based circuits with Network Analyzer

B.1.2 Network Analyzer Test Setup

B.1.2.1 Microstrip Measurement Setup

The HP 8510C network analyzer is used to measure the scattering matrix response data of the bilayer microstrip using the fixture in Figure B.1. The

microstrip fixture is connected to the test set using 3.5 mm cables as shown in Figure B.2.

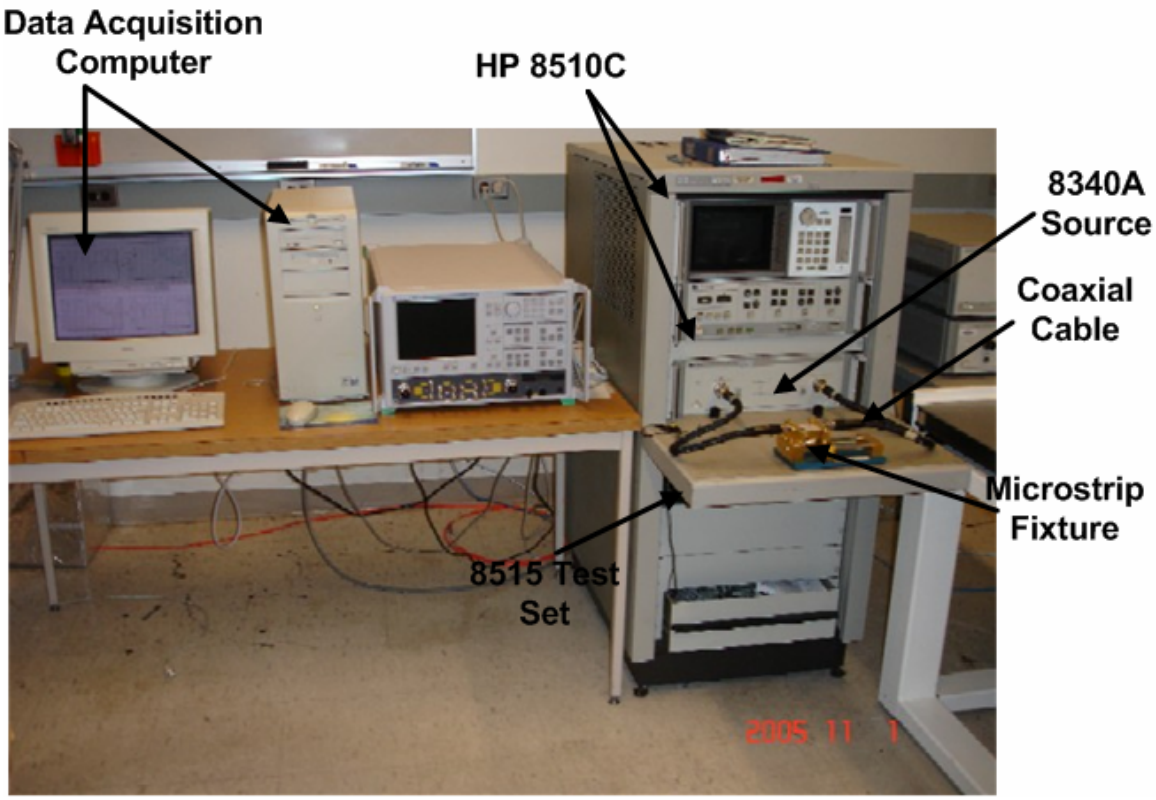

Figure B. 2. Measurement setup for bilayer microstrip measurements with HP 8510C network analyzer and Intercontinental Microwave fixture.

The HP 8510 is interfaced with the computer running MultiCal software. This is used to acquire measured results of the calibration standards which are used to determine calibration coefficient that are then stored in the non-volatile memory of the network analyzer to be used for measurement.

B.1.2.2 On-wafer Probe Measurement Setup

The setup shown in Figure B.3 was used to measure the scattering parameters of the on-wafer coplanar waveguide lines and filters using the Cascade MicroTech probe station. The network analyzer source is capable of

measurements between 45 MHz and 50 GHz. Scattering matrix response data are acquired from the network analyzer data of the probe station over a PCI-GBIP interface with the computer.

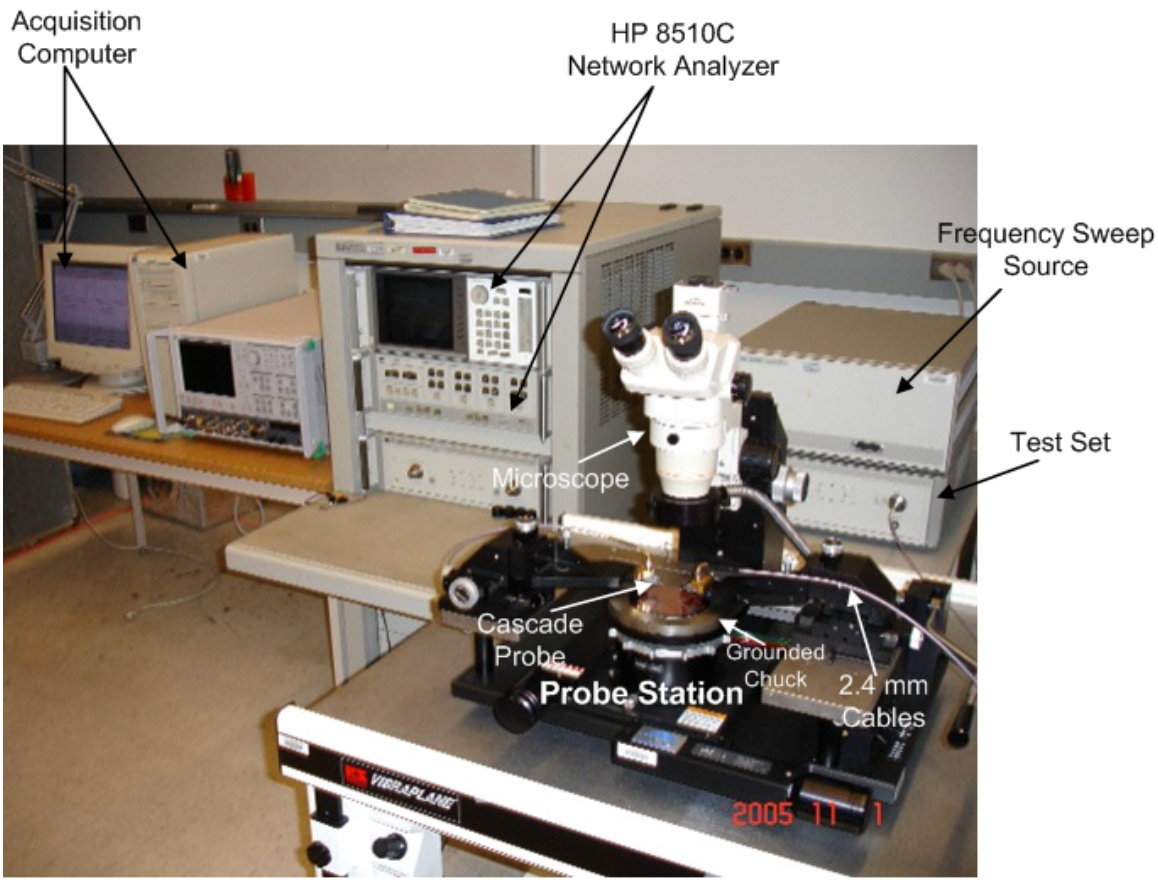

Figure B. 3. HP 8510C network analyzer with Cascade MicroTech probestation used for on-wafer probing of devices.

The MutiCal through, reflect, line (TRL) calibration algorithm by NISTCaL runs on the computer using measure data from the HP8510C to determine the calibration coefficient. These are then stored in the non-volatile storage of the network analyzer and uploaded to perform calibrated measurements of devices. The calibration standards for the TRL calibration are detailed in appendix B.2.

B.2 Calibration Standards

B.2.1 Bilayer Microstrip

For this work, microstrip TRL calibration standards were designed with an impedance of 50 ohms and fabricated on 50 mil thick duroid substrate. To ensure that the band of interest in fully covered, three delay lines were used along with an open calibration standard. An additional length equal to that of the THRU is added to each of the measured delay lines.

Name	Description
THRU	788 mil long through line
OPEN	394 mil long open circuited line ($\times 2$)
LINE	Delay lines with additional length indicated in mil

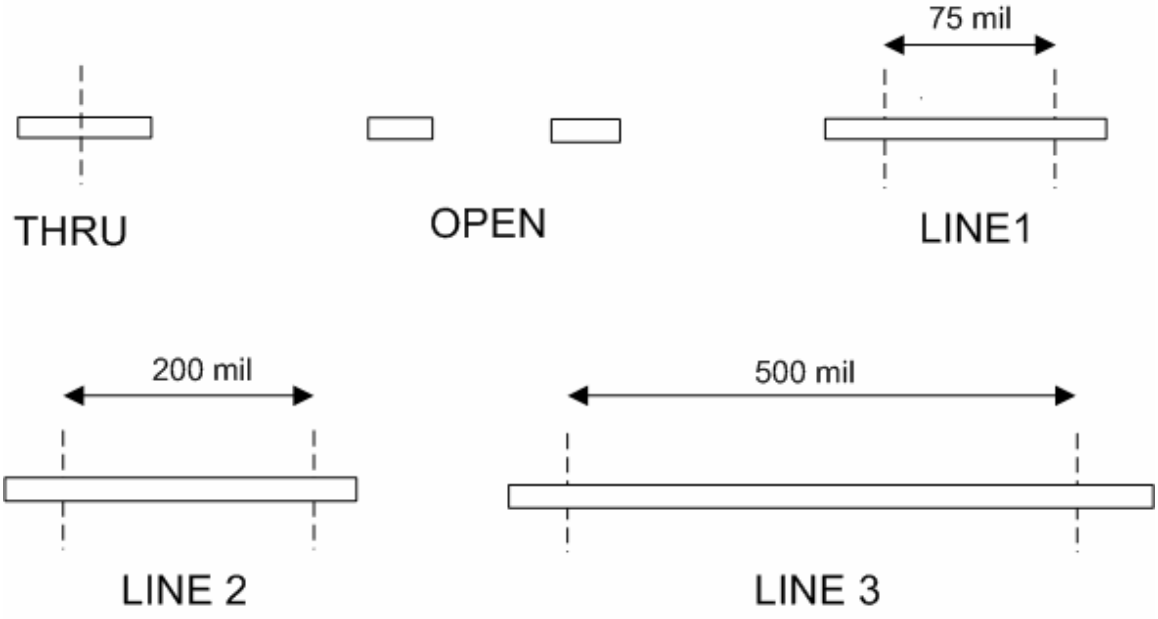

Figure B. 2. Microstrip TRL calibration standards for microstrip line on bilayer (duroid/air) substrate.

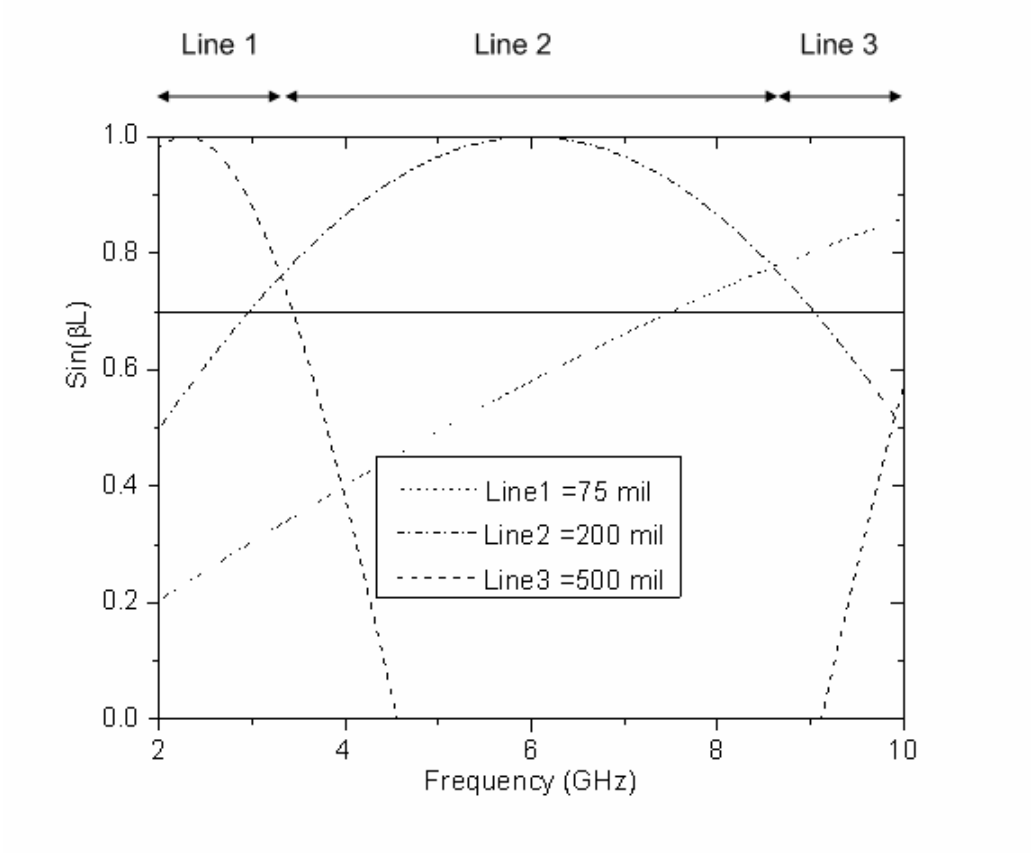

Figure B. 3. Electrical Length variation with frequency for three delay line calibration standards for microstip on bilayer substrate.

The design of the delay lines utilizes the plot shown in Figure B.3. Using an estimated effective dielectric constant of 6.71at approximately mid-band, the line are adjusted to yield a 90 degree electrical length from 45 to 135 of phase delay required by the TRL algorithm. Line1, 2 and 3 cover measurement in the frequency bands 1.5-3.3 GHz, 3.3-8.3 GHz and 8.30-10 GHz respectively.

B.2.2 Surface CPW line and Filter

The TRL calibration standards shown in Figure B.3 were used in the calibration of the on-wafer surface CPW lines and filters. Each standard is

designed with a width of 44 mils equivalent to that of the feed on 50 mil thick RT 6010LM duroid substrate. Three delay lines length are utilized to satisfy phase delay requirements for a frequency band of 2 to 30 GHz.

Name	Description
THRU	1600 μm long through line
OPEN	800 μm long open circuited line (×2)
LINE	Delay lines with additional length indicated in μm

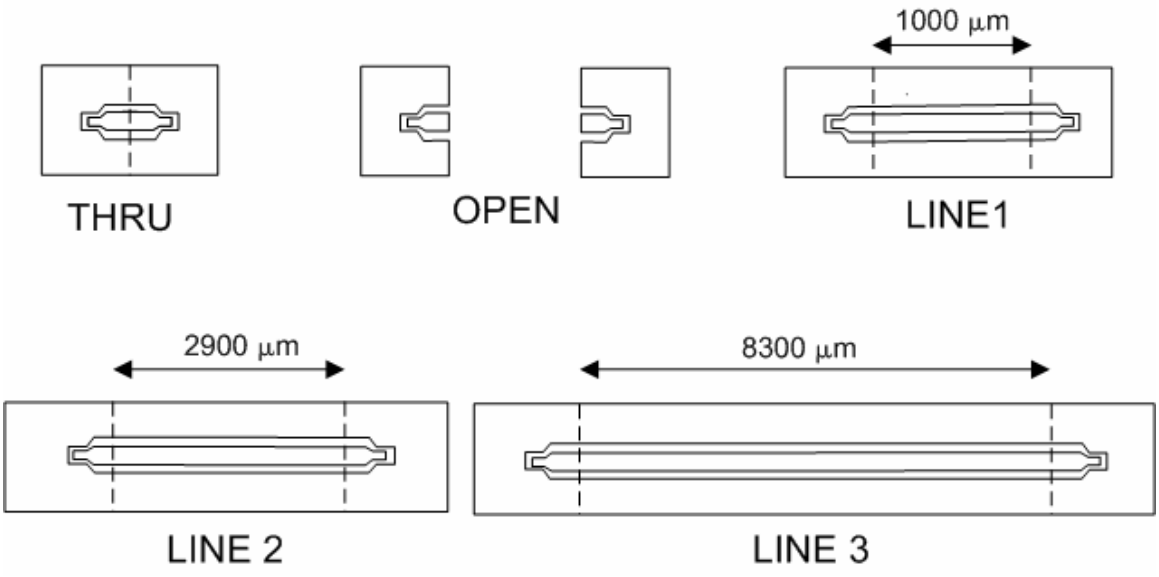

Figure B. 4. TRL calibration standards for on-wafer surface CPW (SCPW) line and filter.

The design of the delay lines utilizes the plot shown in Figure B.4. Using an estimated effective dielectric constant of 6.0 at approximately mid-band, the line are adjusted to yield a 90 degree electrical length from 45 to 135 of phase delay

required by the TRL algorithm. Line1, 2 and 3 cover measurement in the frequency bands 2.0-5.5 GHz, 5.5-15.75 GHz and 15.75-30 GHz respectively.

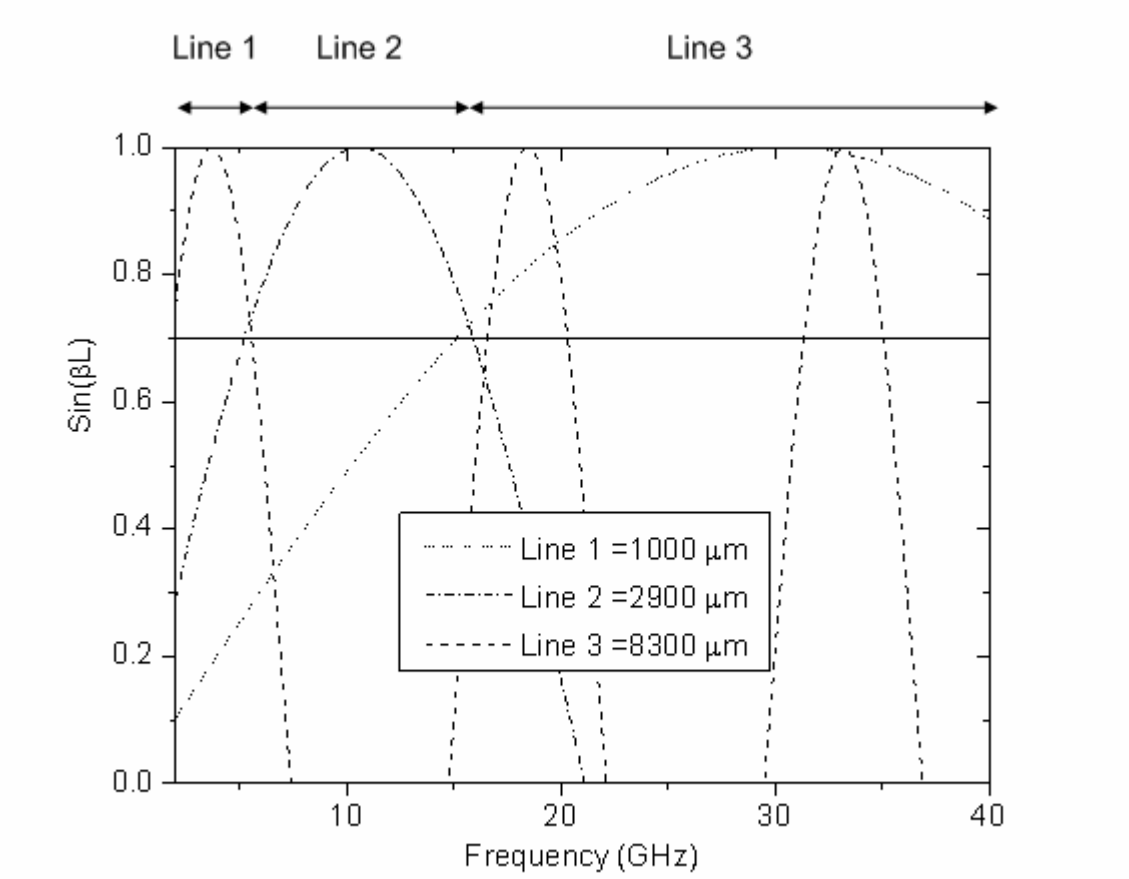

Figure B. 5. Electrical Length variation with frequency for three delay line calibration standards.

B.2.3. Embedded and Partially Embedded CPW line and Filter

The TRL calibration standards shown in Figure B.5 were used in the calibration of the on-wafer surface CPW lines and filters. Each standard is designed with a 50 ohm impedance on full thickness high resistivity silicon. Three

delay lines length are utilized to satisfy phase delay requirements for a frequency band of 2 to 40 GHz.

Name	Description
THRU	1600 μm long through line
OPEN	800 μm long open circuited line (×2)
LINE	Delay lines with additional length indicated in μm

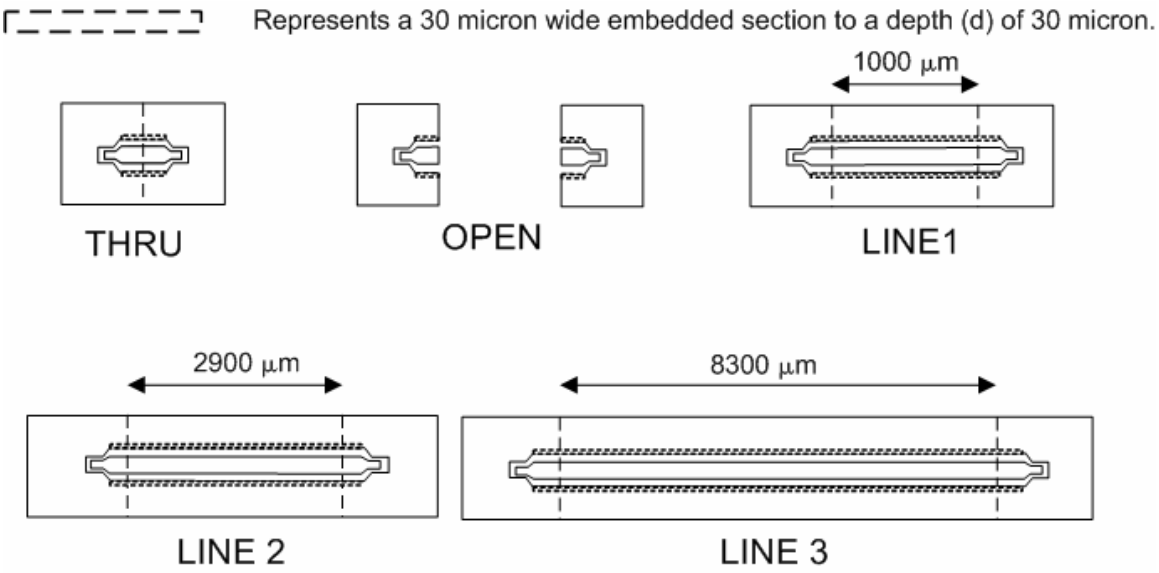

Figure B. 6. TRL calibration standards for on-wafer Partially Embedded and Embedded CPW line and filter.

The design of the delay lines utilizes the plot shown in Figure B.6. Using an estimated effective dielectric constant of 6.2 at approximately mid-band, the line are adjusted to yield a 90 degree electrical length from 45 to 135 of phase delay required by the TRL algorithm. Line1,2 and 3 cover measurement in the frequency bands 2-5.5 GHz, 5.5-15.5 GHz and 15.5-40 GHz respectively.

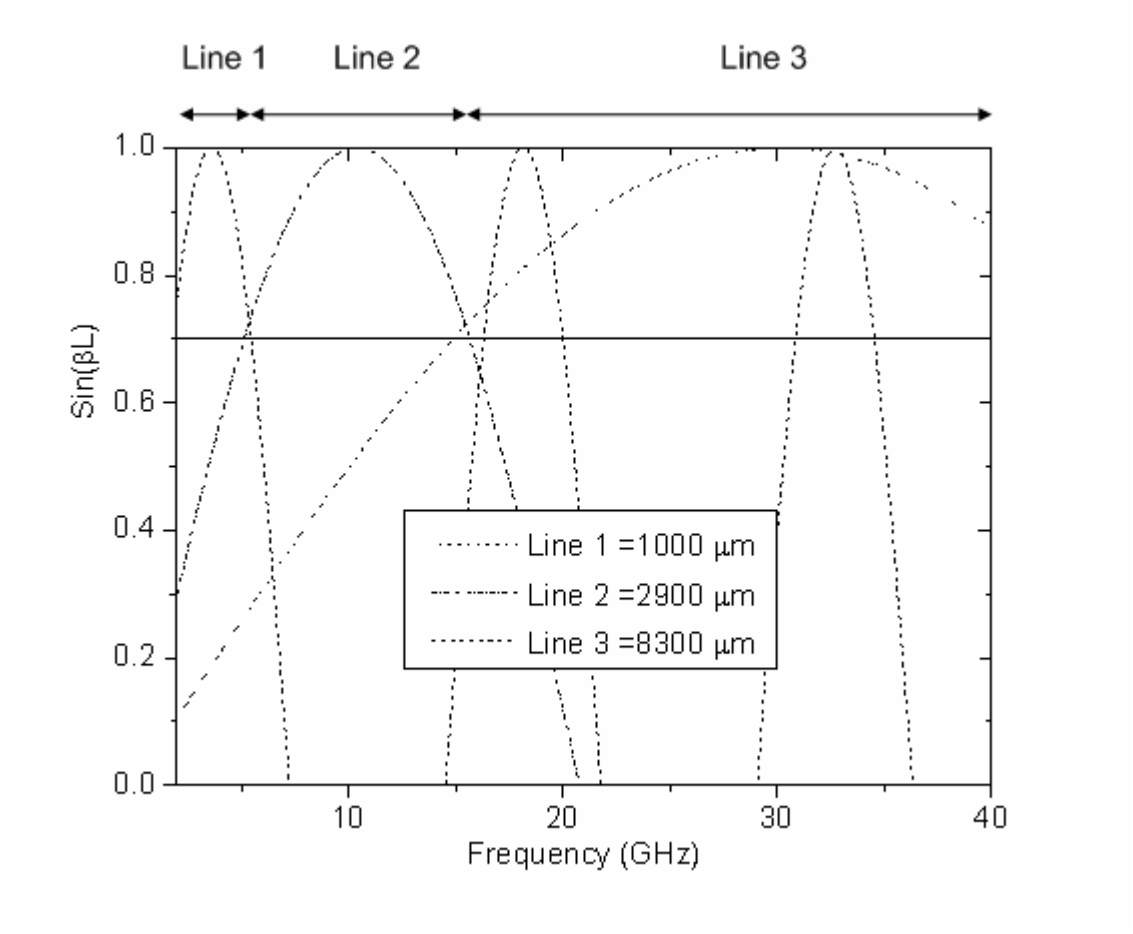

Figure B. 7. Electrical Length variation with frequency for three delay line calibration standards.

B3. Effective Dielectric Constant Extraction

The effective dielectric constant of a structure can be obtained using calibration softwares such as MultiCal. An alternative approach used utilizes the measured transmission scattering parameter (S_{12} and S_{21}) phase of the structure to determine the effective dielectric constant (ε_e) as a function of frequency. The phase can be expressed as:

$$\theta(radians) = \beta\ell = \frac{2\pi.\ell}{\lambda_g} = \frac{2\pi.f.\ell.\sqrt{\varepsilon_e}}{c}$$

Taking the derivative of θ with respect to frequency (*f*) and converting to degrees gives:

$$\frac{d\theta}{df}(\deg rees / Hz) = \frac{360.\ell.\sqrt{\varepsilon_e}}{c}$$

Then solving for the effective dielectric constant (ε_e) with respect to frequency gives:

$$\varepsilon_e(f) = \left[\frac{d\theta}{df}\left(\frac{c}{360.\ell}\right)\right]^2$$

The phase change over the band can be used to calculate a constant static effective dielectric constant ($\varepsilon_e(\Delta f)$) for the substrate.

$$\varepsilon_e(\Delta f) = \left[\frac{\Delta\theta}{\Delta f}\frac{c}{360.\ell}\right]^2$$

APPENDIX C: SIMULATION SETUP

C.1. Embedded and Surface CPW and Filter

The geometries used to simulate the embedded, partially embedded and surface filters as well as the embedded and surface low impedance CPW lines are shown in Figure C 1and Figure C 2. These geometries are used as part of the input to the three-dimensional full-wave electromagnetic solver [1]. The filter structures simulated are shown in Figure 3.14 to Figure 3.16 and the dimensions listed in Table 3.5 to Table 3.7. The CPW dimensions are shown in Table 3.1. Conductors are embedded in the substrate using a subtraction operation. The substrate thickness used in all the simulations was 0.525 mm with a port size of 1.6 mm (width) by 2.0 mm (height). A quarter of the height of the port is below the high resistivity silicon wafer substrate used in the simulations. The port is extended below the substrate to minimize the coupling of fields to the port instead of the conductors. The substrate properties used are shown in Table C 1. To provide appropriate boundary condition for the full-wave simulation, the air box used in all of the simulations is specified as a radiation boundary.

Material	Location	Dielectric constant	Conductivity (S/m)	Tan δ
Copper	Surface and embedded conductors	1	5.8E7	0
High resistivity Silicon	Substrate	11.9	0.05	0.008
Air	Boundary Box	1	0	0

Table C 1. Properties of different materials used in simulation of embedded and surface CPWs and filters.

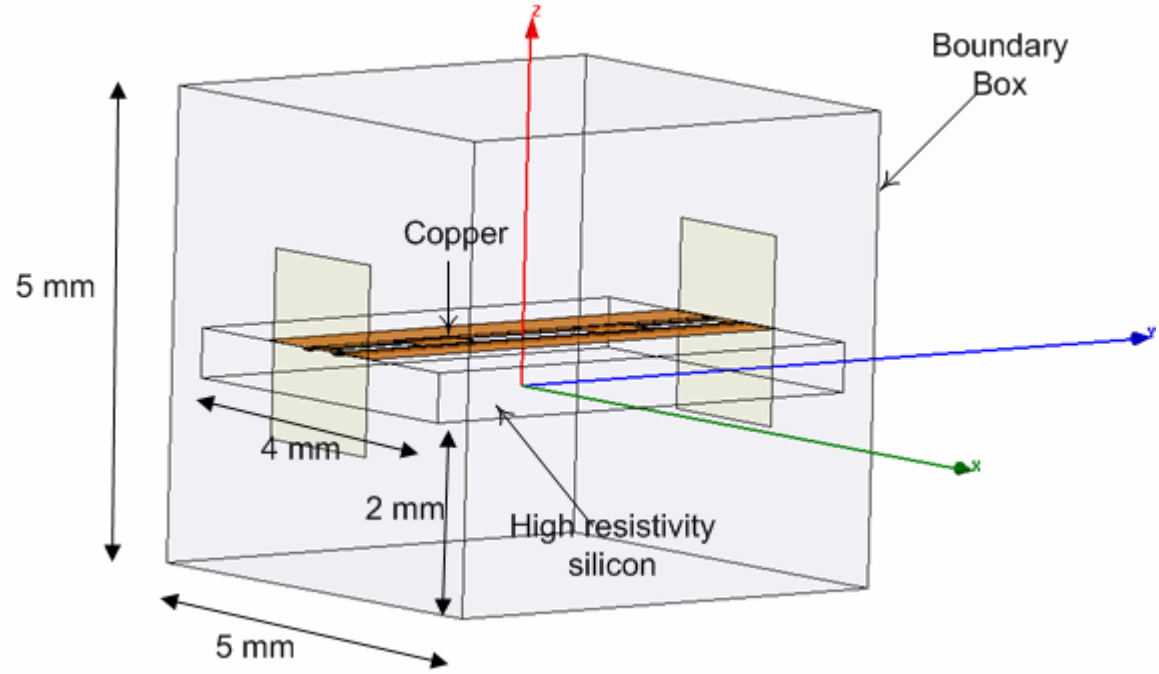

Figure C 1. Three dimensional view of electromagnetic simulation setup for a partially embedded filter. The surface and embedded filter were also setup using a similar approach.

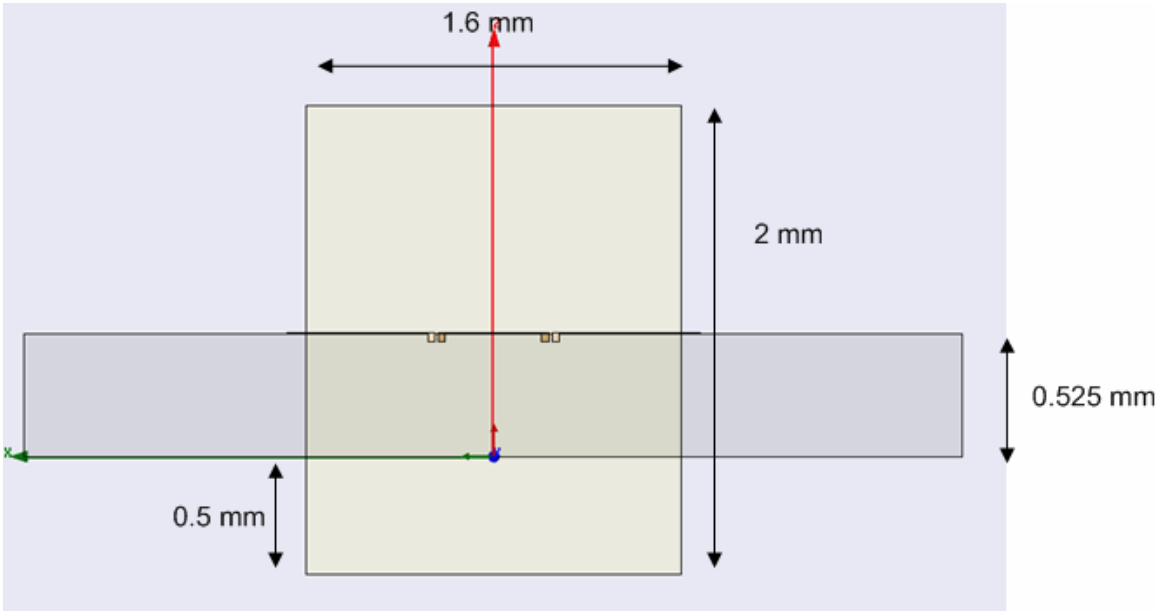

Figure C 2. Side view of picture of geometry and port used in electromagnetic simulation.

C.3. Bilayer Microstrip Filter

The geometries used to simulate the 12 and 6 slot bilayer microstrip photonic bandgap filters are shown in Figure C 3and Figure C 4. These geometrical dimensions form part of the input to the three-dimensional full-wave electromagnetic solver [1]. The dimension of the different bilayer microstrip filters simulated is located in Table 3.12 and Table 3.13. The electromagnetic field of the structure is such that a magnetic (perfect-H) boundary wall is used on one side of the boundary box to replicate the fields hence reducing the computation time by a factor of 2. A radiation boundary is used to provide appropriate boundary conditions on the other sides. The port size for the simulations is 500 mil (width) and 300 mil (height) but since a magnetic wall is used the width is reduced by a factor of 2. The properties of the materials used in the simulations are shown in Table C 2. The thickness of the copper used in all of the simulations is 1.4 mils.

Material	Location	Dielectric constant	Conductivity (S/m)	Tan δ
Copper	Signal and ground conductors	1	5.8E7	0
Duroid RT6010LM	Substrate	0	0	0.0023
Air	Boundary Box and substrate	1	0	0

Table C 2. Properties of different materials used in simulation of embedded and surface CPWs and filters.

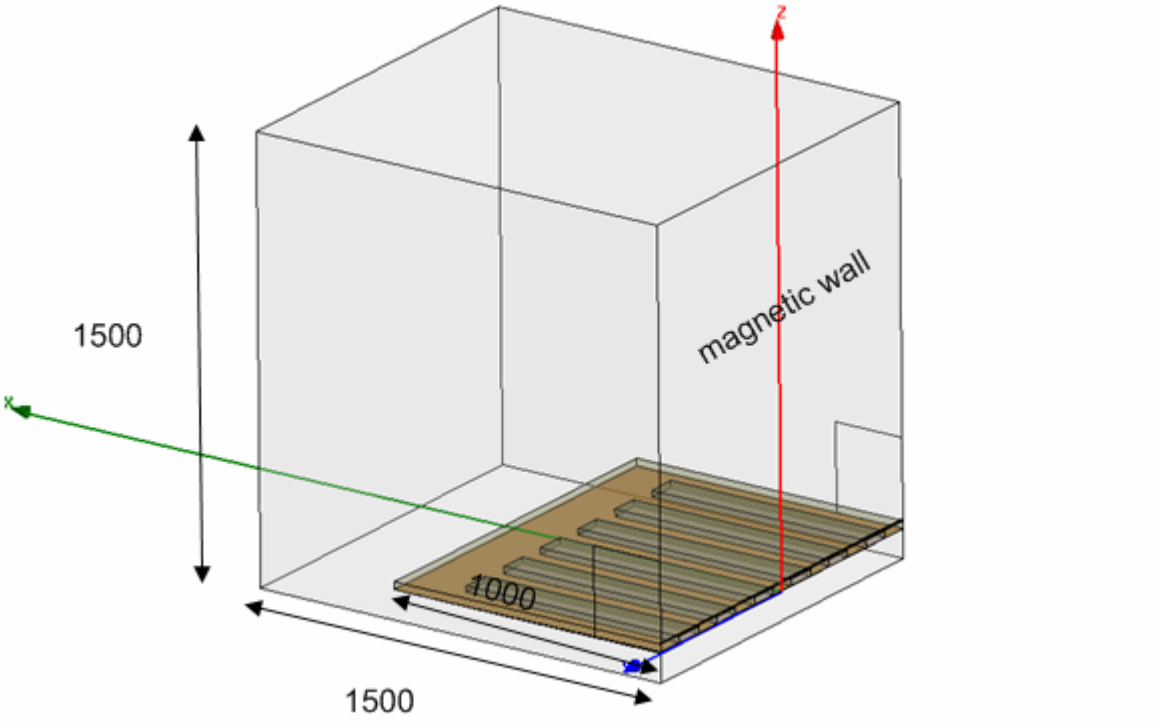

Figure C 3. Three dimensional view of electromagnetic simulation setup for a bilayer filter.

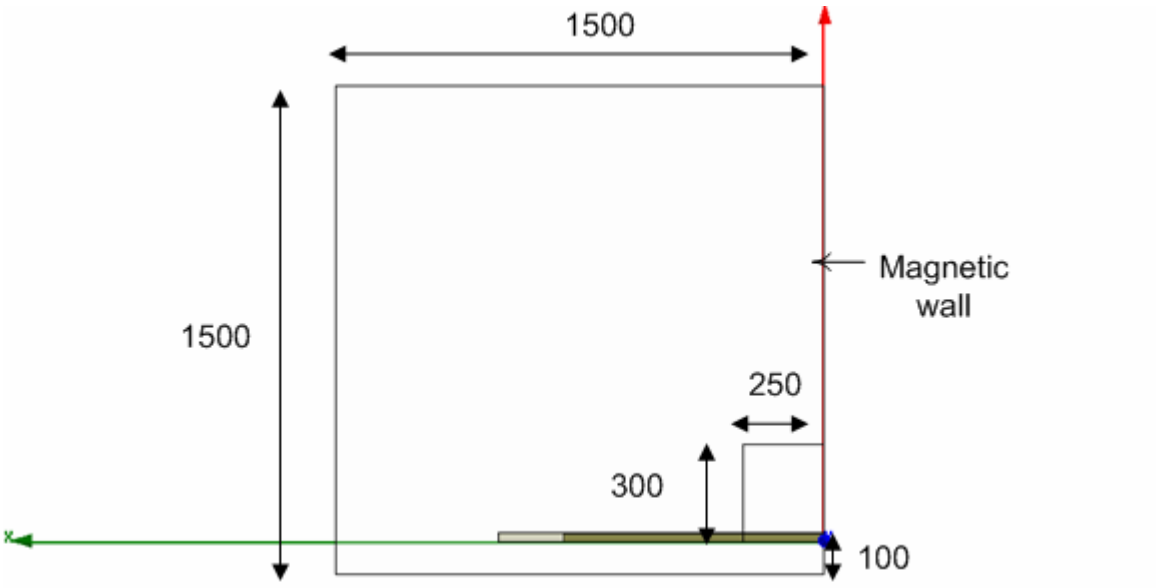

Figure C 4. Cross-sectional picture of electromagnetic simulation setup of bilayer filter.

Appendix References

[1]. HFSS, ver. 7- ver. 9.1, Ansoft Corporation, Pittsburg, PA, 2003.