Attia, John Okyere. “Transistor Circuits.”
Electronics and Circuit Analysis using MATLAB.
Ed. John Okyere Attia
Boca Raton: CRC Press LLC, 1999

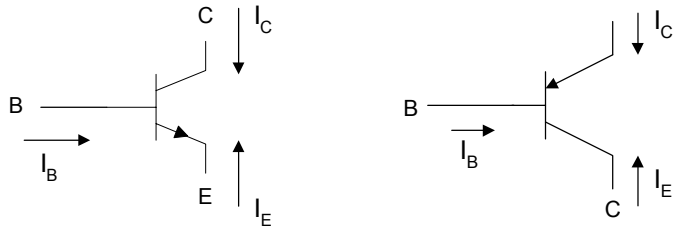
CHAPTER TWELVE

TRANSISTOR CIRCUITS

In this chapter, MATLAB will be used to solve problems involving metal-oxide semiconductor field effect and bipolar junction transistors. The general topics to be discussed in this chapter are dc model of BJT and MOSFET, biasing of discrete and integrated circuits, and frequency response of amplifiers.

12.1 BIPOLAR JUNCTION TRANSISTORS

Bipolar junction transistor (BJT) consists of two pn junctions connected back-to-back. The operation of the BJT depends on the flow of both majority and minority carriers. There are two types of BJT: npn and pnp transistors. The electronic symbols of the two types of transistors are shown in Figure 12.1.



(a) (b)

Figure 12.1 (a) NPN transistor (b) PNP Transistor

The dc behavior of the BJT can be described by the Ebers-Moll Model. The equations for the model are

$$I_F = I_{ES}\left[\exp\left(\frac{V_{BE}}{V_T}\right) - 1\right] \tag{12.1}$$

$$I_R = I_{CS}\left[\exp\left(\frac{V_{BC}}{V_T}\right) - 1\right] \tag{12.2}$$

and

$$I_C = \alpha_F I_F - I_R \tag{12.3}$$

$$I_E = -I_F + \alpha_R I_R \tag{12.4}$$

and

$$I_B = \left(1 - \alpha_F\right) I_F + \left(1 - \alpha_R\right) I_R \tag{12.5}$$

where

I_{ES} and I_{CS} are the base-emitter and base-collector saturation currents, respectively

α_R is large signal reverse current gain of a common-base configuration

α_F is large signal forward current gain of the common-base configuration.

and

$$V_T = \frac{kT}{q} \tag{12.6}$$

where

k is the Boltzmann's constant (k = 1.381 x 10^{-23} V.C/^{o} K),
T is the absolute temperature in degrees Kelvin, and
q is the charge of an electron (q = 1.602 x 10^{-19} C).

The forward and reverse current gains are related by the expression

$$\alpha_R I_{CS} = \alpha_F I_{ES} = I_S \tag{12.7}$$

where

I_S is the BJT transport saturation current.

The parameters α_R and α_F are influenced by impurity concentrations and junction depths. The saturation current, I_S, can be expressed as

$$I_S = J_S A \tag{12.8}$$

where

A is the area of the emitter and

J_S is the transport saturation current density, and it can be further expressed as

$$J_S = \frac{qD_n n_i^2}{Q_B} \tag{12.9}$$

where

D_n is the average effective electron diffusion constant

n_i is the intrinsic carrier concentration in silicon (n_i = 1.45 x 10^{10} atoms / cm^3 at 300° K)

Q_B is the number of doping atoms in the base per unit area.

The dc equivalent circuit of the BJT is based upon the Ebers-Moll model. The model is shown in Figure 12.2. The current sources $\alpha_R I_R$ indicate the interaction between the base-emitter and base-collector junctions due to the narrow base region.

In the case of a pnp transistor, the directions of the diodes in Figure 12.2 are reversed. In addition, the voltage polarities of Equations (12.1) and (12.2) are reversed. The resulting Ebers-Moll equations for pnp transistors are

$$I_E = I_{ES}\left[\exp\left(\frac{V_{EB}}{V_T}\right) - 1\right] - \alpha_R I_{CS}\left[\exp\left(\frac{V_{CB}}{V_T}\right) - 1\right] \tag{12.10}$$

$$I_C = -\alpha_F I_{ES}\left[\exp\left(\frac{V_{EB}}{V_T}\right) - 1\right] + I_{CS}\left[\exp\left(\frac{V_{CB}}{V_T}\right) - 1\right] \tag{12.11}$$

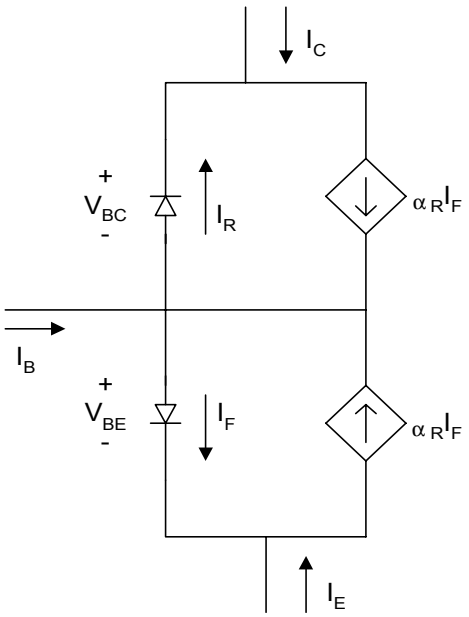


Figure 12.2 Ebers-Moll Static Model for an NPN transistor (Injection Version)

The voltages at the base-emitter and base-collector junctions will define the regions of operation. The four regions of operations are forward-active, reverse-active, saturation and cut-off. Figure 12.3 shows the regions of operation based on the polarities of the base-emitter and base collector junctions.

Forward-Active Region

The forward-active region corresponds to forward biasing the emitter-base junction and reverse biasing the base-collector junction. It is the normal operational region of transistors employed for amplifications. If $V_{BE} > 0.5$ V and $V_{BC} < 0.3$V, then equations (12.1) to (12.4) and (12.6) can be rewritten as

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) \tag{12.12}$$

$$I_E = -\frac{I_S}{\alpha_F}\exp\left(\frac{V_{BE}}{V_T}\right) \tag{12.13}$$

From Figure 12.1,

$$I_B = -\left(I_C + I_E\right) \tag{12.14}$$

Substituting Equations (12.12) and (12.13) into (12.14), we have

$$I_B = I_S\frac{\left(1-\alpha_F\right)}{\alpha_F}\exp\left(\frac{V_{BE}}{V_T}\right) \tag{12.15}$$

$$= \frac{I_S}{\beta_F}\exp\left(\frac{V_{BE}}{V_T}\right) \tag{12.16}$$

where

β_F = large signal forward current gain of common-emitter configuration

$$\beta_F = \frac{\alpha_F}{1-\alpha_F} \tag{12.17}$$

From Equations (12.12) and (12.16), we have

$$I_C = \beta_F I_B \tag{12.18}$$

We can also define, β_R, the large signal reverse current gain of the common-emitter configuration as

$$\beta_R = \frac{\alpha_R}{1-\alpha_R} \tag{12.19}$$

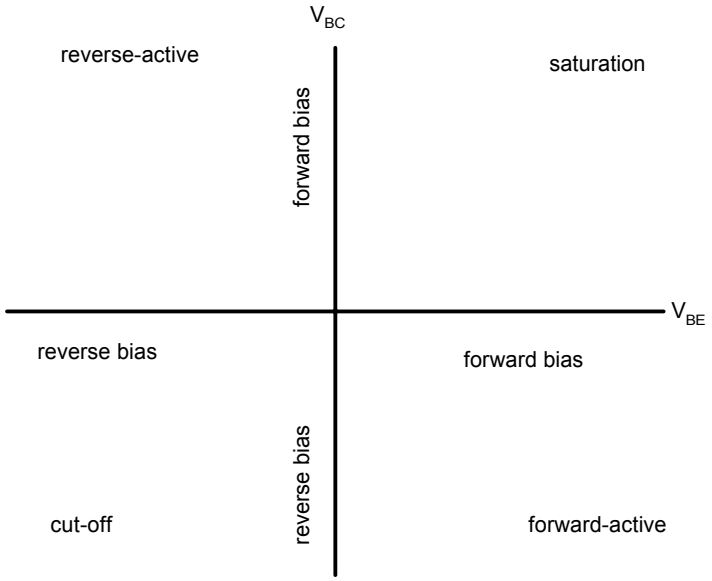


Figure 12.3 Regions of Operation for a BJT as Defined by the Bias of V_{BE} and V_{BC}

Reverse-Active Region

The reverse-active region corresponds to reverse biasing the emitter-base junction and forward biasing the base-collector junction. The Ebers-Moll model in the reverse-active region ($V_{BC} >$ 0.5V and $V_{BE} <$ 0.3V) simplifies to

$$I_E = I_S\left[\frac{V_{BC}}{V_T}\right] \tag{12.20}$$

$$I_B = \frac{I_S}{\beta_R}\exp\left[\frac{V_{BC}}{V_T}\right] \tag{12.21}$$

Thus,

$$I_E = \beta_R I_B \tag{12.22}$$

The reverse-active region is seldom used.

Saturation and Cut-off Regions

The saturation region corresponds to forward biasing both base-emitter and base-collector junctions. A switching transistor will be in the saturation region when the device is in the conducting or "ON" state.

The cut-off region corresponds to reverse biasing the base-emitter and base-collector junctions. The collector and base currents are very small compared to those that flow when transistors are in the active-forward and saturation regions. In most applications, it is adequate to assume that $I_C = I_B = I_E = 0$ when a BJT is in the cut-off region. A switching transistor will be in the cut-off region when the device is not conducting or in the "OFF" state.

Example 12.1

Assume that a BJT has an emitter area of 5.0 mil^2, $\beta_F = 120$, $\beta_R = 0.3$ transport current density, $J_S = 2 * 10^{-10}$ $\mu A / mil^2$ and T = 300°K. Plot I_E versus V_{BE} for V_{BC} = -1V. Assume 0 < V_{BE} < 0.7 V.

Solution

From Equations (12.1), (12.2) and (12.4), we can write the following MATLAB program.

MATLAB Script

```
%Input characteristics of a BJT
diary ex12_1.dat
diary on
k=1.381e-23; temp=300; q=1.602e-19;
cur_den=2e-10; area=5.0; beta_f=120; beta_r=0.3;
vt=k*temp/q; is=cur_den*area;
alpha_f=beta_f/(1+beta_f);
alpha_r = beta_r/(1+beta_r);
ies=is/alpha_f;
vbe=0.3:0.01:0.65;
ics=is/alpha_r;
m=length(vbe)
for i = 1:m
 ifr(i) = ies*exp((vbe(i)/vt)-1);
```

```
 ir1(i) = ics*exp((-1.0/vt)-1);
 ie1(i) = abs(-ifr(i) + alpha_r*ir1(i));
end
plot(vbe,ie1)
title('Input characteristics')
xlabel('Base-emitter voltage, V')
ylabel('Emitter current, A')
```

Figure 12.4 shows the input characteristics.

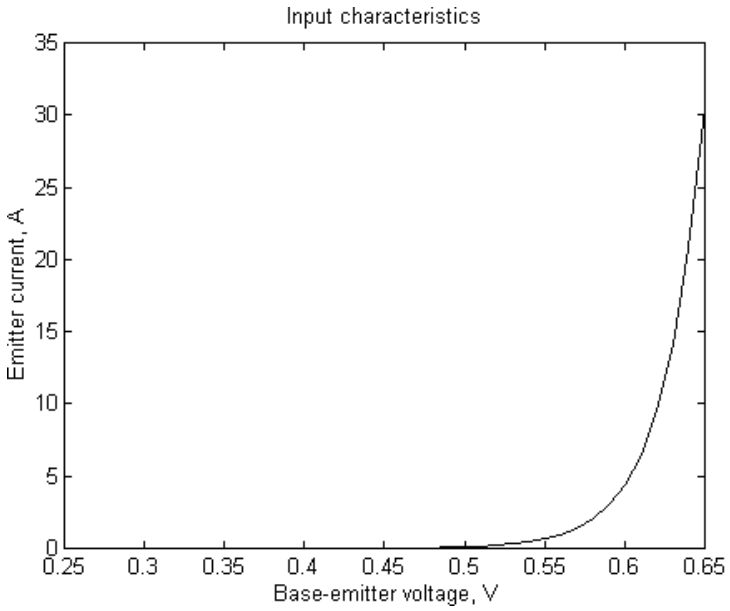


Figure 12.4 Input Characteristics of a Bipolar Junction Transistor

Experimental studies indicate that the collector current of the BJT in the forward-active region increases linearly with the voltage between the collector-emitter V_{CE}. Equation 12.12 can be modified as

$$I_C \cong I_S \exp\left[\frac{V_{BE}}{V_T}\right]\left(1+\frac{V_{CE}}{V_{AF}}\right) \tag{12.23}$$

where

V_{AF} is a constant dependent on the fabrication process.

Example 12.2

For an npn transistor with emitter area of 5.5 mil^2, $\alpha_F = 0.98$, $\alpha_R = 0.35$, $V_{AF} = 250\,V$ and transport current density is $2.0\,x\,10^{-9}\ \mu A / mil^2$. Use MATLAB to plot the output characteristic for V_{BE} = 0.65 V. Neglect the effect of V_{AF} on the output current I_C. Assume a temperature of 300 ^{o}K.

Solution

MATLAB Script

```
%output characteristic of an npn transistor
%
diary ex12_2.dat
k=1.381e-23; temp=300; q=1.602e-19;
cur_den=2.0e-15; area=5.5; alpha_f=0.98;
alpha_r=0.35; vt=k*temp/q; is=cur_den*area;
ies=is/alpha_f; ics=is/alpha_r;
vbe= [0.65];
vce=[0 0.07 0.1 0.2 0.3 0.4 0.5 0.6 0.7 1 2 4 6];
n=length(vbe);
m=length(vce);
for i=1:n
  for j=1:m
    ifr(i,j)= ies*exp((vbe(i)/vt) - 1);
    vbc(j) = vbe(i) - vce(j);
    ir(i,j) = ics*exp((vbc(j)/vt) - 1);
    ic(i,j) = alpha_f*ifr(i,j) - ir(i,j);
  end
end
ic1 = ic(1,:);
plot(vce, ic1,'w')
title('Output Characteristic')
xlabel('Collector-emitter Voltage, V')
ylabel('Collector current, A')
text(3,3.1e-4, 'Vbe = 0.65 V')
axis([0,6,0,4e-4])
```

Figure 12.5 shows the output characteristic.

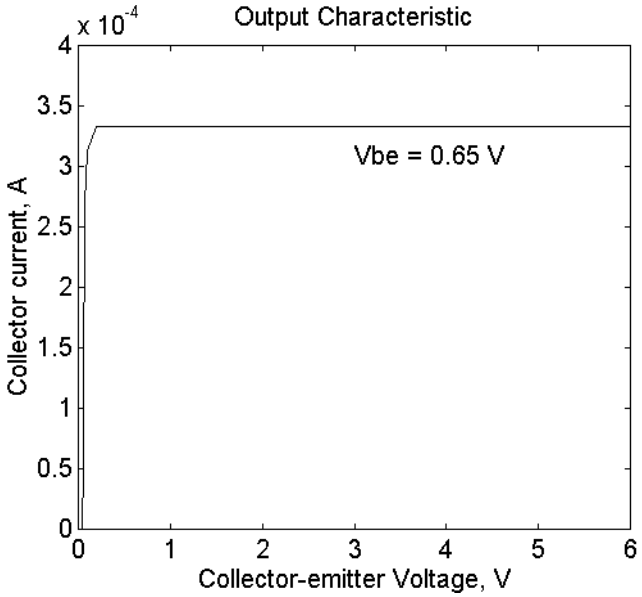
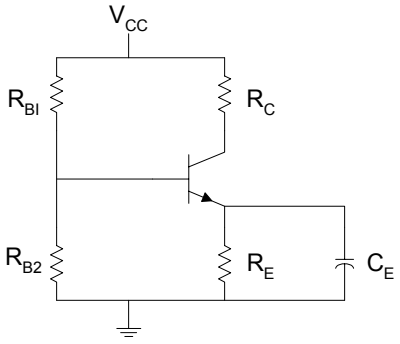


Figure 12.5 Output Characteristic on an NPN Transistor

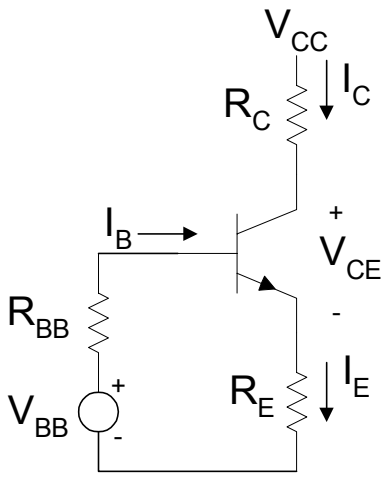
12.2 BIASING BJT DISCRETE CIRCUITS

12.2.1 Self-bias circuit

One of the most frequently used biasing circuits for discrete transistor circuits is the self-bias of the emitter-bias circuit shown in Figure 12.6.



(a)



(b)

Figure 12.6 (a) Self-Bias Circuit (b) DC Equivalent Circuit of (a)

The emitter resistance, R_E, provides stabilization of the bias point. If V_{BB} and R_B are the Thevenin equivalent parameters for the base bias circuit, then

$$V_{BB} = \frac{V_{CC} R_{B2}}{R_{B1} + R_{B2}} \tag{12.24}$$

$$R_B = R_{B1} \| R_{B2} \tag{12.25}$$

Using Kirchoff's Voltage Law for the base circuit, we have

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E \tag{12.26}$$

Using Equation (12.18) and Figure 12.6b, we have

$$I_E = I_B + I_C = I_B + \beta_F I_B = (\beta_F + 1) I_B \tag{12.27}$$

Substituting Equations (12.18) and (12.27) into (12.26), we have

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (\beta_F + 1)R_E} \tag{12.28}$$

or

$$I_C = \frac{V_{BB} - V_{BE}}{\frac{R_B}{\beta_F} + \frac{(\beta_F + 1)}{\beta_F} R_E} \tag{12.29}$$

Applying KVL at the output loop of Figure 12.6b gives

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \tag{12.30}$$

$$= V_{CC} - I_C\left(R_C + R_E / \alpha_F\right) \tag{12.31}$$

12.2.2 Bias stability

Equation (12.30) gives the parameters that influence the bias current I_C. The voltage V_{BB} depends on the supply voltage V_{CC}. In some cases, V_{CC} would vary with I_C, but by using a stabilized voltage supply we can ignore the changes in V_{CC}, and hence V_{BB}. The changes in the resistances R_{BB} and R_E are negligible. There is a variation of β_F with respect to changes in I_C. A typical plot of β_F versus I_C is shown in Figure 12.7.

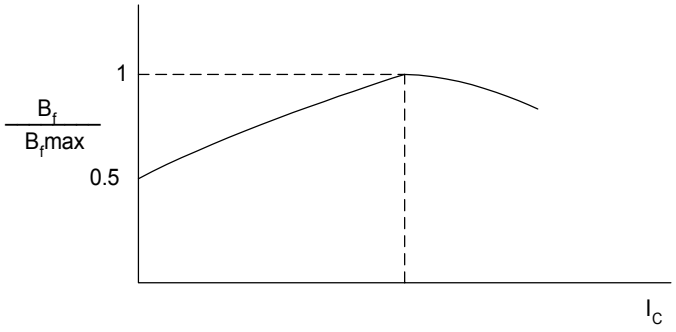


Figure 12.7 Normalized plot of β_F as a Function of Collector Current

Temperature changes cause two transistor parameters to change. These are (1) base-emitter voltage (V_{BE}) and (2) collector leakage current between the base and collector (I_{CBO}). The variation on V_{BE} with temperature is similar to the changes of the pn junction diode voltage with temperature. For silicon transistors, the voltage V_{BE} varies almost linearly with temperature as

$$\Delta V_{BE} \cong -2\left(T_2 - T_1\right) \qquad mV \tag{12.32}$$

where

T_1 and T_2 are in degrees Celsius.

The collector-to-base leakage current, I_{CBO}, approximately doubles every 10^o temperature rise. As discussed in Section 9.1, if I_{CBO1} is the reverse leakage current at room temperature (25 ^{o}C), then

$$I_{CBO2} = 2^{\left(T_2 - 25^O C/10\right)} I_{CBO1}$$

and

$$\Delta I_{CBO} = I_{CBO2} - I_{CBO1} = I$$

$$= I_{CBO}\left[2^{\left(T_2 - 25^O C/10\right)} - 1\right] \tag{12.33}$$

Since the variations in I_{CBO} and V_{BE} are temperature dependent, but changes in V_{CC} and β_F are due to factors other than temperature, the information about the changes in V_{CC} and β_F must be specified.

From the above discussion, the collector current is a function of four variables: $V_{BE}, I_{CBO}, \beta_F, V_{CC}$. The change in collector current can be obtained using partial derivatives. For small parameter changes, a change in collector current is given as

$$\Delta I_C = \frac{\partial I_C}{\partial V_{BE}}\Delta V_{BE} + \frac{\partial I_C}{\partial V_{CBO}}\Delta I_{CBO} + \frac{\partial I_C}{\partial \beta_F}\Delta \beta_F + \frac{\partial I_C}{\partial V_{CC}}\Delta V_{CC} \tag{12.34}$$

The stability factors can be defined for the four variables as

$$S_\beta = \frac{\partial I_C}{\partial \beta_F} \cong \frac{\Delta I_C}{\Delta \beta_F}$$

$$S_v = \frac{\partial I_C}{\partial V_{BE}} \cong \frac{\Delta I_C}{\Delta V_{BE}}$$

$$S_I = \frac{\partial I_C}{\partial I_{CBO}} \cong \frac{\Delta I_C}{\Delta I_{CBO}}$$

and

$$S_{VCC} = \frac{\partial I_C}{\partial V_{CC}} \cong \frac{\Delta I_C}{\Delta V_{CC}} \tag{12.35}$$

Using the stability factors, Equation (12.34) becomes

$$\Delta I_C = S_V \Delta V_{BE} + S_\beta \Delta \beta_F + S_I \Delta I_{CBO} + S_{VCC} \Delta V_{CC} \tag{12.36}$$

From Equation (12.30),

$$S_V = \frac{dI_C}{dV_{BE}} = -\frac{1}{R_B / \beta_F + R_E \left(\beta_F + 1 / \beta_F \right)} \tag{12.37}$$

From Equation (12.31),

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E / \alpha_F} \tag{12.38}$$

Thus, the stability factor S_{VCC} is given as

$$S_{VCC} = \frac{dI_C}{dV_{CC}} = \frac{1}{R_C + R_E / \alpha_F} \tag{12.39}$$

To obtain the stability factor S_I, an expression for I_C involving I_{CBO} needs to be derived. The derivation is assisted by referring to Figure 12.8.

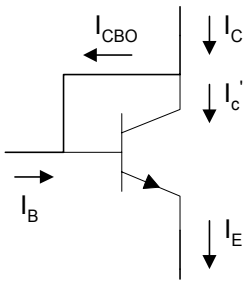


Figure 12.8 Current in Transistor including I_{CBO}

The current

$$I_C = I_C^{'} + I_{CBO} \tag{12.40}$$

and

$$I_C^{'} = \beta_F \left(I_B + I_{CBO} \right) \tag{12.41}$$

From Equations (12.40) and (12.41), we have

$$I_C = \beta_F I_B + \left(\beta_F + 1 \right) I_{CBO} \tag{12.42}$$

Assuming that $\beta_F + 1 \cong \beta_F$, then

$$I_C = \beta_F I_B + \beta_F I_{CBO} \tag{12.43}$$

so

$$I_B = \frac{I_C}{\beta_F} - I_{CBO} \tag{12.44}$$

The loop equation of the base-emitter circuit of Figure 12.6(b) gives

$$\begin{aligned} V_{BB} - V_{BE} &= I_B R_{BB} + R_E \left(I_B + I_C \right) \\ &= I_B \left(R_{BB} + R_E \right) + R_E I_C \end{aligned} \tag{12.45}$$

Assuming that $\beta_F + 1 \cong \beta_F$ and substituting Equation (12.44) into (12.45), we get

$$V_{BB} - V_{BE} = \left(R_{BB} + R_E\right)\left(\frac{I_C}{\beta_F} - I_{CBO}\right) + I_C R_E \tag{12.46}$$

Solving for I_C, we have

$$I_C = \frac{V_{BB} - V_{BE} + \left(R_{BB} + R_E\right) I_{CBO}}{\left(R_{BB} + R_E\right)/\beta_F + R_E} \tag{12.47}$$

Taking the partial derivative,

$$S_I = \frac{\partial I_C}{\partial I_{CBO}} = \frac{R_{BB} + R_E}{\left(R_{BB} + R_E\right)/\beta_F + R_E} \tag{12.48}$$

The stability factor involving β_F and S_β can also be found by taking the partial derivative of Equation (12.47). Thus,

$$S_\beta = \frac{\partial I_C}{\partial \beta} = \frac{\left(R_B + R_E\right)\left[V_{BB} - V_{BE} + \left(R_B + R_E\right) I_{CBO}\right]}{\left(R_B + R_E + \beta R_E\right)^2} \tag{12.49}$$

The following example shows the use of MATLAB for finding the changes in the quiescent point of a transistor due variations in temperature, base-to-emitter voltage and common emitter current gain.

Example 12.3

The self-bias circuit of Figure 12.6 has the following element values: $R_{B1} = 50\ K$, $R_{B2} = 10\ K$, $R_E = 1.2\ K$, $R_C = 6.8\ K$, β_F varies from 150 to 200 and V_{CC} is 10 ± 0.05 V. I_{CBO} is 1 μA at 25 ^{0}C. Calculate the collector current at 25 ^{o}C and plot the change in collector current for temperatures between 25 and 100 ^{o}C. Assume V_{BE} and β_F at 25 ^{o}C are 0.7 V and 150, respectively.

Solution

Equations (12.25), (12.26), and (12.30) can be used to calculate the collector current. At each temperature, the stability factors are calculated using Equations (12.37), (12.39), (12,48) and (12.49). The changes in V_{BE} and I_{CBO} with temperature are obtained using Equations (12.32) and (12.33), respectively. The change in I_C for each temperature is calculated using Equation (12.36).

MATLAB Script:

```
% Bias stability
%
rb1=50e3; rb2=10e3; re=1.2e3; rc=6.8e3;
vcc=10; vbe=0.7; icbo25=1e-6; beta=(150+200)/2;
vbb=vcc*rb2/(rb1+rb2);
rb=rb1*rb2/(rb1+rb2);
ic=beta*(vbb-vbe)/(rb+(beta+1)*re);

%stability factors are calculated
svbe=-beta/(rb+(beta+1)*re);
alpha=beta/(beta+1);
svcc=1/(rc + (re/alpha));
svicbo=(rb+re)/(re+(rb+re)/alpha);
sbeta=((rb+re)*(vbb-vbe+icbo25*(rb+re))/(rb+re+beta*re)^2);
% Calculate changes in Ic for various temperatures

t=25:1:100;
len_t = length(t);
dbeta = 50; dvcc=0.1;
for i=1:len_t
    dvbe(i)= -2e-3*(t(i)-25);
    dicbo(i)=icbo25*(2^((t(i)-25)/10)-1);
    dic(i)=svbe*dvbe(i)+svcc*dvcc...
                +svicbo+dicbo(i)+sbeta*dbeta;
end
plot(t,dicbo)
title('Change in collector current vs. temperature')
xlabel('Temperature, degree C')
ylabel('Change in collector current, A')
```

Figure 12.9 shows I_C versus temperature.

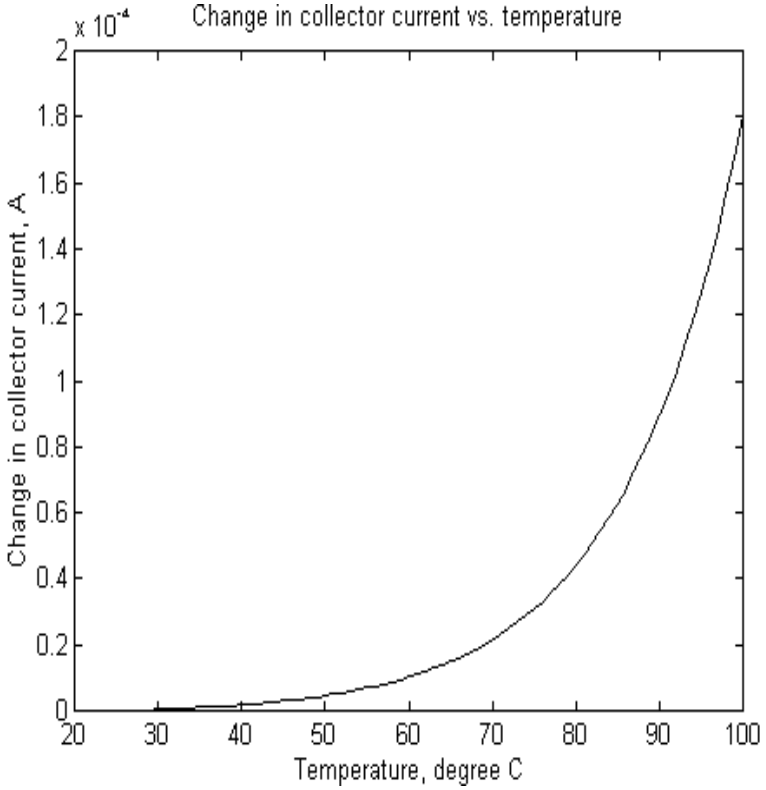


Figure 12.9 I_C versus Temperature

12.3 INTEGRATED CIRCUIT BIASING

Biasing schemes for discrete electronic circuits are not suitable for integrated circuits (IC) because of the large number of resistors and the large coupling and bypass capacitor required for biasing discrete electronic circuits. It is uneconomical to fabricate IC resistors since they take a disproportionately large area on an IC chip. In addition, it is almost impossible to fabricate IC inductors. Biasing of ICs is done using mostly transistors that are connected to create constant current sources. Examples of integrated circuit biasing schemes are discussed in this section.

12.3.1 Simple current mirror

A simple current mirror is shown in Figure 12.10. The current mirror consists of two matched transistors Q_1 and Q_2 with their bases and emitters connected. The transistor Q_1 is connected as a diode by shorting the base to its collector.

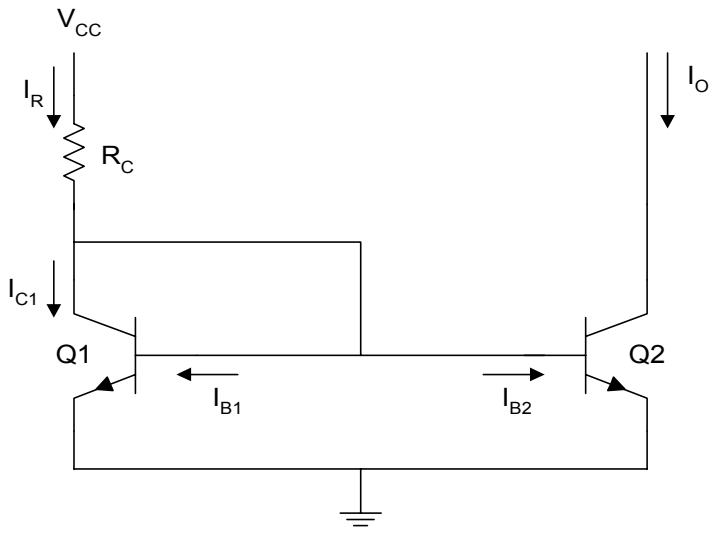


Figure 12.10 Simple Current Mirror

From Figure 12.10, we observe that

$$I_R = \frac{V_{CC} - V_{BE}}{R_C} \tag{12.50}$$

Using KCL, we get

$$I_R = I_{C1} + I_{B1} + I_{B2}$$

$$= I_{E1} + I_{B2} \tag{12.51}$$

But

$$I_{B2} = \frac{I_{E2}}{\beta + 1}$$

Assuming matched transistors

$$I_{B1} \cong I_{B2}$$

$$I_{E1} \cong I_{E2} \tag{12.52}$$

From Equations (12.51) and (12.52), we get

$$I_R = I_{E1} + \frac{I_{E2}}{\beta+1} \cong I_{E2}\left[1 + \frac{1}{\beta+1}\right] = \left[\frac{\beta+2}{\beta+1}\right] I_{E2} \tag{12.53}$$

and

$$I_O = I_{C2} = \beta I_{B2} = \frac{\beta I_{E2}}{\beta+1}$$

Therefore

$$I_O = \left[\frac{\beta}{\beta+1}\right]\left[\frac{\beta+1}{\beta+2}\right] I_R = \frac{\beta}{\beta+2} I_R \tag{12.54}$$

$$I_O \cong I_R \text{ if } \beta >> 1 \tag{12.55}$$

Equation (15.55) is true provided Q_2 is in the active mode. In the latter mode of transistor operation, the device Q_2 behaves as a current source. For Q_2 to be in the active mode, the following relation should be satisfied

$$V_{CE2} > V_{CEsat}$$

12.3.2 Wilson current source

The Wilson current source, shown in Figure 12.11, achieves high output resistance and an output current that is less dependent on transistor β_F. To obtain an expression for the output current, we assume that all three transistors are identical. Thus

$$I_{C1} = I_{C2}$$

$$V_{BE1} = V_{BE2}$$

$$\beta_{F1} = \beta_{F2} = \beta_{F3} = \beta_F \tag{12.56}$$

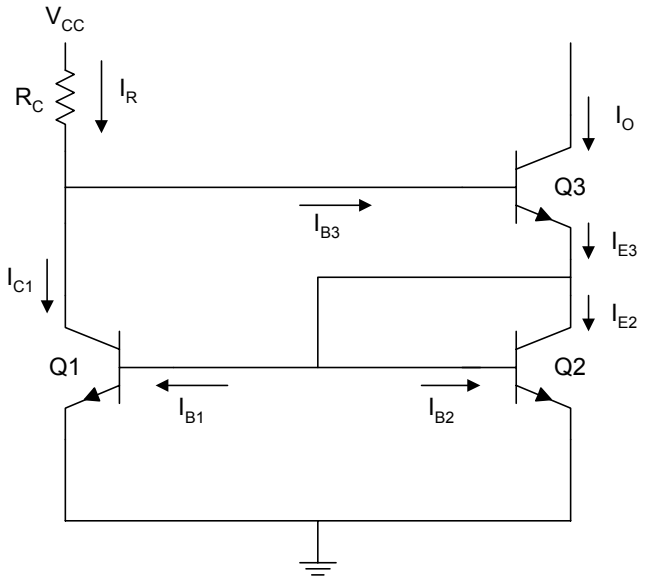


Figure 12.11 Wilson Current Source

Using KCL at the collector of transistor Q_3 , we get

$$I_{C1} = I_R - I_{B3} = I_R - \frac{I_O}{\beta_F}$$

therefore,

$$I_O = \beta_F \left(I_R - I_{C1} \right) \tag{12.57}$$

Using KCL at the emitter of Q_3 , we obtain

$$I_{E3} = I_{C2} + I_{B1} + I_{B2} = I_{C1} + 2I_{B1}$$

$$= I_{C1}\left(1+\frac{2}{\beta_F}\right) \tag{12.58}$$

But

$$I_0 = \alpha_F I_{E3} = \frac{\beta_F}{\beta_F+1} I_{E3} \tag{12.59}$$

Substituting Equation (12.58) into (12.59), we have

$$I_0 = \left(\frac{\beta_F}{\beta_F+1}\right)\left(1+\frac{2}{\beta_F}\right) I_{C1} \tag{12.60}$$

Simplifying Equation (12.60), we get

$$I_{C1} = \left(\frac{\beta_F+1}{\beta_F+2}\right) I_0 \tag{12.61}$$

Combining Equations (12.57) and (12.61), we obtain

$$I_0 = \beta_F\left[I_R - \left(\frac{\beta_F+1}{\beta_F+2}\right) I_0\right] \tag{12.62}$$

Simplifying Equation (12.62), we get

$$I_0 = \left(\frac{\beta_F^2+2\beta_F}{\beta_F^2+2\beta_F+2}\right) I_R$$

$$= \left(1-\frac{2}{\beta_F^2+2\beta_F+2}\right) I_R \tag{12.63}$$

For reasonable values of β_F

$$\left(\frac{2}{\beta_F^2+2\beta_F+2}\right) << 1$$

and Equation (12.63) becomes

$$I_0 \cong I_R$$

Thus, β has little effect on the output current, and

$$I_R = \frac{V_{CC} - V_{BE3} - V_{BE1}}{R_C} \tag{12.64}$$

Example 12.4

For Figures 12.10 and 12.11, what are the percentage difference between the reference and output currents for the β_F from 40 to 200. Assume that for both figures, $V_{CC} = 10\,V$, $R_C = 50K\Omega$ and $V_{BE} = 0.7\,V$.

Solution

We use Equation (12.50) to calculate I_R and Equation (12.53) to find I_0 of the simple current mirror. Similarly, we use Equation (12.64) to find I_R and Equation (12.63) to calculate I_0 of the Wilson current source.

MATLAB Script

```
% Integrated circuit Biasing
vcc=10; rc=50e3; vbe=0.7;
beta =40:5:200;  ir1=(vcc-vbe)/rc;
ir2=(vcc-2*vbe)/rc;  m=length(beta);
for i=1:m
  io1(i) = beta(i)*ir1/(beta(i) + 2);
  pd1(i)=abs((io1(i)-ir1)*100/ir1);
  io2(i)=(beta(i)^2+2*beta(i))/(beta(i)^2+2*beta(i)+2);
  pd2(i)=abs((io2(i)*ir2-ir2)*100/ir2);
end
subplot(211), plot(beta,pd1)
%title('error for simple current mirror')
xlabel('Transistor beta')
ylabel('Percentage error')
text(90,5,'Error for simple current mirror')
subplot(212),plot(beta,pd2)
```

```
%title('Error for Wilson current mirror')
xlabel('Transistor beta')
ylabel('Percentage error')
text(90, 0.13, 'Error for Wilson current source')
```

Figure 12.12 shows the percentage errors obtained for the simple current mirror and Wilson current source.

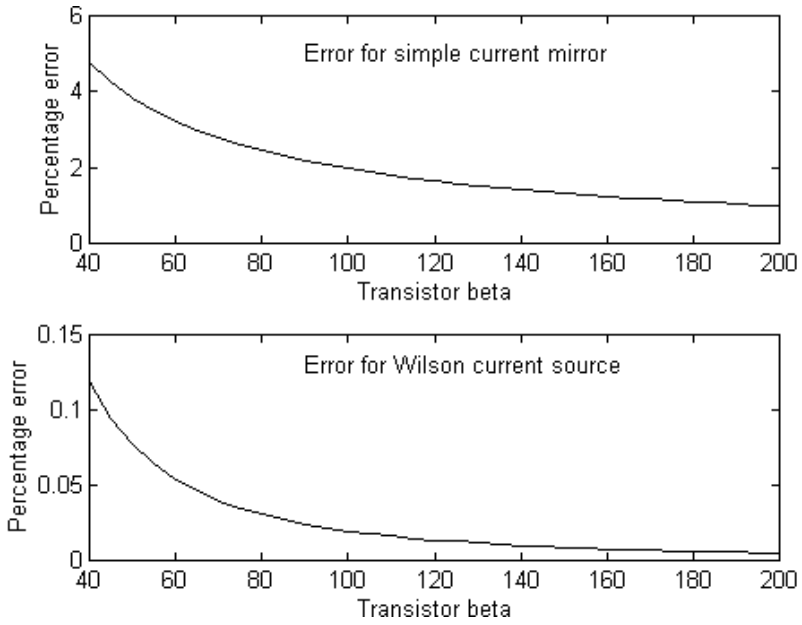


Figure 12.12 Percentage Error between Reference and Output Currents for Simple Current Mirror and Wilson Current Source

12.4 FREQUENCY RESPONSE OF COMMON EMITTER AMPLIFIER

The common-emitter amplifier, shown in Figure 12.13, is capable of generating a relatively high current and voltage gains. The input resistance is medium and is essentially independent of the load resistance R_L. The output resistance is relatively high and is essentially independent of the source resistance.

The coupling capacitor, C_{C1}, couples the source voltage v_S to the biasing network. Coupling capacitor C_{C2} connects the collector resistance R_C to the load R_L. The bypass capacitance C_E is used to increase the midband gain, since it effectively short circuits the emitter resistance R_E at midband frequencies. The resistance R_E is needed for bias stability. The external capacitors C_{C1}, C_{C2}, C_E will influence the low frequency response of the common emitter amplifier. The internal capacitances of the transistor will influence the high frequency cut-off. The overall gain of the common-emitter amplifier can be written as

$$A(s) = \frac{A_m s^2 \left(s + w_z\right)}{\left(s + w_{L1}\right)\left(s + w_{L2}\right)\left(s + w_{L3}\right)\left(1 + s/w_H\right)} \tag{12.65}$$

where

A_M is the midband gain.

w_H is the frequency of the dominant high frequency pole

w_{L1}, w_{L2}, w_{L3} are low frequency poles introduced by the coupling and bypass capacitors

w_Z is the zero introduced by the bypass capacitor.

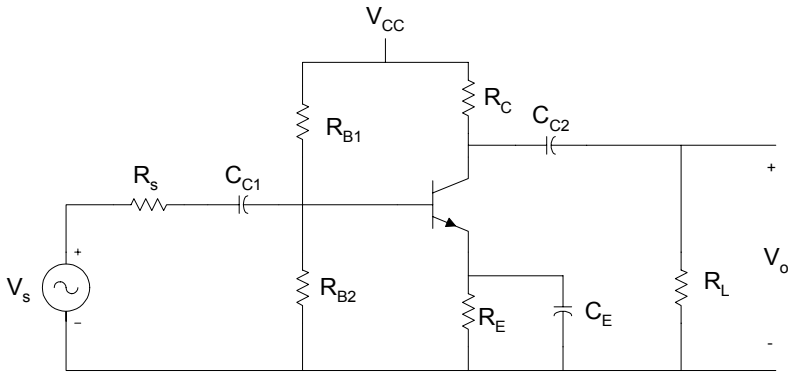


Figure 12.13 Common Emitter Amplifier

The midband gain is obtained by short circuiting all the external capacitors and open circuiting the internal capacitors. Figure 12.14 shows the equivalent for calculating the midband gain.

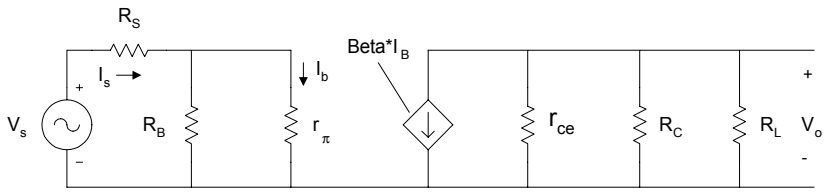


Figure 12.14 Equivalent Circuit for Calculating Midband Gain

From Figure 12.14, the midband gain, A_m, is

$$A_m = \frac{V_O}{V_S} = -\beta\left[r_{CE} \| R_C \| R_L\right]\left[\frac{R_B}{R_B + r_\pi}\right]\left[\frac{1}{R_S + \left[R_B \| r_\pi\right]}\right] \tag{12.66}$$

It can be shown that the low frequency poles, w_{L1}, w_{L2}, w_{L3}, can be obtained by the following equations

$$\tau_1 = \frac{1}{w_{L1}} = C_{C1} R_{IN} \tag{12.67}$$

where

$$R_{IN} = R_S + \left[R_B \| r_\pi\right] \tag{12.68}$$

$$\tau_2 = \frac{1}{w_{L2}} = C_{C2}\left[R_L + \left(R_C \| r_{ce}\right)\right] \tag{12.69}$$

and

$$\tau_3 = \frac{1}{w_{L3}} = C_E R_E^{'} \tag{12.70}$$

where

$$R_E^{'} = R_E \left\| \left[\frac{r_\pi}{\beta_F + 1} + \left(\frac{R_B \| R_S}{\beta_F + 1} \right) \right] \right. \tag{12.71}$$

and the zero

$$w_Z = \frac{1}{R_E C_E} \tag{12.72}$$

Normally, $w_Z < w_{L3}$ and the low frequency cut-off w_L is larger than the largest pole frequency. The low frequency cut-off can be approximated as

$$w_L \cong \sqrt{\left(w_{L1}\right)^2 + \left(w_{L2}\right)^2 + \left(w_{L3}\right)^2} \tag{12.73}$$

The high frequency equivalent circuit of the common-emitter amplifier is shown in Figure 12.15.

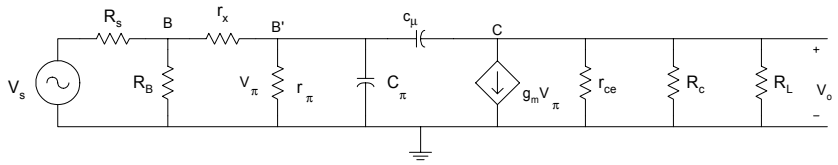


Figure 12.15 Equivalent Circuit of CE Amplifier at High Frequencies

In Figure 12.15, C_μ is the collector-base capacitance, C_π is the emitter to base capacitance, r_X is the resistance of silicon material of the base region between the base terminal B and an internal or intrinsic base terminal B'. Using the Miller Theorem, it can be shown that the 3-dB frequency at high frequencies is approximately given as

$$w_H^{-1} = \left(r_\pi \left\| \left[r_x + \left(R_B \| R_S \right) \right] \right. \right) C_T \tag{12.74}$$

where

$$C_T = C_\pi + C_\mu \left[1 + g_m \left(R_L \| R_C \right) \right] \tag{12.75}$$

and

$$g_m = \frac{I_C}{V_T} \tag{12.76}$$

In the following example, MATLAB is used to obtain the frequency response of a common-emitter amplifier.

Example 12.5

For a CE amplifier shown in Figure 12.13,
$\beta = 150,\ R_L = 2\ K\Omega,\ R_C = 4\ K\Omega, C_\pi = 100\ pF,\ C_\mu = 5\ pF,\ V_{CC} = 10\ V,$
$r_{ce} = r_o = 60\ K\Omega,\ R_E = 1.5\ K\Omega,\ C_{C1} = 2\ \mu F, C_{C2} = 4\ \mu F,\ C_E = 150\ \mu F,$
$R_{B1} = 60\ K\Omega,\ R_{B2} = 40\ K\Omega, R_S = 100\Omega,\ r_x = 10\ \Omega.$
Use MATLAB to plot the magnitude response of the amplifier.

Solution

Using Equations (12.67), (12.69), (12.70) and (12.74) are used to calculate the poles of Equation (12.65). The zero of the overall amplifier gain is calculated using Equation (12.66). The MATLAB program is as follows:

MATLAB Script

```
%Frequency response of CE Amplifier
rc=4e3; rb1=60e3; rb2=40e3; rs=100; rce=60e3;
re=1.5e3; rl=2e3; beta=150; vcc=10; vt=26e-3; vbe =0.7;
cc1=2e-6; cc2=4e-6; ce=150e-6;, rx=10; cpi=100e-12;
cmu=5e-12;
%  Ic is calculated
rb = (rb1 * rb2)/(rb1 + rb2);
vbb = vcc * rb2/(rb1 + rb2);
icq = beta * (vbb - vbe)/(rb + (beta + 1)*re);

% Calculation of low frequency poles
% using equations (12.67), (12.69) and (12.70)
rpi=beta * vt/icq;
rb_rpi=rpi * rb/(rpi + rb);
rin=rs + rb_rpi;
wl1=1/(rin * cc1);
rc_rce=rc * rce/(rc + rce);
```

```
wl2=1/(cc2 * (rl + rc_rce));
rb_rs=rb * rs/(rb + rs);
rx1=(rpi + rb_rs)/(beta + 1);
re_prime=re * rx1/(re + rx1);
wl3=1/(re_prime * ce);

% Calculate the low frequency zero using equation (12.72)
wz = 1/(re*ce);
% Calculate the high frequency pole using equation (12.74)
gm = icq/vt;
rbrs_prx = ( rb * rs/(rb + rs)) + rx;
rt = (rpi * rbrs_prx)/(rpi + rbrs_prx);
rl_rc = rl * rc/(rl + rc);
ct = cpi + cmu * (1 + gm * rl_rc);
wh = 1/(ct * rt);
% Midband gain is calculated
rcercrl = rce * rl_rc/(rce + rl_rc);
am = -beta * rcercrl * (rb/(rb + rpi)) * (1/(rin));

% Frequency response calculation using equation (12.65)
a4 = 1; a3 = wl1 + wl2 + wl3 + wh;
a2 = wl1*wl2 + wl1*wl3 + wl2*wl3 + wl1*wh + wl2*wh + wl3*wh;
a1 = wl1*wl2*wl3 +wl1*wl2*wh + wl1*wl3*wh + wl2*wl3*wh;
a0 = wl1*wl2*wl3*wh;
den=[a4 a3 a2 a1 a0];
b3 = am*wh;
b2 = b3*wz; b1 =0; b0 = 0;
num = [b3 b2 b1 b0];
w = logspace(1,10);
h = freqs(num,den,w);
mag = 20*log10(abs(h));
f = w/(2*pi);
% Plot the frequency response
semilogx(f,mag,'w')
title('Magnitude Response')
xlabel('Frequency, Hz')
ylabel('Gain, dB')
axis([1, 1.0e10, 0, 45])
```

The frequency response is shown in Figure 12.16.

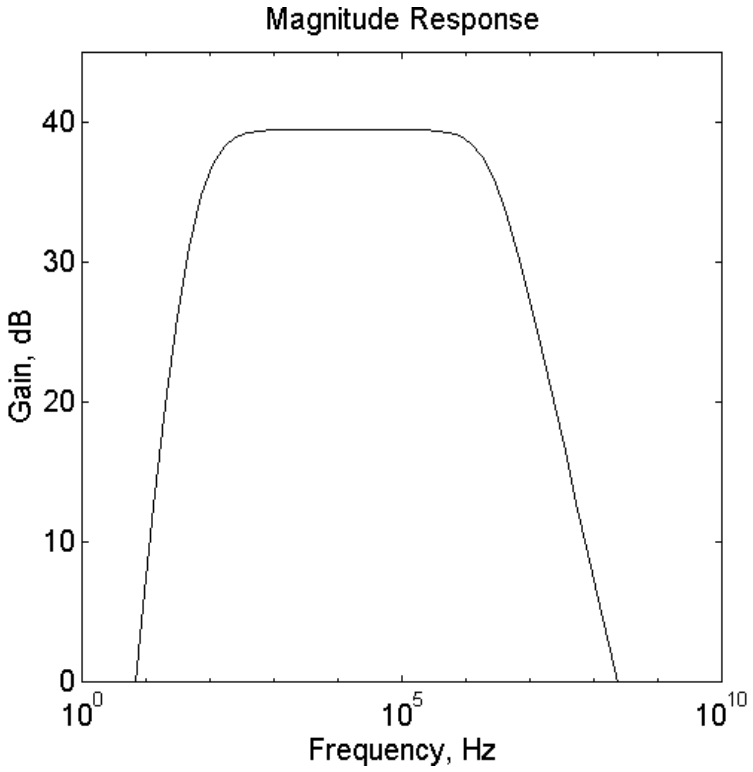


Figure 12.16 Frequency Response of a CE Amplifier

12.5 MOSFET CHARACTERISTICS

Metal-oxide-semiconductor field effect transistor (MOSFET) is a four-terminal device. The terminals of the device are the gate, source, drain, and substrate. There are two types of mosfets: the enhancement type and the depletion type. In the enhancement type MOSFET, the channel between the source and drain has to be induced by applying a voltage on the gate. In the depletion type mosfet, the structure of the device is such that there exists a channel between the source and drain. Because of the oxide insulation between the gate and the channel, mosfets have high input resistance. The electronic symbol of a mosfet is shown in Figure 12.19.

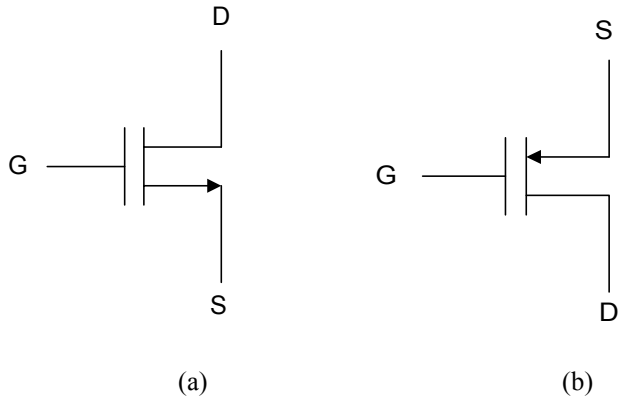


Figure 12.17 Circuit Symbol of (a) N-channel and (b) P-channel MOSFETs

Mosfets can be operated in three modes: cut-off, triode, and saturation regions. Because the enhancement mode mosfet is widely used, the presentation in this section will be done using an enhancement-type mosfet. In the latter device, the channel between the drain and source has to be induced by applying a voltage between the gate and source. The voltage needed to create the channel is called the threshold voltage, V_T. For an n-channel enhancement-type mosfet , V_T is positive and for a p-channel device it is negative.

Cut-off Region

For an n-channel mosfet, if the gate-source voltage V_{GS} satisfies the condition

$$V_{GS} < V_T \tag{12.77}$$

then the device is cut-off. This implies that the drain current is zero for all values of the drain-to-source voltage.

Triode Region

When $V_{GS} > V_T$ and V_{DS} is small, the mosfet will be in the triode region. In the latter region, the device behaves as a non-linear voltage-controlled resistance. The I-V characteristics are given by

$$I_D = k_n\left[2\left(V_{GS} - V_T\right)V_{DS} - {V_{DS}}^2\right] \tag{12.78}$$

provided

$$V_{DS} \le V_{GS} - V_T \tag{12.79}$$

where

$$k_n = \frac{\mu_n \varepsilon \varepsilon_{ox}}{2t_{ox}}\frac{W}{L} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right) \tag{12.80}$$

and

μ_n	is surface mobility of electrons
ε	is permittivity of free space (8.85 E-14 F/cm)
ε_{ox}	is dielectric constant of SiO_2
t_{ox}	is thickness of the oxide
L	is length of the channel
W	is width of the channel

Saturation Region

Mosfets can operate in the saturation region. A mosfet will be in saturation provided

$$V_{DS} \ge V_{GS} - V_T \tag{12.81}$$

and I-V characteristics are given as

$$I_D = k_n\left(V_{GS} - V_T\right)^2 \tag{12.82}$$

The dividing locus between the triode and saturation regions is obtained by substituting

$$V_{DS} = V_{GS} - V_T \tag{12.83}$$

into either Equation (12.78) or (12.82), so we get

$$I_D = k_n V_{DS}^{\ 2} \tag{12.84}$$

In the following example, I-V characteristics and the locus that separates triode and saturation regions are obtained using MATLAB.

Example 12.6

For an n-channel enhancement-type MOSFET with $k_n = 1\ \ mA/V^2$ and $V = 1.5\,V$, use MATLAB to sketch the I-V characteristics for $V_{GS} = 4, 6, 8\,V$ and for V_{DS} between 0 and $12\,V$.

Solution

MATLAB Script

```
% I-V characteristics of mosfet
%
kn=1e-3; vt=1.5;
vds=0:0.5:12;
vgs=4:2:8;
m=length(vds);
n=length(vgs);

for i=1:n
        for j=1:m
          if vgs(i) < vt
                cur(i,j)=0;
          elseif vds(j) >= (vgs(i) - vt)
                cur(i,j)=kn * (vgs(i) - vt)^2;
          elseif vds(j) < (vgs(i) - vt)
                cur(i,j)= kn*(2*(vgs(i)-vt)*vds(j) - vds(j)^2);
          end
    end
end
plot(vds,cur(1,:),'w',vds,cur(2,:),'w',vds,cur(3,:),'w')
xlabel('Vds, V')
ylabel('Drain Current,A')
title('I-V Characteristics of a MOSFET')
text(6, 0.009, 'Vgs = 4 V')
```

```
text(6, 0.023, 'Vgs = 6 V')
text(6, 0.045, 'Vgs = 8 V')
```

Figure 12.18 shows the I-V characteristics.

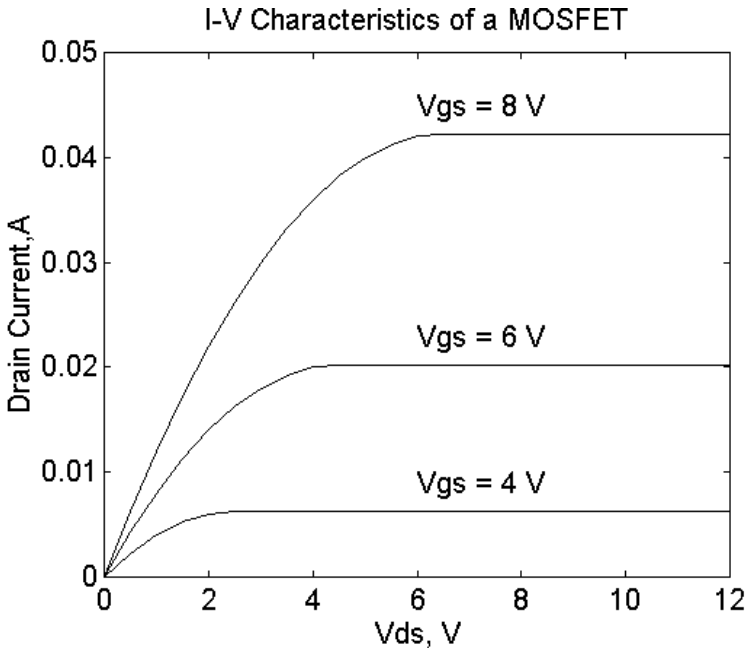


Figure 12.18 I-V Characteristics of N-channel Enhancement-type Mosfet

12.6 BIASING OF MOSFET CIRCUITS

A popular circuit for biasing discrete mosfet amplifiers is shown in Figure 12.19. The resistances R_{G1} and R_{G2} will define the gate voltage. The resistance R_S improves operating point stability.

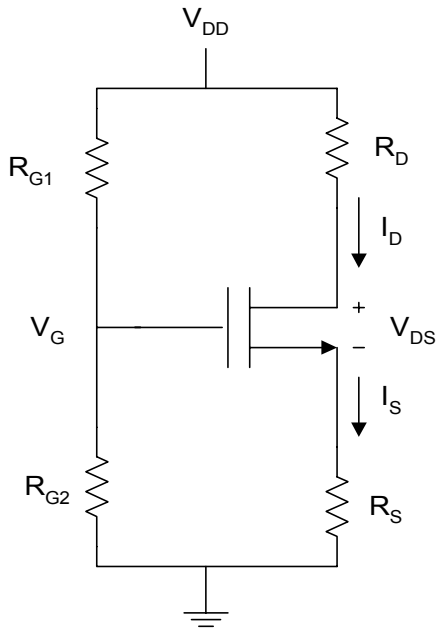


Figure 12.19 Simple Biasing Circuit for Enhancement-type NMOS

Because of the insulated gate, the current that passes through the gate of the MOSFET is negligible. The gate voltage is given as

$$V_G = \frac{R_{G1}}{R_{G1} + R_{G2}} V_{DD} \tag{12.85}$$

The gate-source voltage V_{GS} is

$$V_{GS} = V_G - I_S R_S \tag{12.86}$$

For conduction of the MOSFET, the gate-source voltage V_{GS} should be greater than the threshold voltage of the mosfet, V_T. Since $I_D = I_S$, Equation (12.86) becomes

$$V_{GS} = V_G - I_D R_S \tag{12.87}$$

The drain-source voltage is obtained by using KVL for the drain-source circuit

$$V_{DS} = V_{DD} - I_D R_D - I_S R_S$$

$$= V_{DD} - I_D (R_D - R_S) \tag{12.88}$$

For proper operation of the bias circuit,

$$V_{GS} > V_T \tag{12.89}$$

When Equation (12.89) is satisfied, the MOSFET can either operate in the triode or saturation region. To obtain the drain current, it is initially assumed that the device is in saturation and Equation (12.82) is used to calculate I_D. Equation (12.81) is then used to confirm the assumed region of operation. If Equation (12.82) is not satisfied, then Equation (12.78) is used to calculate I_D. The method is illustrated by the following example.

Example 12.7

For Figure 12.19, V_T = 2 V, k_n = 0.5 mA/V^2, V_{DD} = 9V, $R_{G1} = R_{G2} = 10\ M\Omega$, $R_S = R_D = 10\ K\Omega$. Find I_D and V_{DS}.

Solution

Substituting Equation (12.86) into Equation (12.82), we have

$$I = k_n \left(V_g - I_D R_D - V_T \right)^2 \tag{12.90}$$

Simplifying Equation (12.90), we have

$$0 = k_n R_D^2 I_D^2 - \left[1 + 2(V_g - V_T) R_D \right] I_D + k \left(V_g - V_T \right)^2 \tag{12.91}$$

The above quadratic equation is solved to obtain I_D. Two solutions of I_D are obtained. However, only one is sensible and possible. The possible one is

the one that will make $V_{GS} > V_T$. With the possible value of I_D obtained, V_{DS} is calculated using Equation (12.88). It is then verified whether

$$V_{DS} > V_{GS} - V_T$$

The above condition ensures saturation of the device. If the device is not in saturation, then substituting Equation (12.86) into Equation (12.78), we get

$$I_D = k_n\left[2(V_g - I_D R_D - V_T)(V_{DD} - (R_D + R_S)I_D) - \left(V_{DD} - (R_D + R_S)I_D\right)^2\right] \quad (12.92)$$

Simplifying Equation (12.92), we get the quadratic equation

$$\begin{aligned} 0 = {} & I_D^2\left[(R_S + R_D)^2 + 2R_D(R_D + R_S)\right] \\ & + I_D\left[2V_{DD}(R_D + R_S) - 2V_{DD}R_D - 2(V_g - V_T)(R_D + R_S) - {}^{1}\!/_{k_n}\right] \\ & + 2(V_g - V_T)V_{DD} - V_{DD}^2 \end{aligned} \quad (12.93)$$

Two roots are obtained by solving Equation (12.93). The sensible and possible root is the one that will make

$$V_{GS} > V_T$$

The MATLAB program for finding I_D is shown below.

MATLAB Script

```
%
% Analysis of MOSFET bias circuit
%
diary ex12_7.dat
diary on
vt=2; kn=0.5e-3; vdd=9;
rg1=10e6; rg2=10e6; rs=10e3; rd=10e3;
vg=vdd * rg2/(rg1 + rg2);

% Id is calculated assuming device is in saturation

a1=kn*(rd^2);
a2=-(1 + 2*(vg - vt)*rd * kn);
```

```
a3=kn * (vg - vt)^2;
p1=[a1,a2,a3];
r1=roots(p1);

% check for the sensible value of the drain current

vgs = vg - rs * r1(1);
 if vgs > vt
          id = r1(1);
  else
          id = r1(2);
% check for sensible value of the drain current
  vgs = vg - rs*r2(1);
          if vgs > vt
            id = r2(1);
           else
            id=r2(2);
          end
vds=vdd - (rs + rd)*id;
end

% print out results
fprintf('Drain current is %7.3e Amperes\n',id)
fprintf('Drain-source voltage is %7.3e Volts\n', vds)
```

The results are

```
Drain current is 1.886e-004 Amperes
Drain-source voltage is 5.228e+000 Volts
```

The circuit shown in Figure 12.20 is a mosfet transistor with the drain connected to the gate. The circuit is normally referred to as diode-connected enhancement transistor.

From Equation (12.88), the MOSFET is in saturation provided

$$V_{DS} > V_{GS} - V_T$$

i.e.,

$$V_{DS} - V_{GS} > -V_T \quad \text{or} \quad V_{DS} + V_{SG} > -V_T$$

or

$$V_{DG} > -V_T \tag{12.94}$$

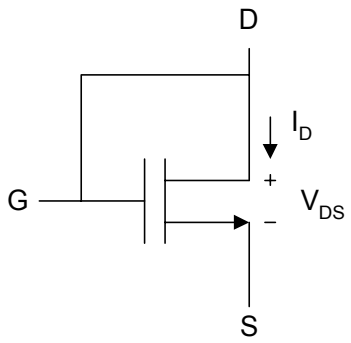


Figure 12.20 Diode-connected Enhancement Type MOSFET

Since $V_{DG} = 0$ and V_T is positive for n-channel MOSFET, the device is in saturation and

$$i_D = k_n\left(V_{GS} - V_T\right)^2 \tag{12.95}$$

But if $V_{GS} = V_{DS}$, Equation (12.101) becomes

$$i_D = k_n\left(V_{DS} - V_T\right)^2$$

The diode-connected enhancement mosfet can also be used to generate dc currents for nMOS and CMOS analog integrated circuits. A circuit for generating dc currents that are constant multiples of a reference current is shown in Figure 12.21. It is a MOSFET version of current mirror circuits discussed in Section 12.3.

Assuming the threshold voltages of the transistors of Figure 12.21 are the same, then since transistor T1 is in saturation,

$$I_{REF} = k_1\left(V_{GS1} - V_T\right)^2 \tag{12.96}$$

Since transistors T1 and T2 are connected in parallel, we get

$$V_{GS1} = V_{GS2} = V_{GS} \tag{12.97}$$

and

$$I_0 = k_2\left(V_{GS2} - V_T\right)^2$$

$$I_0 = k_2\left(V_{GS} - V_T\right)^2 \tag{12.98}$$

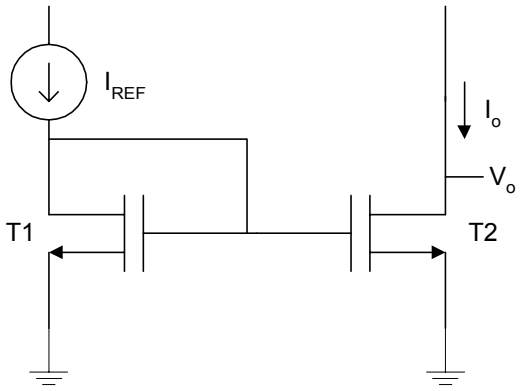


Figure 12.21 Basic MOSFET Current Mirror

Combining Equations (12.96) and (12.98), the current

$$I_0 = I_{REF}\left(\frac{k_2}{k_1}\right) \tag{12.99}$$

and using Equation (12.74), Equation (12.99) becomes

$$I_0 = I_{REF}\left(\frac{\left(W/L\right)_2}{\left(W/L\right)_1}\right) \tag{12.100}$$

Thus, I_0 will be a multiple of I_{REF}, and the scaling constant is determined by the device geometry. In practice, because of the finite output resistance of transistor T2, I_0 will be a function of the output voltage v_0.

Example 12.8

For the circuit shown in Figure 12.22, $R_1 = 1.5\ M\Omega$, $L_1 = L_2 = 6\ \mu m$, $W_1 = 12\ \mu m$, $W_2 = 18\ \mu m$, V_T = 2.0 V and $V_{DD} = 5$ V. Find the output current I_{D1}, V_{GS1}, I_0 and R_2. Assume that V_0 = 2.5 V, μC_{OX} = 30 $\mu A / V^2$. Neglect channel length modulation.

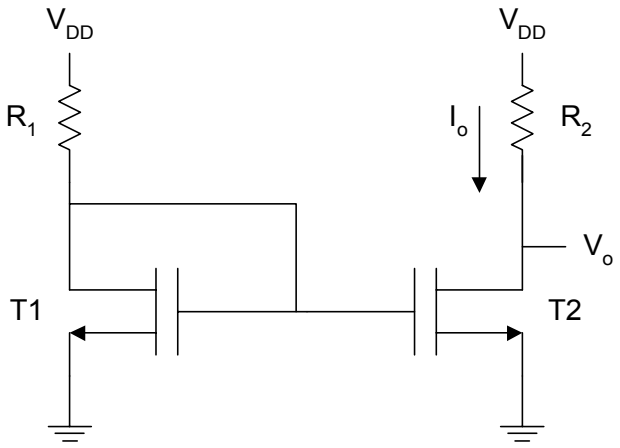


Figure 12.22 Circuit for Example 12.8

Solution

Since T1 is in saturation,

$$I_{D1} = k_{n1}\left(V_{GS} - V_T\right)^2 = k_{n1}(V_{DS} - V_T)^2 \qquad (12.101)$$

$$V_{DS} = V_{DD} - I_{D1}R_1 \qquad (12.102)$$

Substituting Equation (12.100) into (12.99), we get

$$I_{D1} = k_{n1}\left(V_{DD} - V_T - R_1 I_{D1}\right)^2$$

$$\frac{I_{D1}}{k_{n1}} = \left(V_{DD} - V_T\right)^2 - 2(V_{DD} - V_T)R_1 I_{D1} + R_1^2 I_{D1}^2$$

$$0 = R_1^2 I_{D1}^2 - \left(2(V_{DD} - V_T)R_1 + \frac{1}{k_{n1}}\right)I_{D1} + \left(V_{DD} - V_T\right)^2 \qquad (12.103)$$

The above quadratic equation will have two solutions, but only one of the solution of I_{D1} will be valid. The valid solution will result in $V_{GS} > V_T$.

Using equation (12.100), we obtain

$$I_0 = I_{D1}\left(\frac{\left(W/L\right)_2}{\left(W/L\right)_1}\right) \qquad (12.104)$$

and

$$R = \frac{5 - V_0}{I_0} \qquad (12.105)$$

The MATLAB program is as follows:

MATLAB Script

```
%
% Current mirror
%
diary ex12_8.dat
diary on
ucox = 30e-6; l1 = 6e-6; l2 = 6e-6;
w1 = 12e-6; w2=18e-6;
r1=1.5e6; vt=2.0; vdd=5; vout=2.5;

% roots of quadratic equation(12.103) is obtained
kn = ucox * w1/(2 * l1);
a1 = r1^2;
a2 = -2*(vdd - vt)*r1 - (1/kn);
```

```
a3 = (vdd - vt)^2;
p = [a1,a2,a3];
i = roots(p);

% check for realistic value of drain current
vgs=vdd - r1*i(1);
if vgs > vt
        id1 = i(1);
 else
        id1 = i(2);
end

% output current is calculated from equation(12.100)
% r2 is obtained using equation (12.105)
iout = id1*w2*l1/(w1 * l2);
r2=(vdd - vout)/iout;

% print results
fprintf('Gate-source Voltage of T1 is %8.3e Volts\n',vgs)
fprintf('Drain Current of T1 is %8.3e Ampers\n', id1)
fprintf('Drain Current Io is %8.3e Ampers\n', iout)
fprintf('Resistance R2 is %8.3e Ohms\n', r2)
```

The results are

```
Gate-source Voltage of T1 is 1.730e+000 Volts
Drain Current of T1 is 1.835e-006 Ampers
Drain Current Io is 2.753e-006 Ampers
Resistance R2 is 9.082e+005 Ohms
```

12.7 FREQUENCY RESPONSE OF COMMON-SOURCE AMPLIFIER

The common-source amplifier has characteristics similar to those of the common-emitter amplifier discussed in Section 12.4. However, the common-source amplifier has higher input resistance than that of the common-emitter amplifier. The circuit for the common source amplifier is shown in Figure 12.23.

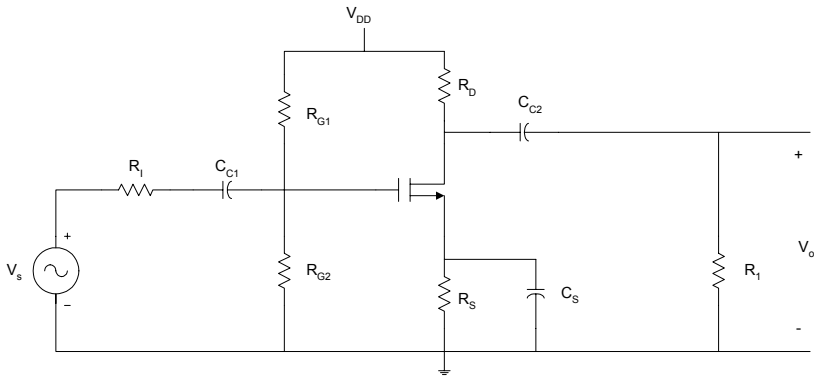


Figure 12.23 Common-Source Amplifier

The external capacitors C_{C1}, C_{C2} and C_S will influence the low frequency response. The internal capacitances of the FET will affect the high frequency response of the amplifier. The overall gain of the common-source amplifier can be written in a form similar to Equation (12.65).

The midband gain, A_m, is obtained from the midband equivalent circuit of the common-source amplifier. This is shown in Figure 12.24. The equivalent circuit is obtained by short-circuiting all the external capacitors and open-circuiting all the internal capacitances of the FET.

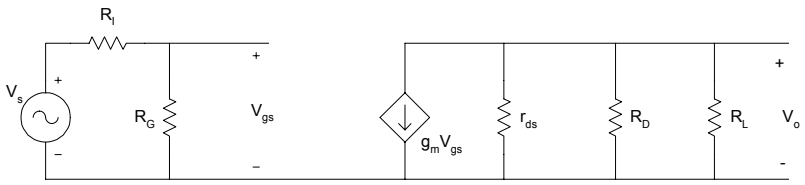


Figure 12.24 Midband Equivalent Circuit of Common-Source Amplifier

Using voltage division,

$$v_{gs} = \frac{R_G}{R_I + R_G} v_S \tag{12.106}$$

From Ohm's Law,

$$v_0 = -g_m v_{gs}\left(r_{ds} \| R_D \| R_L\right) \tag{12.107}$$

Substituting Equation (12.106) into (12.107), we obtain the midband gain as

$$A_m = \frac{v_0}{v_s} = -g_m\left(\frac{R_G}{R_G + R_I}\right)\left(r_{ds} \| R_D \| R_L\right) \tag{12.108}$$

At low frequencies, the small signal equivalent circuit of the common-source amplifier is shown in Figure 12.25.

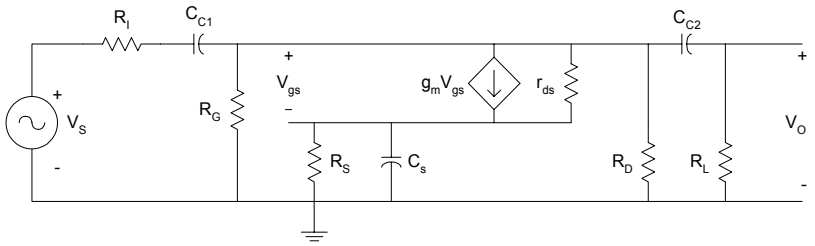


Figure 12.25 Equivalent Circuit for Obtaining the Poles at Low Frequencies of Common-source Amplifier

It can be shown that the low frequency poles due to C_{C1} and C_{C2} can be written as

$$\tau_1 = \frac{1}{w_{L1}} \cong C_{C1}(R_g + R_I) \tag{12.109}$$

$$\tau_2 = \frac{1}{w_{L2}} \cong C_{C2}(R_L + R_D \| r_{ds}) \tag{12.110}$$

Assuming r_d is very large, the pole due to the bypass capacitance C_S can be shown to be

$$\tau_3 = \frac{1}{w_{L3}} \cong C_S\left(\frac{R_S}{1 + g_m R_S}\right) \tag{12.111}$$

and the zero of C_S is

$$w_Z = \frac{1}{R_S C_S} \tag{12.112}$$

The 3-dB frequency at the low frequency can be approximated as

$$w_L \cong \sqrt{\left(w_{L1}\right)^2 + \left(w_{L2}\right)^2 + \left(w_{L3}\right)^2} \tag{12.113}$$

For a single stage common-source amplifier, the source bypass capacitor is usually the determining factor in establishing the low 3-dB frequency.

The high frequency equivalent circuit of a common-source amplifier is shown in Figure 12.26. In the figure, the internal capacitances of the FET, C_{gs}, C_{gd} and C_{ds} are shown. The external capacitors of the common of common-source amplifier are short-circuited at high frequencies.

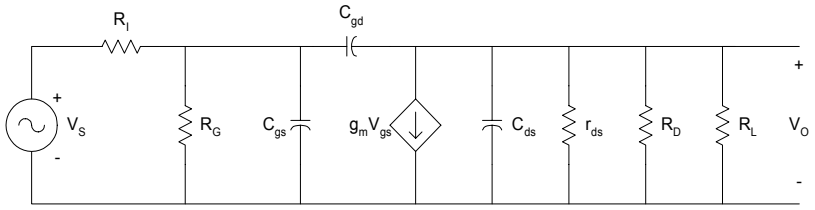


Figure 12.26 High Frequency Equivalent Circuit of Common-source Amplifier

Using the Miller theorem, Figure 12.26 can be simplified. This is shown in Figure 12.27.

The voltage gain at high frequencies is

$$A_V = \frac{v_0}{v_s} \cong -\left(\frac{R_G}{R_G + R_I}\right)\left(\frac{g_m R_L^{'}}{\left(1 + s(R_G \| R_I)C_1\right)\left(1 + sR_L^{'}C_2\right)}\right) \tag{12.114}$$

where

$$C_1 = C_{gs} + C_{gd}\left(1 + g_m R_L^{'}\right) \tag{12.115}$$

and

$$C_2 = C_{ds} + C_{gd} \tag{12.116}$$

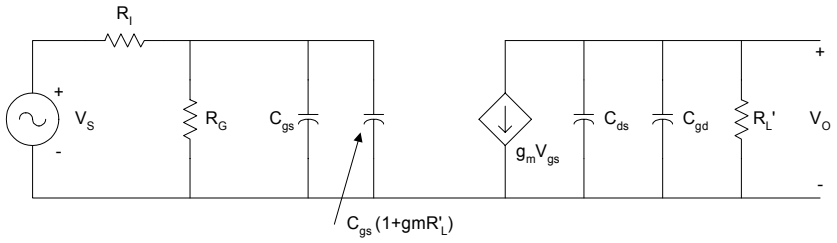


Figure 12.27 Simplified High Frequency Equivalent Circuit for Common-source Amplifier

The high frequency poles are

$$w_{H1} = \frac{1}{C_1\left(R_G \| R_I\right)} \tag{12.117}$$

$$w_{H2} = \frac{1}{C_2\left(R_L \| R_D \| r_{ds}\right)} \tag{12.118}$$

The approximate high frequency cut-off is

$$w_H = \frac{1}{\sqrt{\left(\frac{1}{w_{H1}}\right)^2 + \left(\frac{1}{w_{H2}}\right)^2}} \tag{12.119}$$

In the following example, MATLAB is used to obtain the midband gain, cut-off frequencies and bandwidth of a common-source amplifier.

Example 12.9

For the common-source amplifier, shown in Figure 12.23, $C_{C1} = C_{C2} = 1\mu F$, $C_S = 50\mu F$. The FET parameters are $C_{gd} = C_{ds} = 1\ pF$, $C_{gs} = 10\ pF$, $g_m = 10\ mA/V$, $r_{ds} = 50\ K\Omega$. $R_D = 8\ K\Omega$, $R_L = 10\ K\Omega$, $R_S = 2\ K\Omega$, $R_I = 50\ \Omega$, $R_{G1} = 5\ M\Omega$, $R_{G2} = 5\ M\Omega$. Determine (a) midband gain, (b) the low frequency cut-off, (c) high frequency cut-off, and (d) bandwidth of the amplifier.

Solution

MATLAB Script

```
%
% common-source amplifier
%
diary ex12_9.dat
diary on
rg1=5e6; rg2=5e6; rd=8e3; rl=10e3;
ri=50; rs=2e3; rds=50e3;
cc1=1e-6; cc2=1e-6; cs=50e-6;
gm=10e-3; cgs=10e-12; cgd=1e-12; cds=1e-12;

% Calculate midband gain using equation (12.108)
a = (1/rds) + (1/rd) + (1/rl);
rlprime = 1/a;
rg = rg1*rg2/(rg1 + rg2);
gain_mb = -gm*rg*rlprime/(ri + rg);

% Calculate Low cut-off frequency using equation (12.113)
t1 = cc1*(rg + ri);
wl1 = 1/t1;
rd_rds = (rd*rds)/(rd + rds);
t2 = cc2 * (rl + rd_rds);
wl2=1/t2;
t3=cs * rs/(1 + gm * rs);
wl3=1/t3;
wl=sqrt(wl1^2 + wl2^2 + wl3^2);
```

```
% Calculate high frequency cut-off using equations (12.115 to
12.119)
c1=cgs + cgd * (1 + gm * rlprime);
c2=cds + cgd;
rg_ri=rg * ri/(rg + ri);
wh1=1/(rg_ri * c1);
wh2=1/(rlprime * c2);
int_term = sqrt((1/wh1)^2 + (1/wh2)^2);
wh = 1/int_term;
bw = wh-wl;

%  Print results
fprintf('Midband Gain is %8.3f\n', gain_mb)
fprintf('Low frequency cut-off is %8.3e\n', wl)
fprintf('High frequency cut-off is %8.3e\n', wh)
fprintf('Bandwidth is %8.3e Hz\n', bw)
```

The results are

```
Midband Gain is  -40.816
Low frequency cut-off is 2.182e+002
High frequency cut-off is 1.168e+008
Bandwidth is 1.168e+008 Hz
```

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EXERCISES

12.1 For the data provided in Example 12.2, Use MATLAB to sketch the output characteristics for $V_{BE} = 0.3, 0.5, 0.7$ V. Do not neglect the effect of V_{AF} on the collector current.

12.2 For the self-bias circuit, shown in Figure 12.6, the collector current involving I_{CBO} is given by Equation (12.47). Assuming that $R_{B1} = 75\ K\Omega$, $R_{B2} = 25\ K\Omega$, $R_E = 1\ K\Omega$, $R_C = 7.5\ K\Omega$, $\beta_F = 100$, and at 25° C, V_{BE} = 0.6 V and I_{CBO} = 0.01 μA, determine the collector currents for temperatures between 25 °C and 85 °C. If R_E is changed to 3 $K\Omega$, what will be the value of I_C?

12.3 For Figure 12.13, if $R_{B1} = 50\ K\Omega$, $R_{B2} = 40\ K\Omega$, $r_S = 50\ \Omega$, $r_X = 10\ \Omega$, $R_L = 5\ K\Omega$, $R_C = 5\ K\Omega$, $r_{ce} = 100\ K\Omega$, $C_{C1} = C_{C2} = 2\mu F$, $C_\pi = 50pF$, $C_\mu = 2pF$, $\beta_F = 100$, V_{CC} = 10 V, explore the low frequency response for the following values of R_E: 0.1 KΩ, 1 KΩ, 5 KΩ. Calculate the high frequency cut-off for R_E = 0.1 KΩ.

12.4 For the Widlar current source, shown in Figure P12.4, determine the output current if $R_C = 40\ K\Omega$, V_{CC} = 10 V, V_{BE1} = 0.7 V and $R_2 = 25\ K\Omega$.

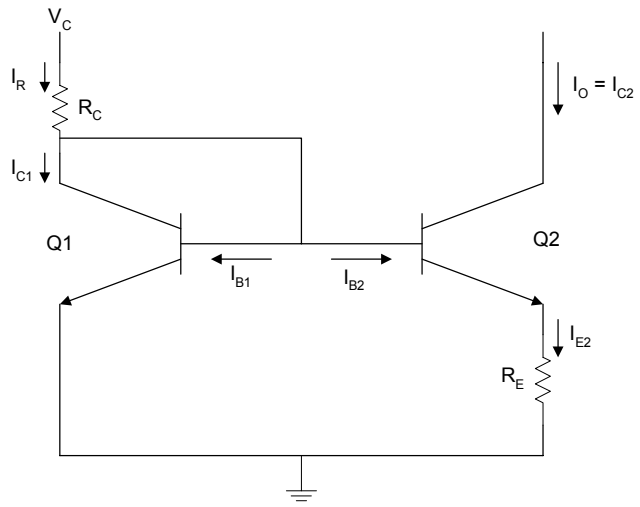

Figure P12.4 Widlar Current Source

12.5 For the n-channel enhancement-type MOSFET with $k_n = 2\ mA/V^2$ and $V_T = 1\,V$, write a MATLAB program to plot the triode characteristics for $V_{GS} = 2, 3, 4, 5$ V when $V_{DS} < 1\,V$.

12.6 For Figure 12.19, V_T = 1.5 V, k_n = 0.5 mA/V^2, V_{DD} = 10V, $R_{G1} = 10\ M\Omega$, $R_{G2} = 12\ M\Omega$, and $R_D = 10\ K\Omega$. Find I_D for the following values of R_S: $2, 4, 6, 8\ K\Omega$. Indicate the region of operation for each value of R_S.

12.7 For the common-source amplifier shown in Figure 12.23, $R_D = 10\ K\Omega$, $R_L = 1\ M\Omega$, $R_{SB} = 1.5\ K\Omega$, $R_S = 100\ \Omega$, $R_{G1} = 10\ M\Omega$, $R_{G2} = 10\ M\Omega$, $C_{C1} = C_{C2} = 2\ \mu F$, $C_S = 40\ \mu F$. The FET parameters are $C_{gs} = 10\ pF$, $C_{gd} = C_{ds} = 1.5\ pF$, $g_m = 5\ mA/V$, and $r_{ds} = 100\ K\Omega$. Use MATLAB to plot the frequency response of the amplifier.